2007 Fall: Electronic Circuits 2

CHAPTER 10
Digital CMOS Logic Circuits

Deog-Kyoon Jeong
dkjeong@snu.ac.kr
School of Electrical Engineering
Seoul National University

Introduction

- In this chapter, we will be covering…
  - Digital Circuit Design
  - Design and Performance Analysis of the CMOS Inverter

10.1 Digital Circuit Design: An Overview

- Digital IC technologies and logic-circuit families

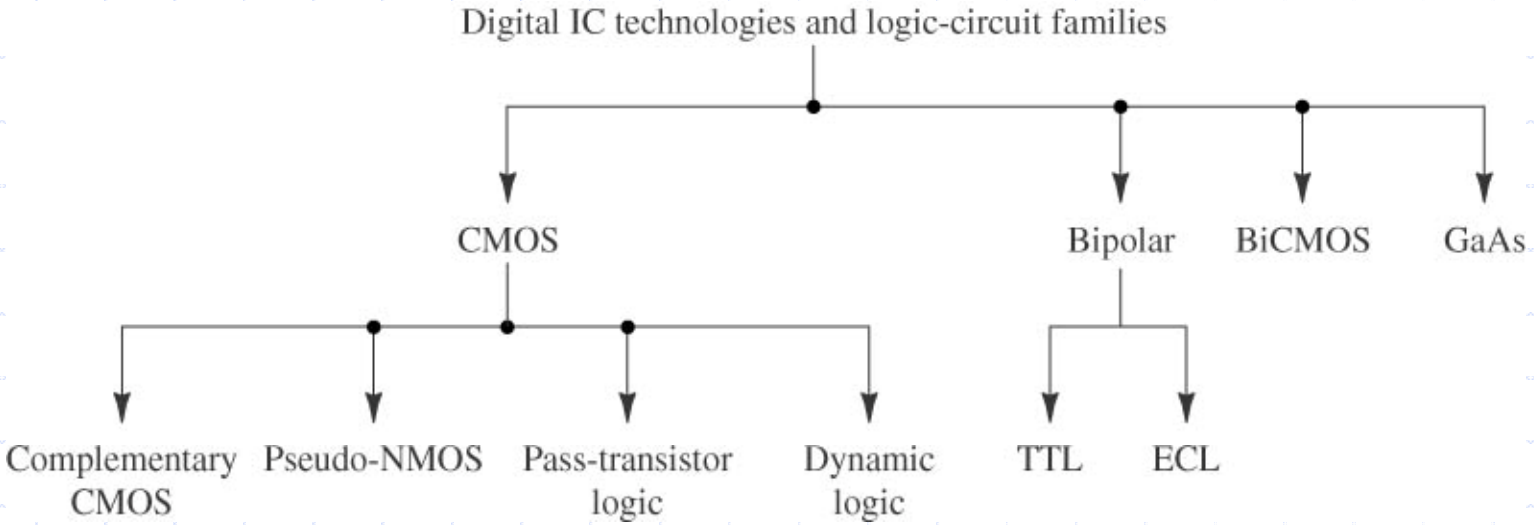


Figure 10.1 Digital IC technologies and logic-circuit families.

10.1 Digital Circuit Design: An Overview

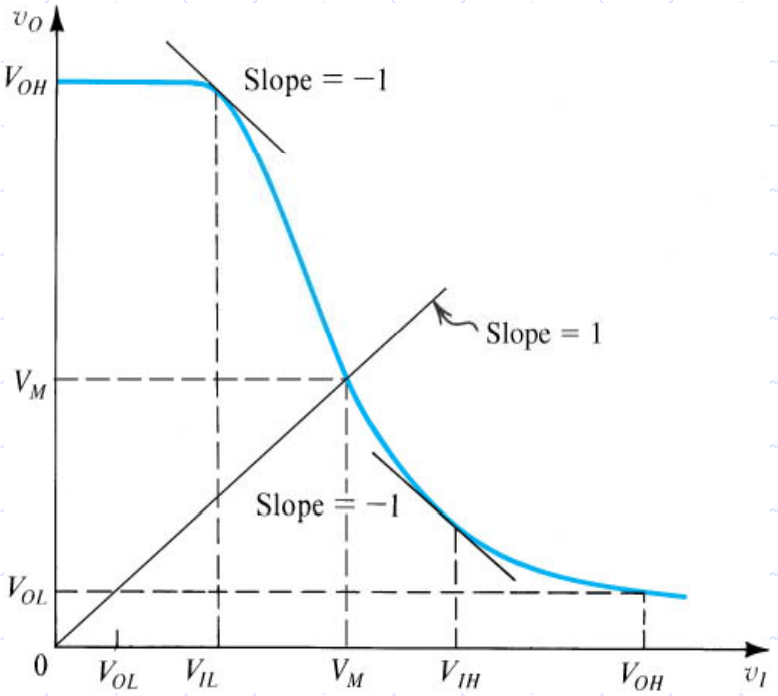
- 10.1.1 Digital IC Technologies and Logic-Circuit Families

- Brief remarks of four technology
  - **CMOS**
    - Low static power dissipation.
    - High input impedance for temporary storage.
    - Device scaling possible for higher level of integration.
    - CMOS logic types: complementary MOS (CMOS), pseudo-NMOS, pass-transistor logic and dynamic CMOS logic.
  - **Bipolar**
    - Transistor-transistor logic (TTL or Schottky TTL)
    - Emitter-coupled logic (ECL): suitable for high speed operation
  - **BiCMOS**
  - **GaAs**

10.1 Digital Circuit Design: An Overview

- 10.1.2 Logic-Circuit Characterization

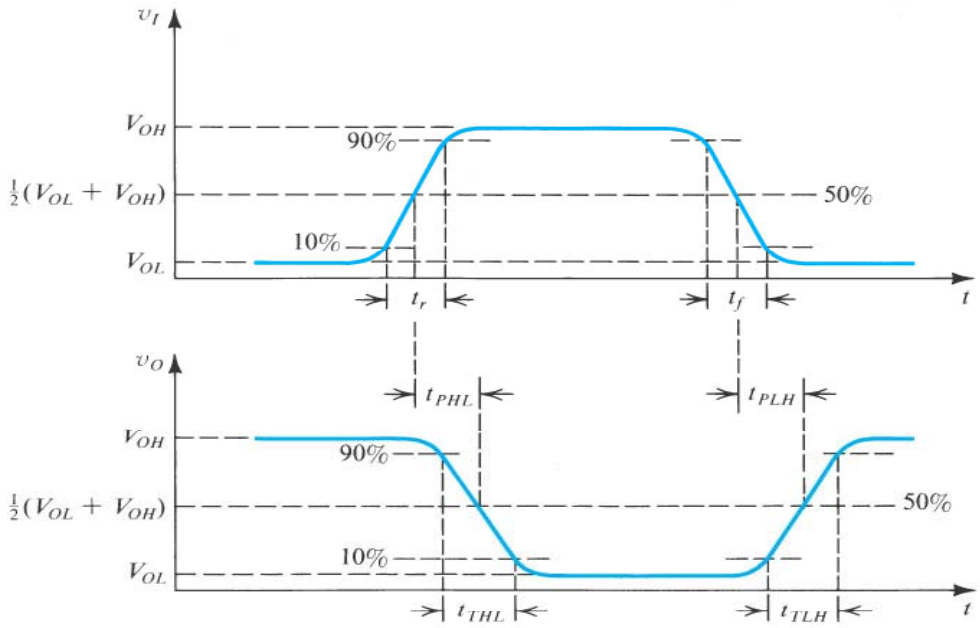
- Noise Margins
  - V_{OH}: maximum output voltage
  - V_{OL}: minimum output voltage
  - V_{IH}, V_{IL}: the point at the slope of VTC = -1
  - V_M: (logic) the point of threshold voltage at v_O=v_I
  - **$N_{MH} = V_{OH} - V_{IH}$**
  - **$N_{ML} = V_{IL} - V_{OL}$**



10.1 Digital Circuit Design: An Overview

- 10.1.2 Logic-Circuit Characterization

- Propagation Delay
  - t_{PHL} : high-to-low propagation delay
  - t_{PLH} : low-to-high propagation delay
  - t_P (propagation delay) = (t_{PLH} + t_{PHL})/2



10.1 Digital Circuit Design: An Overview

- 10.1.2 Logic-Circuit Characterization

- Power Dissipation
  - Two types of power dissipation: static and dynamic
  - Static power
    - The power that the gate dissipates in the absence of switching action
    - It results from the presence of a path in the gate circuit between the power supply and ground
  - Dynamic power
    - Occurs when the gate is switched
    - An inverter operated from a power supply V_{DD} and driving a load capacitance C, dissipates dynamic power P_D

$$P_D = fCV_{DD}^2$$

(*f* is the frequency at which the inverter is being switched)

10.1 Digital Circuit Design: An Overview

- 10.1.2 Logic-Circuit Characterization

- Delay-Power Product
  - Goal: High speed performance combined with low power dissipation.
  - Figure-of-merit for comparing logic-circuit technologies is the delay-power product, defined as

$$DP = P_D t_p$$

10.1 Digital Circuit Design: An Overview

- 10.1.2 Logic-Circuit Characterization

- Silicon Area
  - An obvious objective in the design of digital VLSI circuits is the minimization of silicon area per logic gate.

- Fan-In and Fan-Out
  - The fan-in of a gate is the number of its inputs.
  - A four-input NOR gate has a fan-in of 4.
  - Fan-out is the maximum number of similar gates that a gate can drive while remaining within guaranteed specifications.

10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.1 Circuit Structure

- The CMOS logic inverter consists of a pair of complementary MOSFETs switched by the input voltage v_I

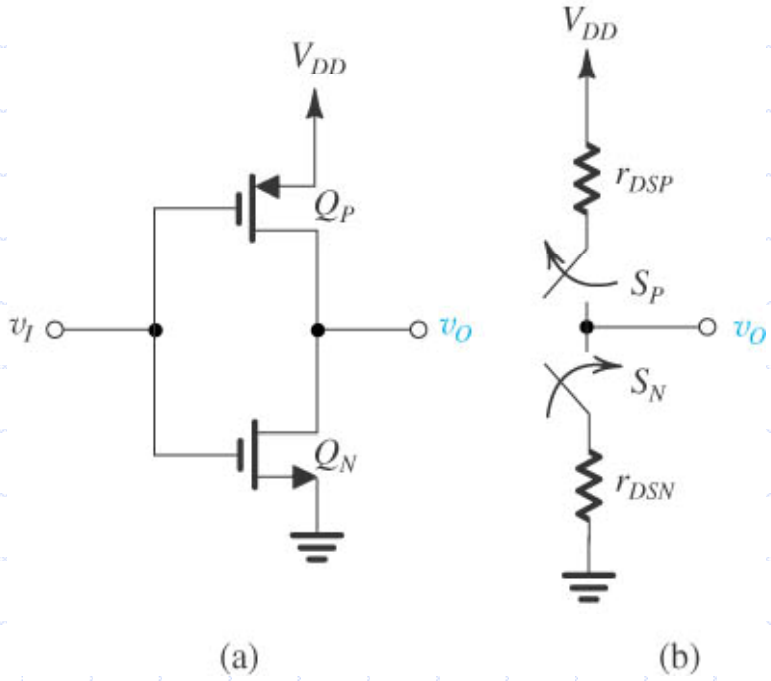


Figure 10.4 **(a)** The CMOS inverter and **(b)** its representation as a pair of switches operated in a complementary fashion.

10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.1 Circuit Structure

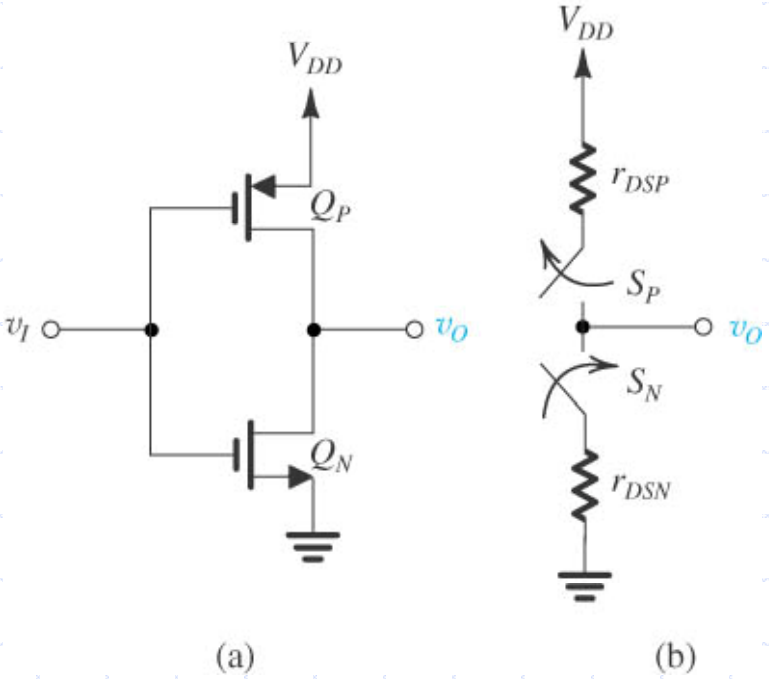


Figure 10.4 **(a)** The CMOS inverter and **(b)** its representation as a pair of switches operated in a complementary fashion.

- The source of each device is connected to its body, thus eliminating the body effect.
- Usually, the threshold voltages V_{in} V_{ip} are equal in magnitude.
- Each switch is modeled by a finite on resistance, which is the source-drain resistance of the respective transistor, evaluated near $|v_{DS}|=0$,

$$r_{DSN} = 1 \Big/ \left[k_n' \left(\frac{W}{L} \right)_n (V_{DD} - V_t) \right]$$

$$r_{DSP} = 1 \Big/ \left[k_P' \left(\frac{W}{L} \right)_p (V_{DD} - V_t) \right]$$

10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.2 Static Operation

- In the steady state, no direct-current path exists between V_{DD} and ground – the static-current and the static-power dissipation are both zero.
- The switching threshold V_{th}

$$V_{th} = \frac{V_{DD} - |V_{tp}| + \sqrt{k_n/k_p}\,V_{tn}}{1 + \sqrt{k_n/k_p}}$$

$$(k_n = k_n'(W/L)_n,\ k_p = k_p'(W/L)_p)$$

- For symmetry,

$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

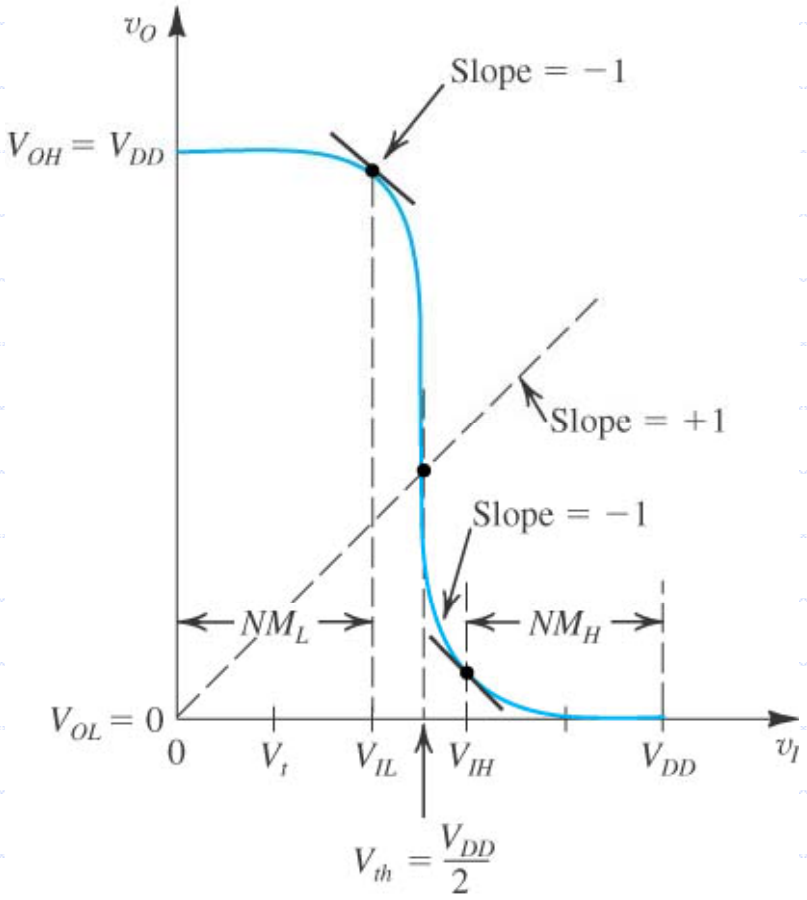


Figure 10.5 The voltage transfer characteristic (VTC) of the CMOS inverter when Q_N and Q_P are matched.

10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.2 Static Operation

- Matching condition
  - Symmetrical transfer characteristic

$$\left(\frac{W}{L}\right)_p = \frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_n$$

  - Equal driving capability for NMOS and PMOS
  - Swing threshold is $V_{DD}/2$ in matched case.
  - Noise margins in matched case:

$$NM_H = NM_L = \frac{3}{8}\left(V_{DD} + \frac{2}{3}V_t\right)$$

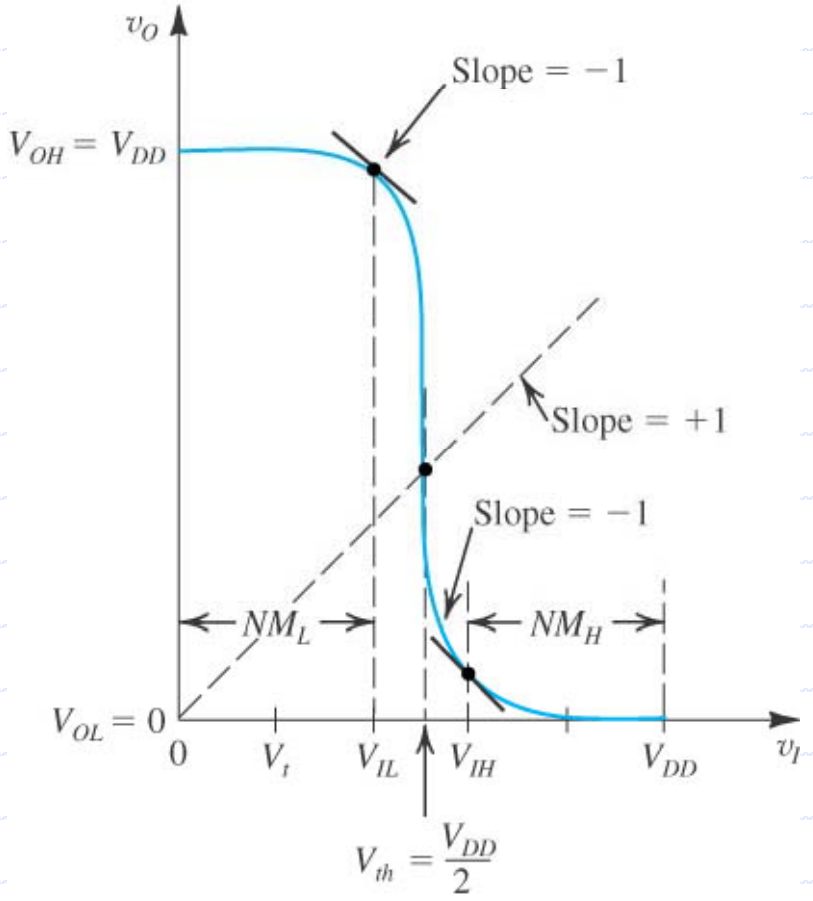


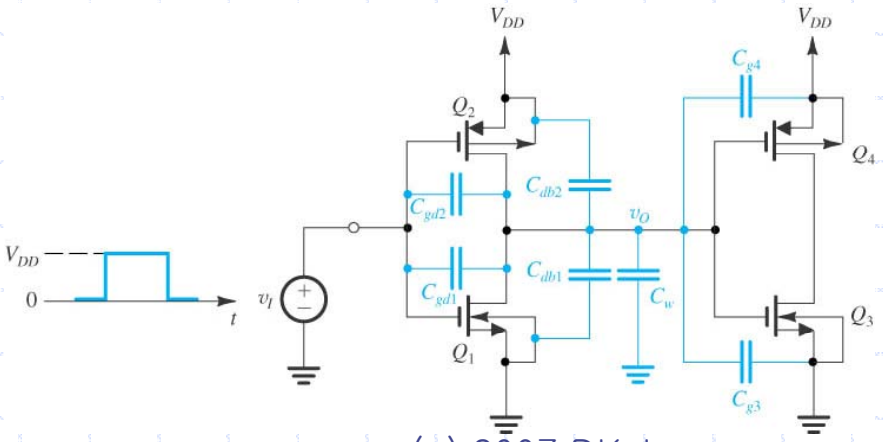
Figure 10.5 The voltage transfer characteristic (VTC) of the CMOS inverter when Q_N and Q_P are matched.

10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.3 Dynamic Operation

- Capacitance calculations
  - The gate-drain overlap capacitance→$2C_{gd}$ (2 arises because of the Miller effect.)
  - The drain-body capacitance → C_{db} (no miller effect)
  - The input capacitance of second inverter → $C_{g3}+C_{g4}$ $=(W\cdot L)_3C_{ox}+(W\cdot L)_4C_{ox}+C_{gsov3}+C_{gdov3}+C_{gsov4}+C_{gdov4}$
  - The wiring capacitance →C_w
  - The total value of load capacitance C is given by

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$



10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.3 Dynamic Operation

- Determining the propagation delays
  - Computing an average value for the discharge current during the interval t=0 to t=t_{PHL}
  - The average discharge current

$$i_{DN}\,|_{av} = \frac{1}{2}\left[i_{DN}(0) + i_{DN}(t_{PHL})\right] \quad where,$$

$$i_{DN}(0) = \frac{1}{2}k'_n\left(\frac{W}{L}\right)_N (V_{DD} - V_t)^2$$

$$i_D(t_{PHL}) = k'_n\left(\frac{W}{L}\right)_n\left[(V_{DD} - V_t)\frac{V_{DD}}{2} - \frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right]$$

  - Assuming V_t=0.2V_{DD}, t_{PHL} is

$$t_{PHL} = \frac{C\Delta V}{i_{DN}\,|_{av}} = \frac{CV_{DD}/2}{i_{DN}\,|_{av}} \approx \frac{1.7C}{k'_n\left(\frac{W}{L}\right)_n V_{DD}}$$

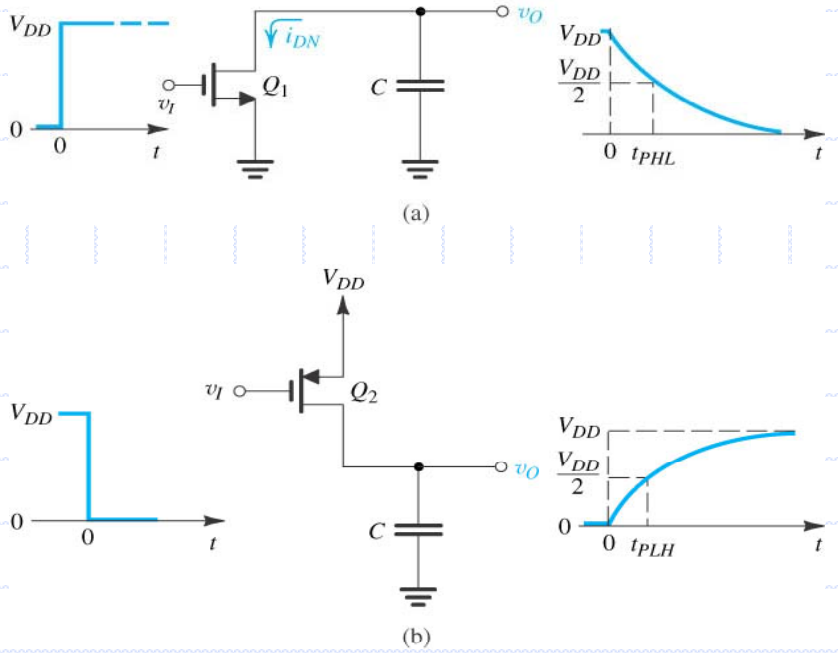


Figure 10.7 Equivalent circuits for determining the propagation delays **(a)** t_{PHL} *and* **(b)** t_{PLH} of the inverter.

10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.3 Dynamic Operation

- By analogy, t_{PLH} is

$$t_{PLH} = \frac{1.7C}{k'_p \left(\frac{W}{L}\right)_p V_{DD}}$$

- The propagation delay tp can be found as the average of t_{PHL} and t_{PLH}

$$t_P = \frac{1}{2}(t_{PHL} + t_{PLH})$$

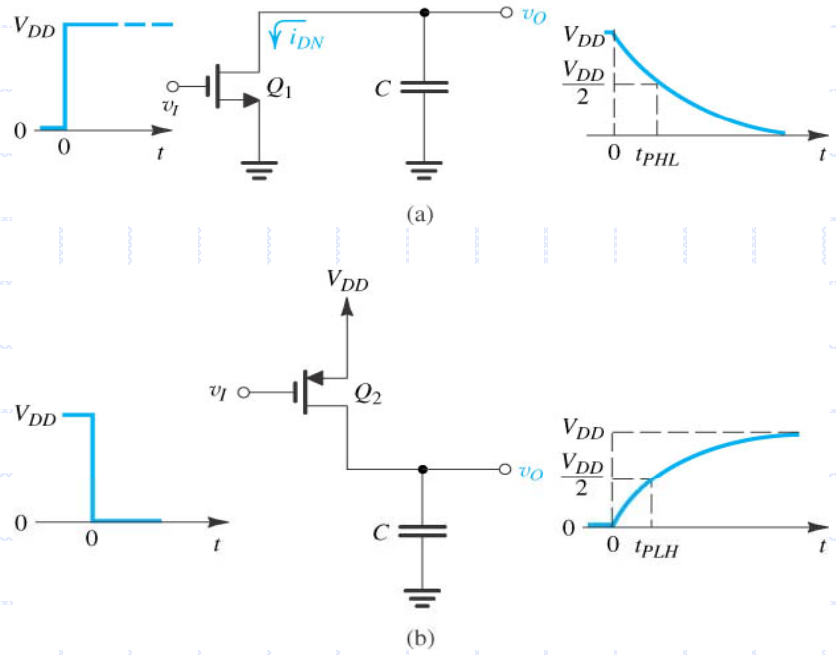


Figure 10.7 Equivalent *circuits for determining the propagation delays* ***(a)*** t_{PHL} *and* **(b)** t_{PLH} of the inverter.

10.2 Design and Performance Analysis of the CMOS Inverter

- 10.2.4 Dynamic Power Dissipation

- The dynamic power dissipated in the CMOS inverter is given by

$$P_D = fCV_{DD}^2$$

where *f* is the frequency at which the gate is switched.

10.2 Design and Performance Analysis of the CMOS Inverter

- Example 10.1

  Consider a CMOS inverter fabricated in a 0.25-μm process for which C_{ox} = 6 fF/μm^2, $\mu_n C_{ox}$ = 115 μA/V^2, $\mu_p C_{ox}$ = 30 μA/V^2, $V_{tn} = -V_{tp}$ = 0.4 V, and V_{DD} = 2.5 V. The W/L ratio of Q_N is 0.375 μm/0.25 μm, and that for Q_P is 1.125 μm/0.25 μm. The gate-source and gate drain overlap capacitances are specified to be 0.3 fF/μm of gate width. Further, the effective value of drain body capacitances are C_{dbn} = 1 fF and C_{dbp} = 1 fF. The wiring capacitance C_w = 0.2 fF. **Find t_{PHL}, t_{PLH}, and t_p.**

10.2 Design and Performance Analysis of the CMOS Inverter

- Example 10.1
  - Equivalent Capacitance

$$C_{gd1} = 0.3 \times W_n = 0.1125\, fF$$
$$C_{gd2} = 0.3 \times Wp = 0.3375\, fF$$
$$C_{db1} = 1\, fF$$
$$C_{db2} = 1\, fF$$
$$C_{g3} = 0.375 \times 0.25 \times 6 + 2 \times 0.3 \times 0.375 = 0.7875\, fF$$
$$C_{g4} = 1.125 \times 0.25 \times 6 + 2 \times 0.3 \times 1.125 = 2.3625\, fF$$
$$C_w = 0.2\, fF$$

  - Thus,

$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w = 6.25\, fF$$

10.2 Design and Performance Analysis of the CMOS Inverter

- Example 10.1
  - Average discharge current

$$i_{DN}(0) = \frac{1}{2}k'_n\left(\frac{W}{L}\right)_n(V_{DD}-V_t)^2$$
$$= 380\mu A$$

$$i_{DN}(t_{PHL}) = k'_n\left(\frac{W}{L}\right)_n\left((V_{DD}-V_t)\frac{V_{DD}}{2}-\frac{1}{2}\left(\frac{V_{DD}}{2}\right)^2\right)$$
$$= 318\mu A$$

  - Thus,

$$i_{DN|av} = \frac{i_{DN}(0)+i_{DN}(t_{PHL})}{2} = 349\mu A$$

10.2 Design and Performance Analysis of the CMOS Inverter

- Example 10.1
  - t_{PHL}

$$t_{PHL} = \frac{C(V_{DD}/2)}{i_{DN|av}} = 23.3\,ps$$

  - t_{PLH} – since $W_p/W_n=3$ and $\mu_n/\mu_p=3.83$, the inverter is not perfectly matched. Therefore, we expect t_{PLH} to be greater than t_{PHL} by a factor of 3.83/3=1.3, thus

$$t_{PLH} = 1.3 \times 23.3 = 30\,ps$$

  - Thus,

$$t_p = \frac{t_{PHL} + t_{PLH}}{2} = 26.5\,ps$$