Analog Electronic Circuits
Department of Electrical and Computer Engineering
Seoul National University

Midterm Exam 1

October 6, 2014 D.K. Jeong

A sheet of one-sided, A4-size note is allowed.

Roster Number (학번):

Name:

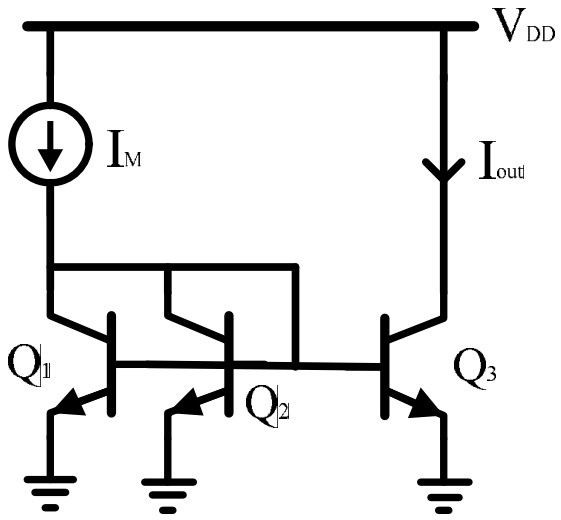
Signature :

Problem	**Max Score**	**Score**
1	20	
2	40	
3	40	
Total	100	

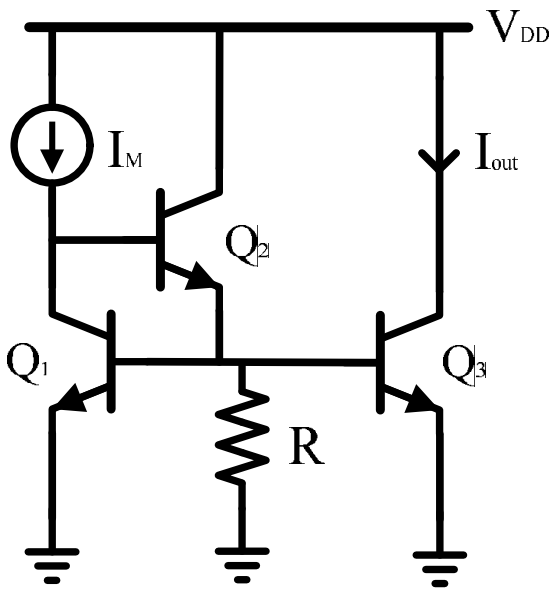
[1] Find the **output current** of each of the following current mirrors.

Assume that all the BJT transistors are operated in the **active** region and MOS transistors are operated in the **saturation** region. Also, assume that the sizes of the transistors are same. Neglect the Early effect or channel length modulation. Use V_T =26mV, β=100, I_S=2.0156*10^{-15}A, $V_{BE,active,1}$ =0.7V, R=1kΩ ,V_{TN} =0.5V, V_{TP} =-0.5V, and I_M=1mA.

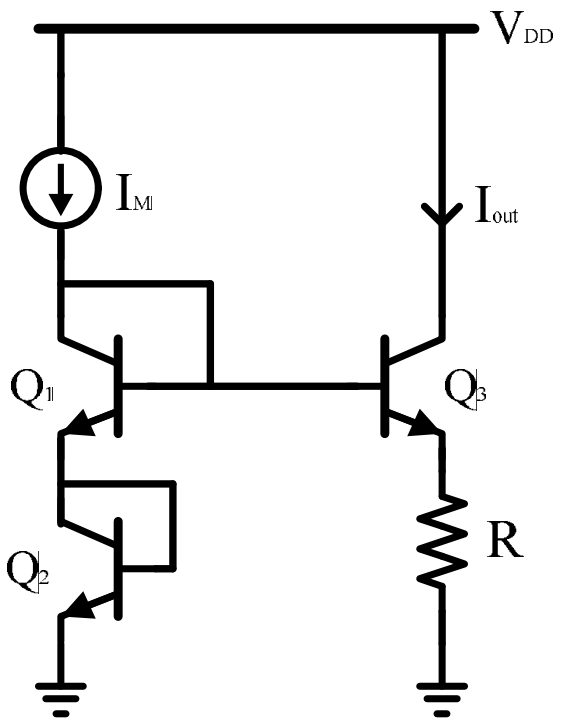
A.



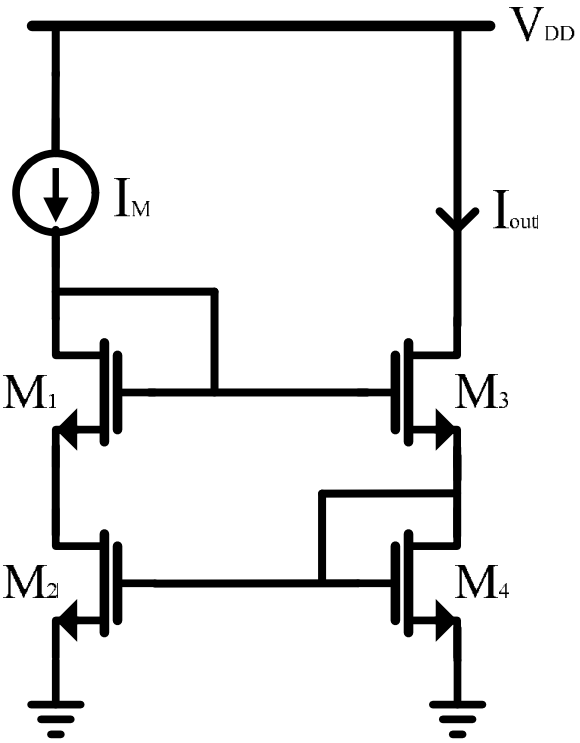
B.



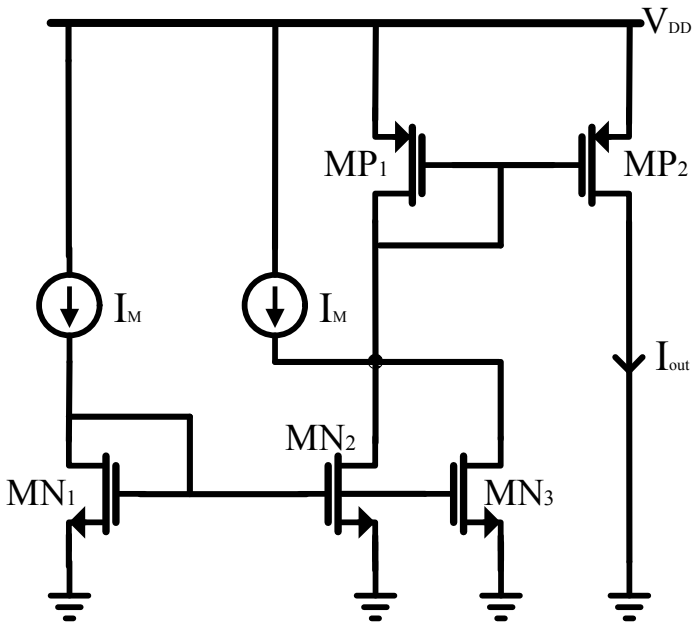
C.



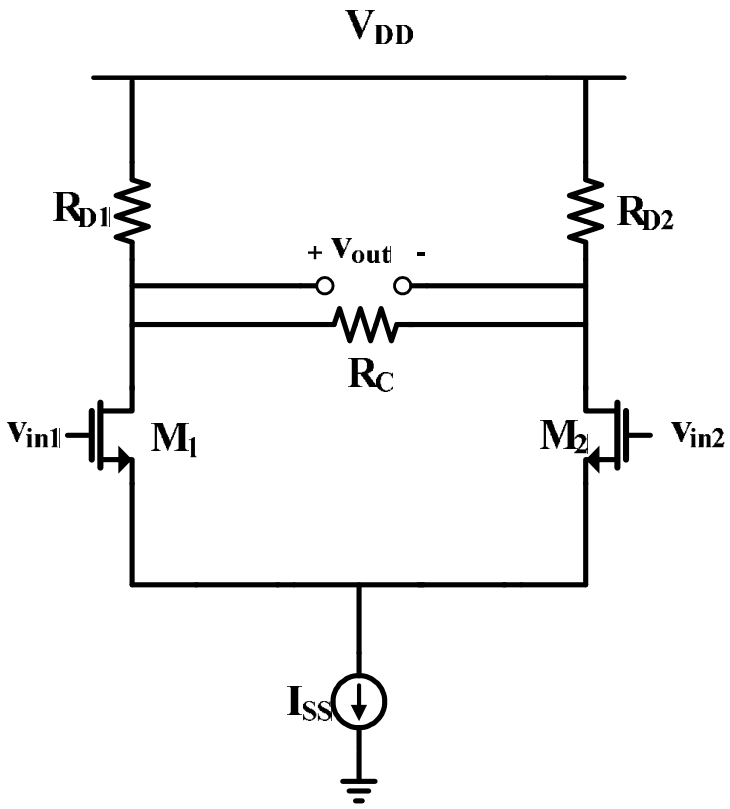
D.



E.



[2] For the following MOS differentialamplifier, use $\mu_n C_{ox}$= 100μA/V^2, R_{D1}=R_{D2}=5kΩ, R_C=10kΩ, V_{DD}=10V, V_{TN} = 0.5V, and I_{SS}=1mA. Assume λ=0 for simplicity.



A. Determine (W/L) of the input transistors if all the tail current completely steered into one leg of the differential path when $|V_{in1}-V_{in2}|_{max}$ =100mV. (In other words, $|V_{in1}-V_{in2}|_{max}$ is the input voltage difference that places one of the transistors at the edge of conduction.)

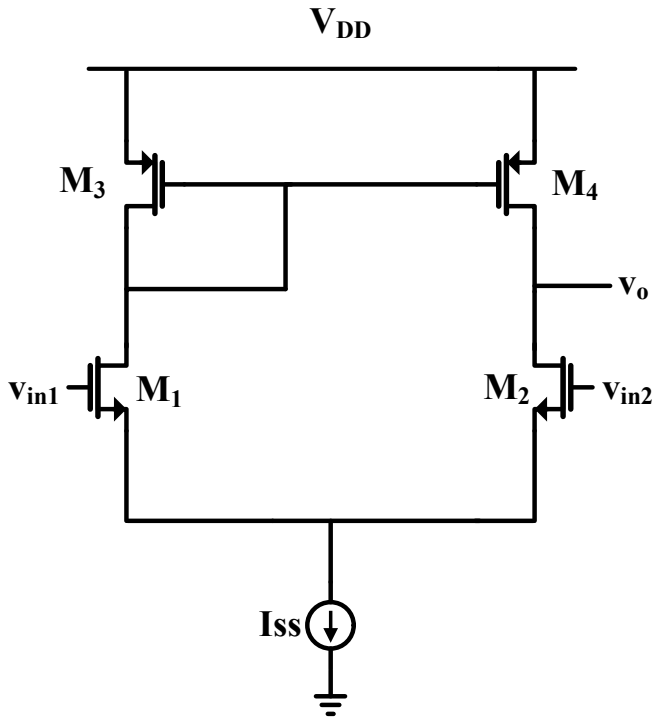
B. Assuming that V_{CM}= 5V at the inputs, determine the DC bias voltages of all the nodes and indicate them in the circuit above using the result of A. Assuming that the tail current source works only above 0.5V, what is the allowable range of the input CM level?

C. Find the input and output resistances, R_{in} and $R_{out.}$

D. Calculate the small-signal voltage gain A_v at equilibrium using the results of A.

E. When (W/L) of one of the input transistors is changed by 1%, what are the input and output offset voltages?

[3] For the following circuit, answer the questions. Use $\mu_n C_{ox}$= 100μA/V^2, λ=0.02V^{-1}, V_{TN}= -V_{TP}=0.5V, V_{DD}=5V, I_{SS}=1mA, $(\frac{W}{L})_1 = (\frac{W}{L})_2$=20,and$(\frac{W}{L})_3 = (\frac{W}{L})_4$=40.



A. What is its small-signal voltage gain A_v?

B. We want to double A_v from the value given in A. Calculate the width of the input transistors.

C. We want to double A_v from the value given in A. Calculate the tail current. Do not use the results of B.

D. If we double the widths of the two PMOS transistors in the current mirror, how much does A_v change?

E. Assume $\lambda \propto 1/L$, how much does the A_v change if we double L and W of all the MOS transistors?

{End of Midterm 1}