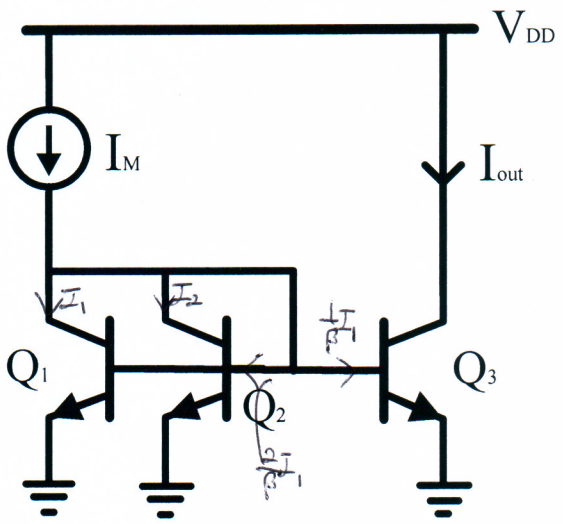
☆B, C에서만☆ 〈Sol〉

[1] Find the **output current** of each of the following current mirrors.

Assume that all the BJT transistors are operated in the **active** region and MOS transistors are operated in the **saturation** region. Also, assume that the sizes of the transistors are same. Neglect the Early effect or channel length modulation. Use V_T =26mV, β=100, I_S=~~2.0136*10^-15~~A, $V_{BE,active,1}$ =0.7V, R=1kΩ, V_{TN} =0.5V, V_{TP} =-0.5V, and I_M=1mA.

$\boxed{2\times10^{-15}A}$

A.

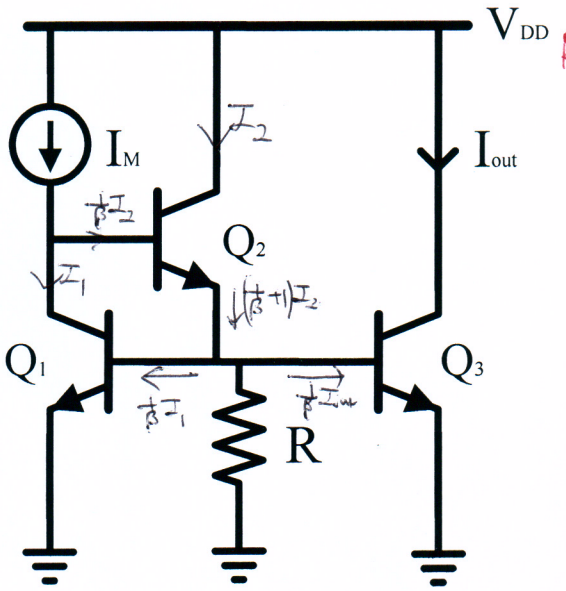


$V_{BE1} = V_{BE2} = V_{BE3} \Rightarrow I_{out} = I_1 = I_2$

$\left(\frac{3}{\beta}+2\right)I_1 = I_M \qquad I_1 = \frac{I_M}{\frac{3}{\beta}+2} \doteq \boxed{0.49261(mA)}$

(*)

B.



KCL (*)

① $\left(\frac{1}{\beta}+1\right)I_2 = \frac{V_{BE,1}}{R} + \frac{1}{\beta}(I_1+I_1) \Rightarrow I_2 = \frac{\beta}{\beta+1}\left\{\frac{V_{BE,1}}{R} + \frac{2I_1}{\beta}\right\}$

② $I_M = I_1 + \frac{1}{\beta}I_2$

$= I_1 + \frac{1}{\beta+1}\left\{\frac{V_{BE,1}}{R} + \frac{2I_1}{\beta}\right\}$

$I_1\left(1+\frac{2}{(\beta+1)\beta}\right) = I_M - \frac{1}{\beta+1}\frac{V_{BE1}}{R}$

$I_{out} = I_1 = \frac{I_M - \frac{1}{\beta+1}\frac{V_{BE1}}{R}}{1+\frac{2}{\beta(\beta+1)}} \doteq \boxed{0.99287\ (mA)}$ (V_{BE3} 영향X)

↓

$\frac{\pi}{2}$에서 1) Since $V_{BE1} = V_{BE3} \Rightarrow I_{out} = I_1$

$\frac{\pi}{2}$에서 2) $I_{out} = I_1 = I_S \exp\left(\frac{V_{BE1}}{V_T}\right)$ (*)

$\doteq \boxed{0.985312\ (mA)}$ (V_{BE3} 영향)

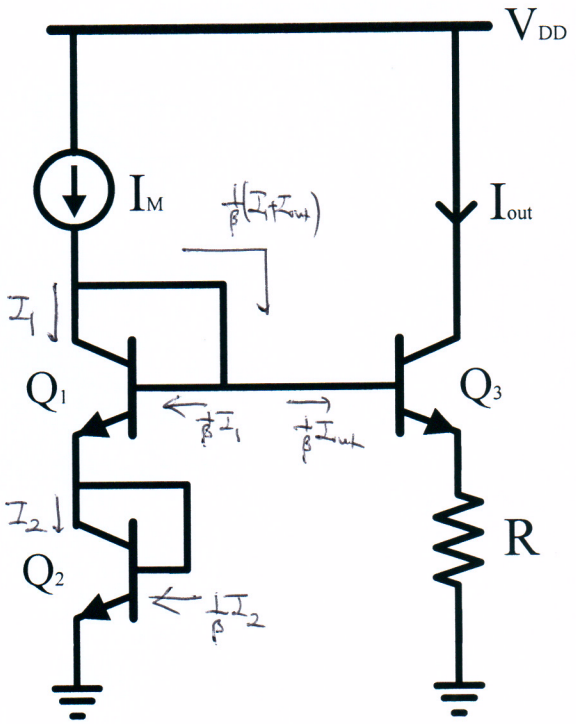
→ 훨씬 영향

$\frac{\pi}{2}$에서 3) from KCL(*) ②

② $\frac{1}{\beta}I_2 = 10^{-3} - I_1 \doteq 1.4688\times10^{-3}$

① $\left(\frac{1}{\beta}+1\right)I_2 = \frac{V_{BE1}}{\beta} + \frac{V_{BE}}{R} + \frac{I_{out}}{\beta} \Rightarrow \boxed{I_{out} \doteq 0.0177\ A}$

C.



$\frac{I}{2}$에서) $I_1 + \frac{1}{\beta} I_1 = I_2 + \frac{1}{\beta} I_2 \Rightarrow I_1 = I_2 = I_s \exp\left(\frac{V_{BE_1}}{V_T}\right) \doteq 0.9853m$

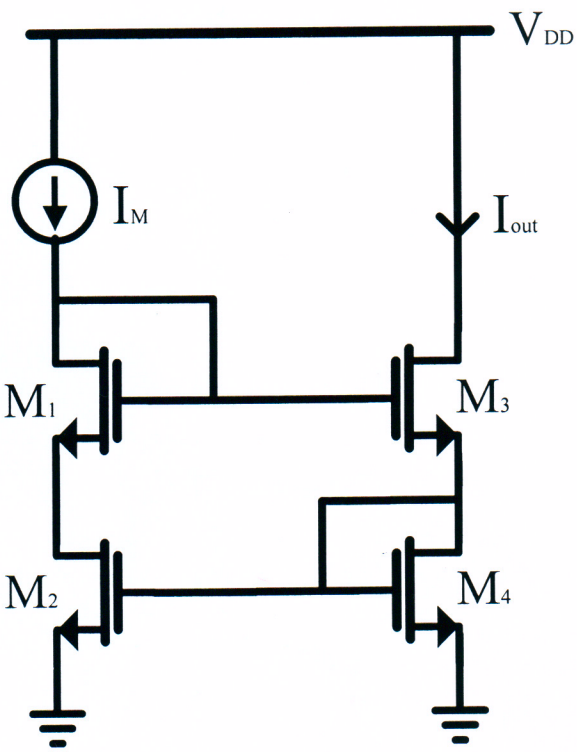
KCL) (*) $I_M = \frac{\beta+1}{\beta} I_1 + \frac{1}{\beta} I_{out}$

$\Rightarrow I_{out} = \beta I_M - (\beta+1) I_s \exp\left(\frac{V_{BE_1}}{V_T}\right) \doteq$ $\boxed{0.515\,(mA) \sim 0.4834\,(mA)}$ (R이용X)

$\frac{I}{2}$에서) (*) $I_{out} = I_s \exp \frac{1.4 - R\frac{\beta+1}{\beta} I_{out}}{V_T}$

$\boxed{I_{out} \doteq 0.702\,(mA)}$ (R이용)

D.



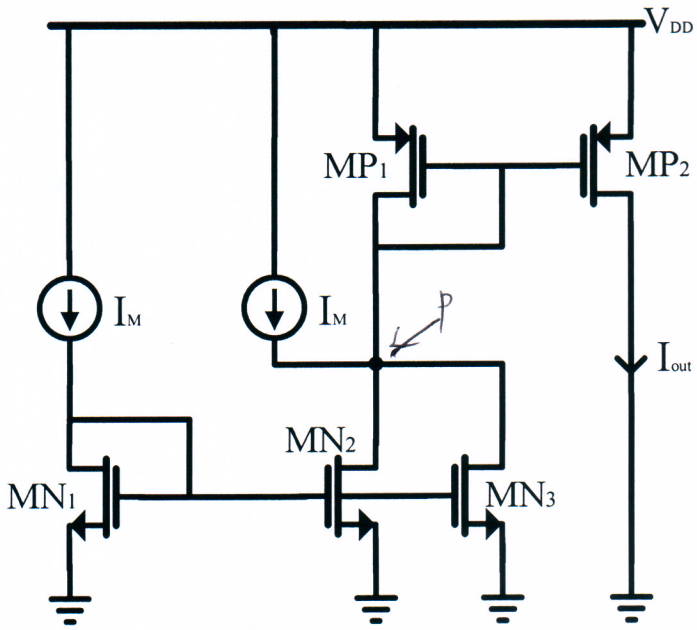
$I_{out} = I_3 = I_4$, $I_M = I_1 = I_2$

$V_{GS2} = V_{GS4}$

Since, all transistors operate in the saturation region,

$I_2 = I_4$ $\boxed{\therefore I_{out} = I_M}$

E.



$I_M = I_1 = I_2 = I_3$

@node P, Use KCL

$I_{P_1} = I_M - I_{P_2} = I_{out}$

$\boxed{\therefore I_{out} = I_M}$

〈채점기준〉 각 4점 계산 실수시 -1점

A. 답이 틀린경우, (*)식 있으면 2점

(*) 근사시, 정당한 적분, 이유 명시해야 만점. 단순히 $\frac{1}{2}$mA ⇒ 1점

B. 답이 틀린경우,

풀이 1과 풀이 2) (*)식 있으면 2점

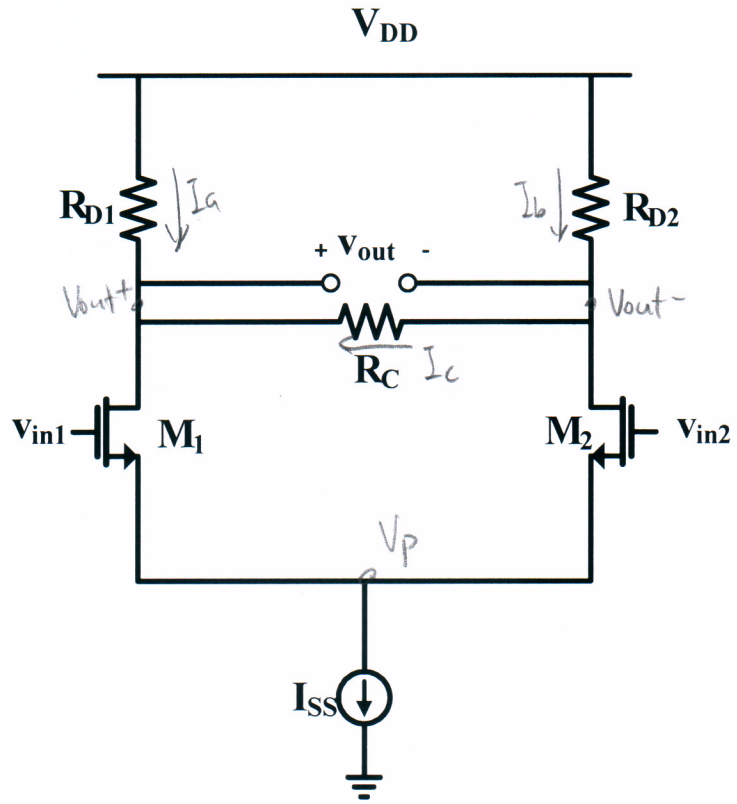
풀이가 중요. (KCL or BJT equation) 어느 지점을 잡고 푸느냐에 따라 답이 달라집니다. 그래서 부분점수를 후하게 주었습니다.

C. 〃 2점

D와 E. 답 틀리면 0점

중간1차 시험 2번 채점 기준.

[2] For the following MOS differentialamplifier, use $\mu_n C_{ox}$= 100μA/V^2, R_{D1}=R_{D2}=5kΩ, R_C=10kΩ, V_{DD}=10V, V_{TN} = 0.5V, and I_{SS}=1mA. Assume λ=0 for simplicity.



[6점] A. Determine (W/L) of the input transistors if all the tail current completely steered into one leg of the differential path when $|V_{in1}-V_{in2}|_{max}$ =100mV. (In other words, $|V_{in1}-V_{in2}|_{max}$ is the input voltage difference that places one of the transistors at the edge of conduction.)

모든 전류가 M1 으로 흐른다고 했을 때, $I_{D1} = I_{SS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS1}-V_{TN})^2$

$\Rightarrow V_{GS1} = \sqrt{\frac{2I_S}{\mu_n C_{ox}\frac{W}{L}}} + V_{TN}$ $\quad V_{GS2} = V_{TN}$ ($\because$ M_2가 edge of conduction)

$\therefore |V_{in1}-V_{in2}|_{max} = |V_{GS1}-V_{GS2}| = \sqrt{\frac{2I_S}{\mu_n C_{ox}\frac{W}{L}}} = 0.1$ [V] (3)

$\therefore \frac{W}{L} = 2\times10^3$ (3)

[6+6점] B. Assuming that V_{CM}= 5V at the inputs, determine the DC bias voltages of all the nodes and indicate them in the circuit above using the result of A. Assuming that the tail current source works only above 0.5V, what is the allowable range of the input CM level?

$I_{D1} = I_{D2} = \frac{I_{SS}}{2} = 0.5mA$ (1)

$V_{out+} = V_{DD} - I_{D1}R_{D1} = 7.5V$ (1)

$V_{out-} = V_{DD} - I_{D2}R_{D2} = 7.5V$ (1)

$\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{CM}-V_p-V_{TN})^2 = \frac{I_{SS}}{2}$ (1)

$\Rightarrow V_p = 4.43$ or 4.57

$\Rightarrow V_p = 4.43V$ (2) (MOS가 sat. region 이기 위해서)

MOS가 sat. region 이기위한 조건

① $V_{DS} > V_{GS} - V_{TN}$

$V_{CM} < V_{DS} + V_{TN} + V_S = V_D + V_{TN} = 8V$ (2)

MOS가 $\frac{I_{SS}}{2}$ 의 전류를 흘릴수 있기위한 조건

$(V_{GS}-V_{TN})_{equil} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$ (2)

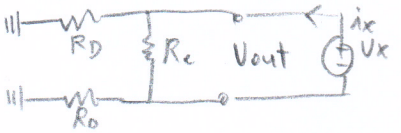
$\Rightarrow V_{CM} > 1.07V$

$\therefore 1.07V < V_{CM} < 8V$ (1)

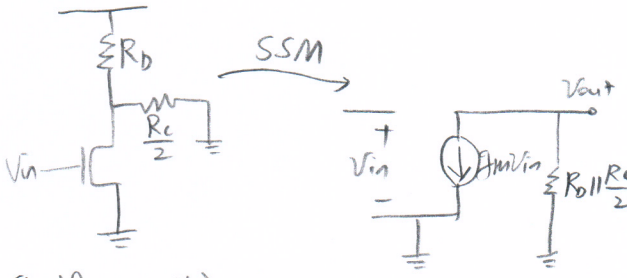
[5점] C. Find the input and output resistances, R_{in} and R_{out}.

gate 로 들어가는 전류 = 0 ⇒ $i_x = 0$ ⇒ $R_{in} = \infty$ (2)

Vin을 short 시키고 SSM을 그려보면



$\therefore R_{out} = \frac{V_x}{i_x} = R_c \parallel (R_D + R_D) = 5k\Omega$ (3)



<half circuit>

* 문제에서 모호의 소지가 있어, half circuit 의 Rin Rout 을 구한 경우도 정답처리함 ($R_{in} = \infty$, $R_{out} = R_D \parallel \frac{R_c}{2} = 2.5k\Omega$)

[5점] D. Calculate the small-signal voltage gain A_v at equilibrium using the results of A.

위 의 half circuit small signal model 에서

$$V_{out} = -g_m V_{in} \left(R_D \parallel \frac{R_c}{2}\right)$$

$$\therefore A_v = \frac{V_{out}}{V_{in}} = -g_m \left(R_D \parallel \frac{R_c}{2}\right) \quad (2)$$

$$= -\sqrt{2 \cdot \mu_n C_{ox} \frac{W}{L} \cdot \frac{I_{SS}}{2}} \cdot \left(R_D \parallel \frac{R_c}{2}\right) = -35.3553 \ [V/V] \quad (3)$$

* 부호 틀릴 시 (-1)

[12점] E. When (W/L) of one of the input transistors is changed by 1%, what are the input and output offset voltages?

M1 의 (W/L) 이 1% 커졌다고 가정. R_{D1} 에 흐르는 전류 : I_a, R_{D2} 에 흐르는 전류 : I_b, R_c 에 흐르는 전류 : I_c, 라고 하면,

Vout+ node 에서 KCL : $I_a + I_c = I_{D1} = I_D + \Delta I_D$

Vout- node 에서 KCL : $I_b - I_c = I_{D1} = I_D$

$$(I_D + \Delta I_D) + I_D = 2I_D + \Delta I_D = 2.01 I_D = I_{SS} \Rightarrow I_D = \frac{100}{201} I_{SS},\ \Delta I_D = \frac{1}{201} I_{SS}$$

(2)

$V_{out+} = V_{DD} - I_a R_D$

$V_{out-} = V_{DD} - I_b R_D$

$$V_{out+} - V_{out-} = -I_c R_c = R_D (I_b - I_a)$$

$$= R_D (I_c + I_D - (I_D + \Delta I_D - I_c))$$

$$= R_D (2I_c - \Delta I_D)$$

$$\Rightarrow I_c = \frac{R_D \Delta I_D}{R_c + 2R_D}$$

$$= \frac{5k}{10k + 10k} \times \frac{1}{201} I_{SS}$$

$$= 1.24 \mu A$$

(4)

* 다른 방식으로 풀었어도 식이 옳으면 만점.
(R_c를 고려하지 않고 풀면 부분점수 없음)

$$\therefore V_{out.offset} = I_c \cdot R_c = (1.24\mu A) \cdot (10k\Omega) = 12.4 mV \quad (2) \quad (1)$$

$$V_{in.offset} = \frac{V_{out.offset}}{|A_v|} = 350.7 \mu V \quad (2) \quad (1)$$

E. 다른 풀이.

input에 ΔV 의 offset이 걸려서 $I_{D1} = I_{D2} = \frac{I_{SS}}{2}$ 라고 할 때, (2)

$$V_{GS1} - V_{th} = V_{in} + \Delta V - V_S - V_{th} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L} \cdot (1.01)}}$$

$$- \left(V_{GS2} - V_{th} = V_{in} - V_S - V_{th} = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}} \right)$$ (4)

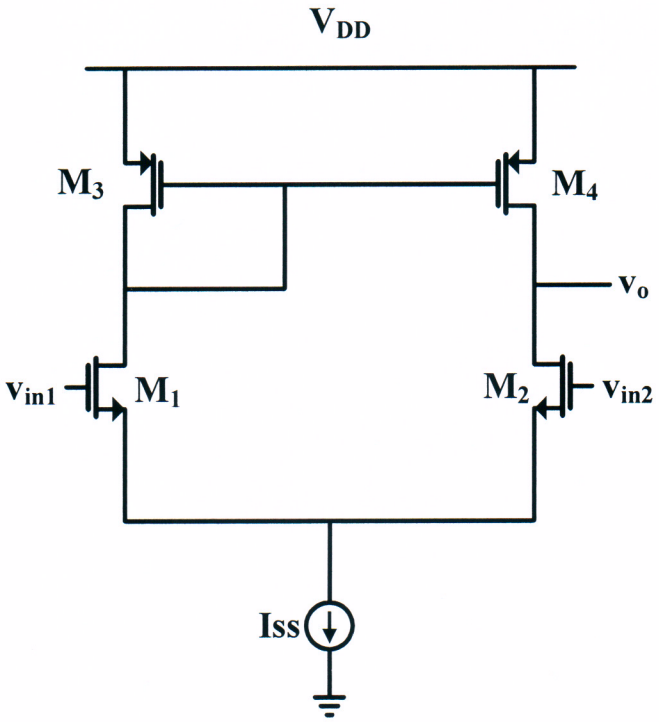
$$\Delta V = \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L} (1.01)}} - \sqrt{\frac{I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$ (2)

$$= -350.9\mu V$$

$$\therefore V_{in.offset} = |\Delta V| = \underline{350.9\mu V}$$ (1)

$$\underline{V_{out.offset} = |V_{in.offset} \cdot A_v|}$$ (2) $$= \underline{12.4\,mV}$$ (1)

[3] For the following circuit, answer the questions. Use $\mu_n C_{ox}$= 100μA/V^2, λ=0.02V^{-1}, V_{TN}= -V_{TP}=0.5V, V_{DD}=5V, I_{SS}=1mA, $(\frac{W}{L})_1 = (\frac{W}{L})_2$=20,and$(\frac{W}{L})_3 = (\frac{W}{L})_4$=40.



A. What is its small-signal voltage gain A_v? [8 pts]

$$g_{m2} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_2 \cdot I_D} = \sqrt{2\times100\times10^{-6}\times20\times\frac{10^{-3}}{2}} = \sqrt{2}\ mS$$

$$r_{o2} = \frac{1}{\lambda I_D} = \frac{1}{0.02\cdot\frac{10^{-3}}{2}} = 100k\Omega = r_{o4}$$

$$A_v = g_{m2}(r_{o2} \| r_{o4}) = 50\sqrt{2}$$

* 다 맞으면 8점
식만 맞으면 3점 (gain 구하는 식이 맞아야 함) 숫자를 대입하기 직전의
제대로 된 식도 없으면 0점.

(부호 실수 -3
단순계산 실수 -3

B. We want to double A_v from the value given in A. Calculate the width of the input transistors. [8pts]

$(\frac{W}{L})_1 = (\frac{W}{L})_2 = 80 \Rightarrow g_{m2}$가 4배 $\Rightarrow A_v$ 2배.

* 설명과 답이 다 있으면 8점
답은 맞는데 설명이 충분하지 않은 경우 4점. 일부 맞는 내용 있으면 2점.
둘 다 없거나 틀렸으면 0점

C. We want to double A_v from the value given in A. Calculate the tail current. Do not use the results of B.

[8 pts]

$I_{ss} = 0.25mA \Rightarrow$ g_{m_2} $\frac{1}{2}$배, r_{o_2}, r_{o_4} 4배 $\Rightarrow A_v$ 2배.

* B와 같은 기준

D. If we double the widths of the two PMOS transistors in the current mirror, how much does A_v change?

[8 pts]

PMOS의 width (혹은 $\frac{W}{L}$ 비율)를 증가시켜도 $A_v = g_{m_2}(r_{o_2} \| r_{o_4})$ 에 영향 X.
따라서 A_v는 변하지 않는다.

* B와 같은 기준

E. Assume $\lambda \propto 1/L$, how much does the A_v change if we double L and W of all the MOS transistors?

[8 pts]

L, W 2배 $\Rightarrow r_{o_2}, r_{o_4}$ 2배 $\Rightarrow A_v$ 2배.

* B와 같은 기준

{End of Midterm 1}