Design Styles

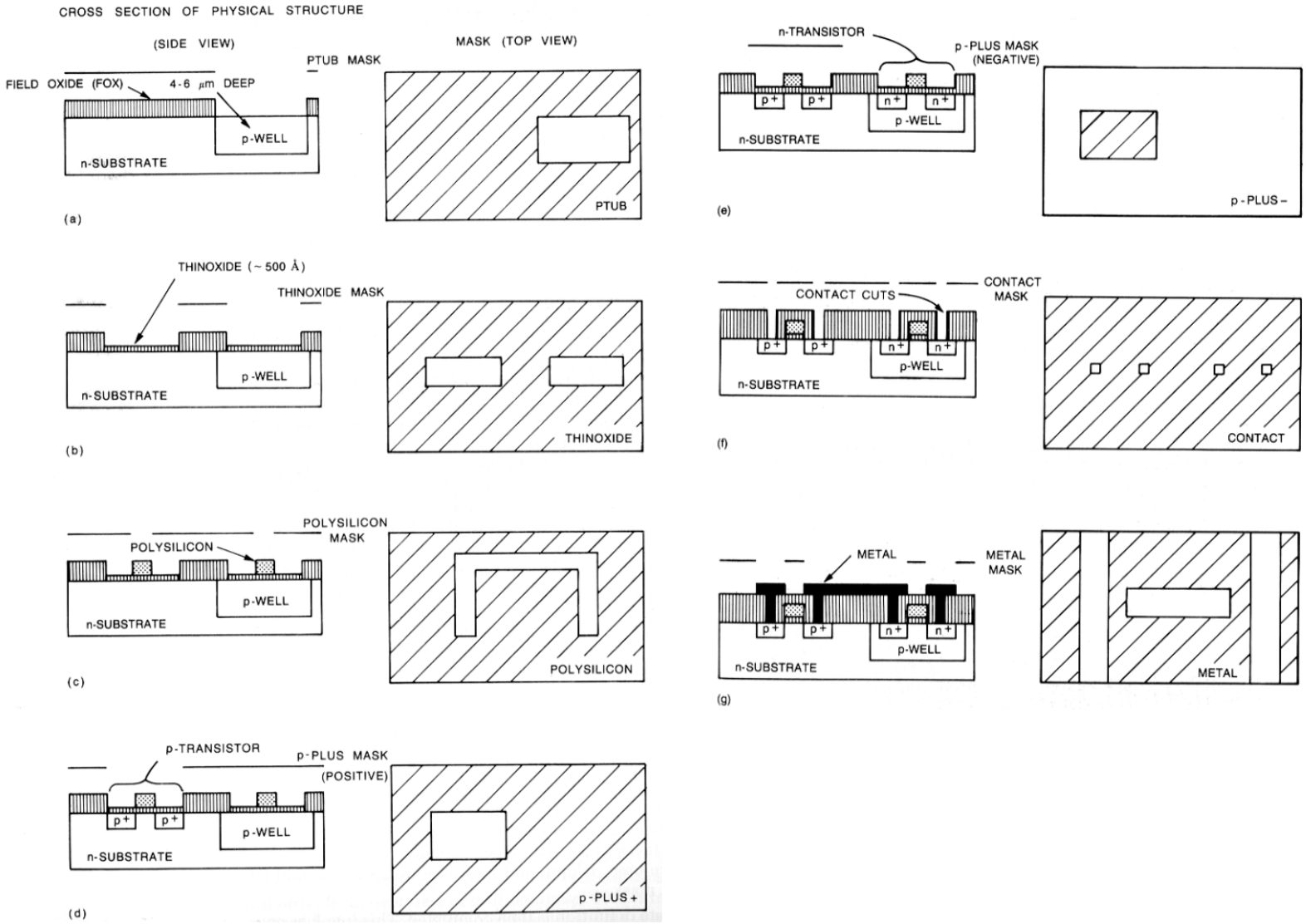
(4541.554 Introduction to Computer-Aided Design)

School of EECS

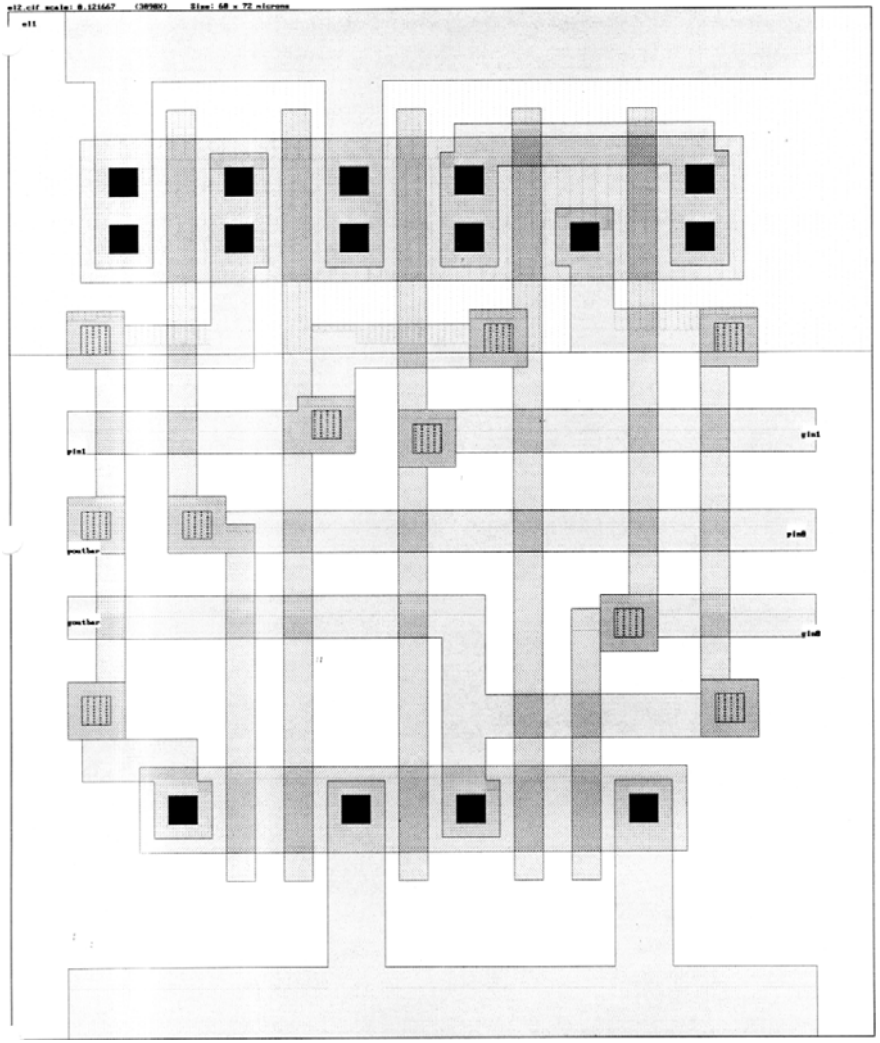
Seoul National University

IC Fabrication and Mask Layout Design

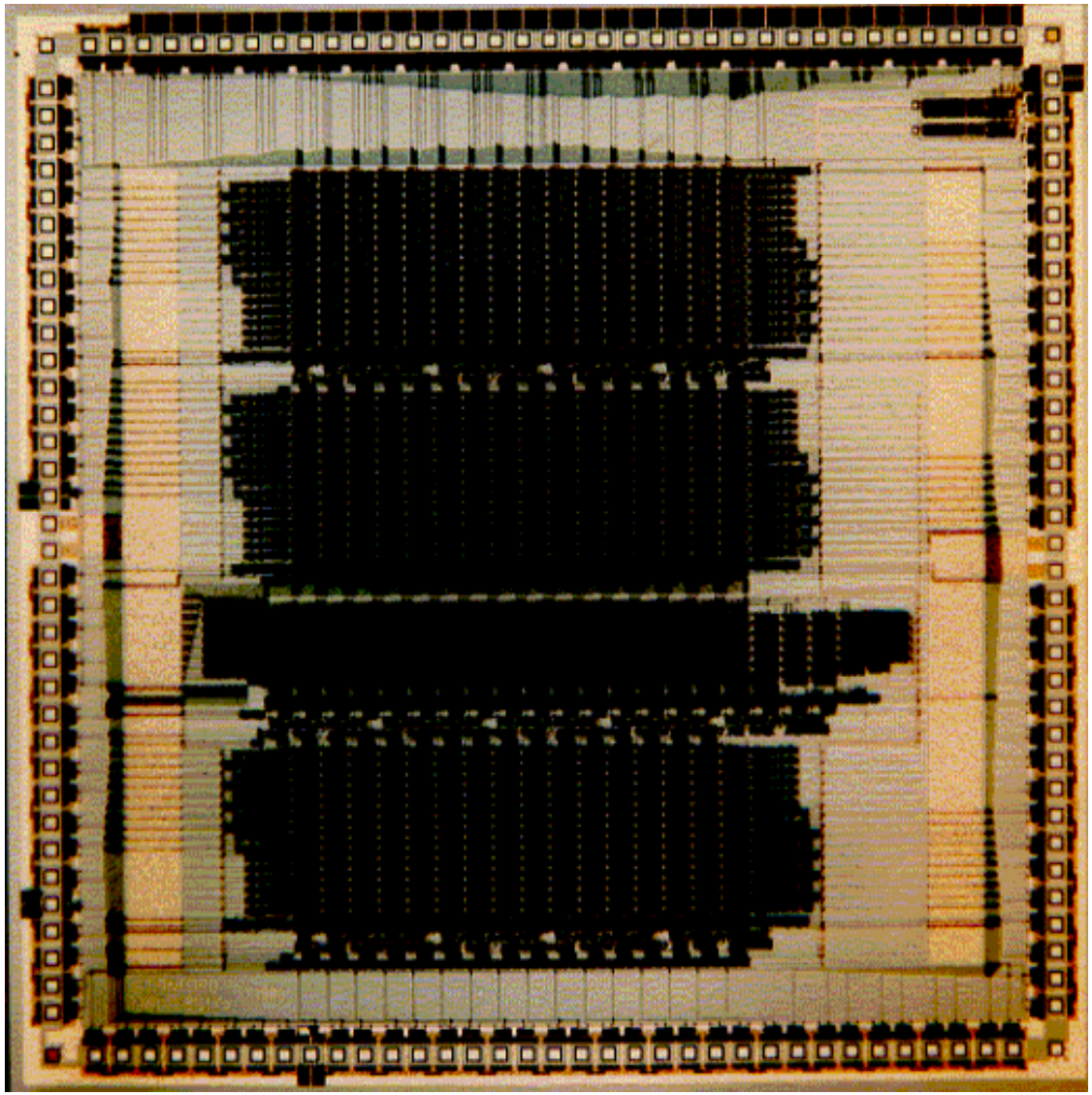
- **Fabrication Process**



- **Cell Layout**



- **IC Layout**



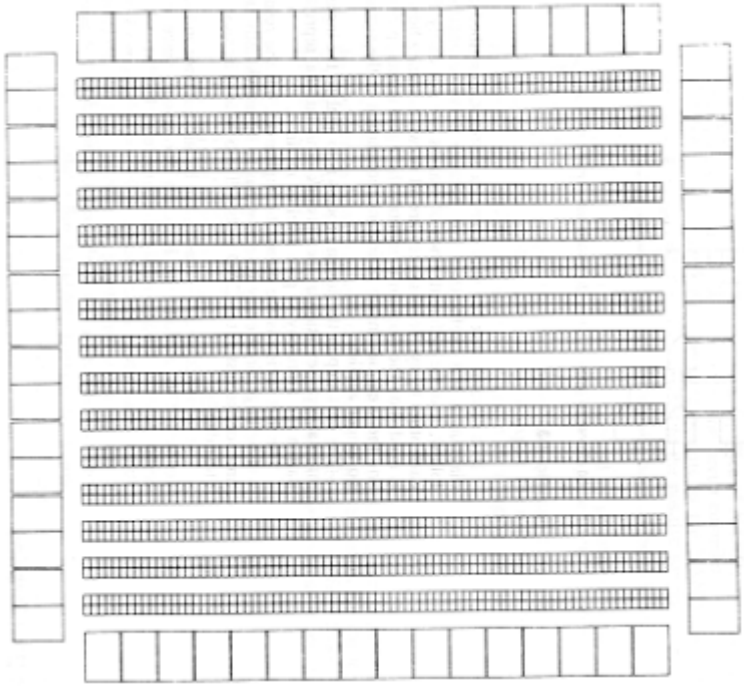
Taxonomy of Design Style

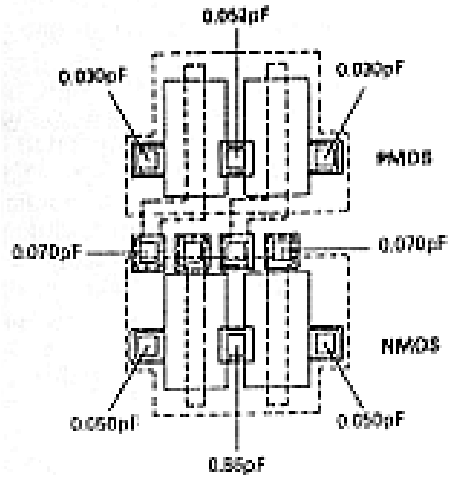
- **According to Fabrication Method**
  - **Custom fabrication**
  - **Mask-programmable gate array**
    - **Gate array**
    - **Sea of gate**
  - **Field-programmable device**
- **According to Design Method**
  - **Full custom design**
  - **Standard cell design**
  - **Macro-cell design**
  - **IP/platform-based design**

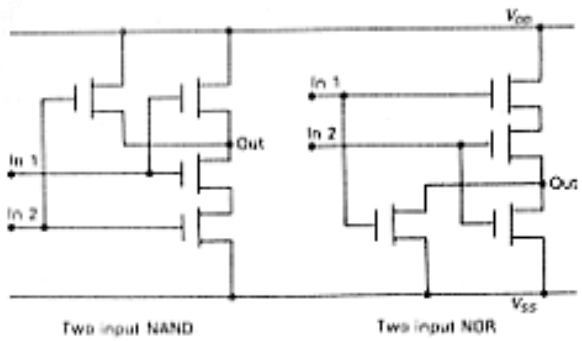
- **Custom Fabrication**
  - **Custom-made masks**
  - **Goes thru all fabrication processes**
  - **Can obtain best performance**
  - **High fabrication cost**
  - **Takes long time (several months)**
  - **Mass production helps lower unit cost.**

- **Mask-Programmable Gate Array**
  - **Pre-production of wafers containing arrays of transistors/gates.**
  - **Gate Array**
    - **Array of sites(gates)**
    - **1 - 2 interconnection layers are used within a site.**
    - **Site-to-site interconnection uses 1 - 3 interconnection layers and routing channels.**
    - **Less number of custom-made masks and lower NRE (Non-Recurring Engineering) cost**
    - **Fast turnaround**
  - **Sea of Gate**
    - **Gate array with no fixed routing channel**
    - **Routing over active area**

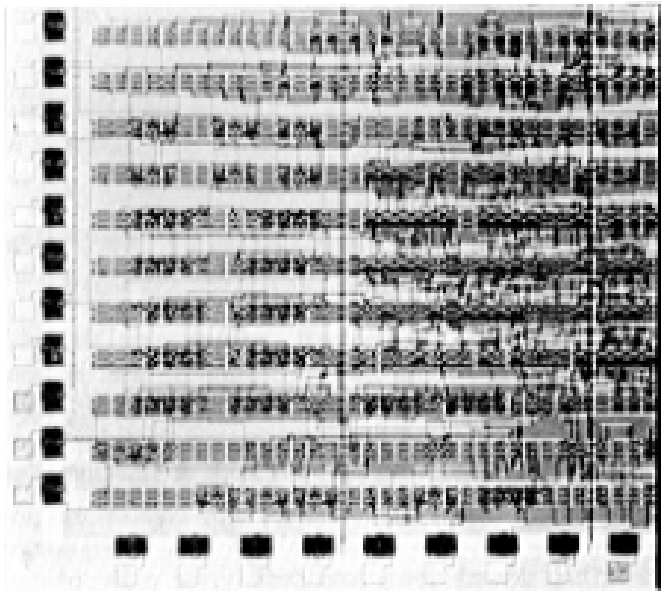
– Structure of a Gate Array

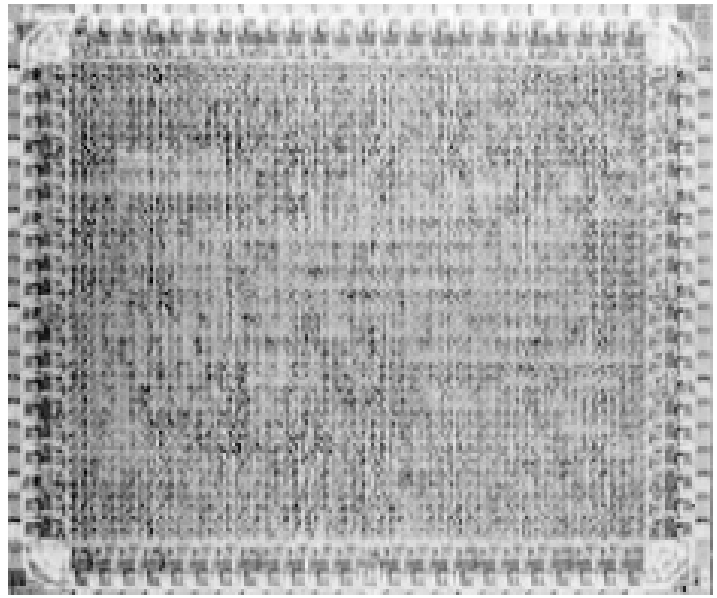






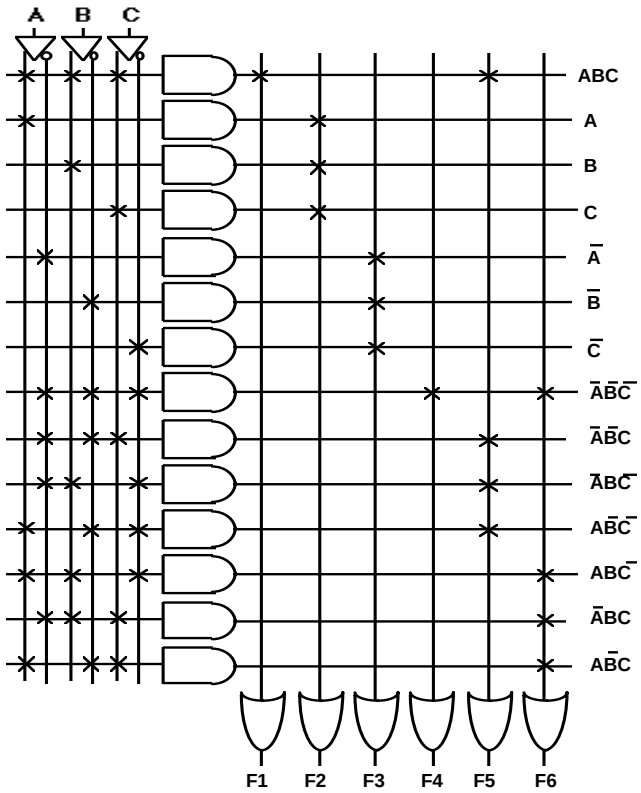
– Gate Array and Sea of Gate

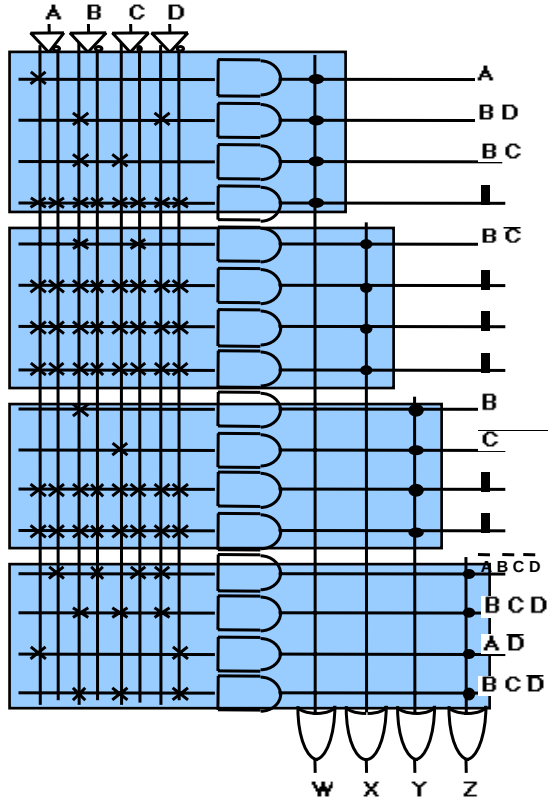




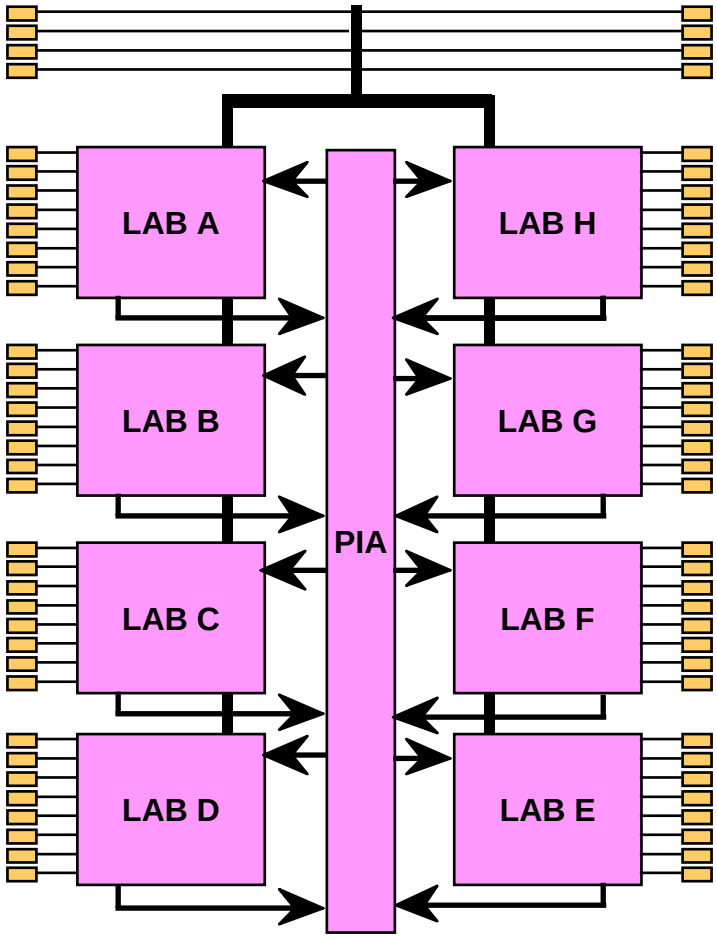
- **Field-Programmable Devices**
  - **Pre-laid out transistors as well as partial interconnects**
  - **Transistors and partial interconnects are connected electrically for desired functionality**
  - **No need of fabrication process in a foundry**
  - **Low manufacturing cost**
  - **Short manufacturing time (minutes)**
  - **Mass production does not help lower unit cost**
  - **Good for prototyping or pre-production**
  - **Large overhead in performance and area**

- **Taxonomy of Field-Programmable Devices**
  - **PLD (Programmable Logic Device):**
    - **PAL, FPLA, EPLD, EEPLD, ...**
  - **FPGA(Field-Programmable Gate Array):**
    - **fuse, anti-fuse, SRAM-based, EPROM-based, EEPROM-based, ...**
- **PLA vs. PAL**

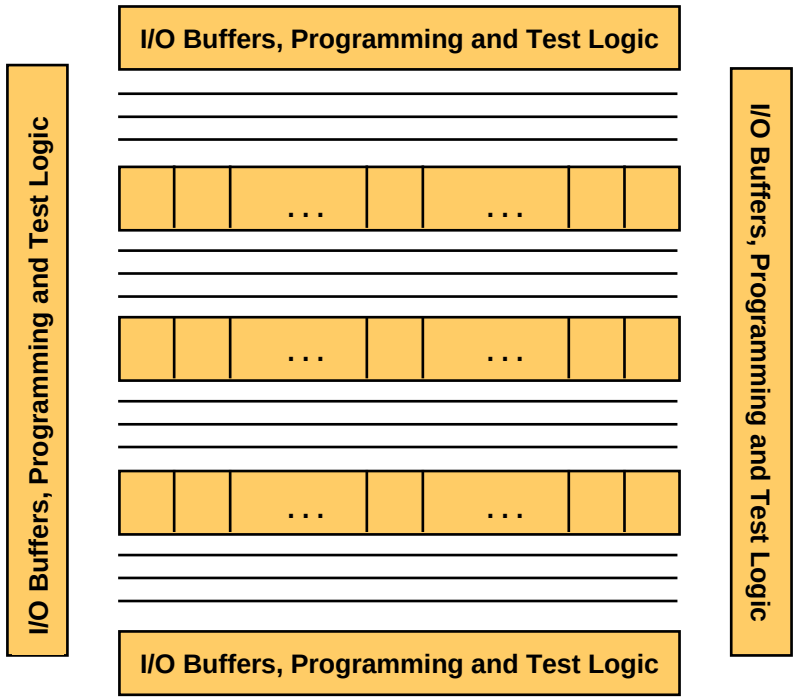


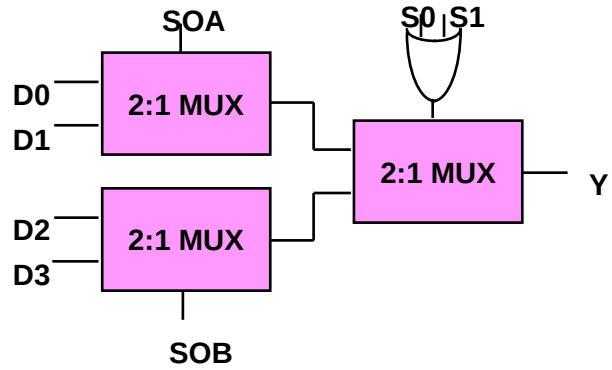


– **Altera Multiple Array Matrix (MAX)**

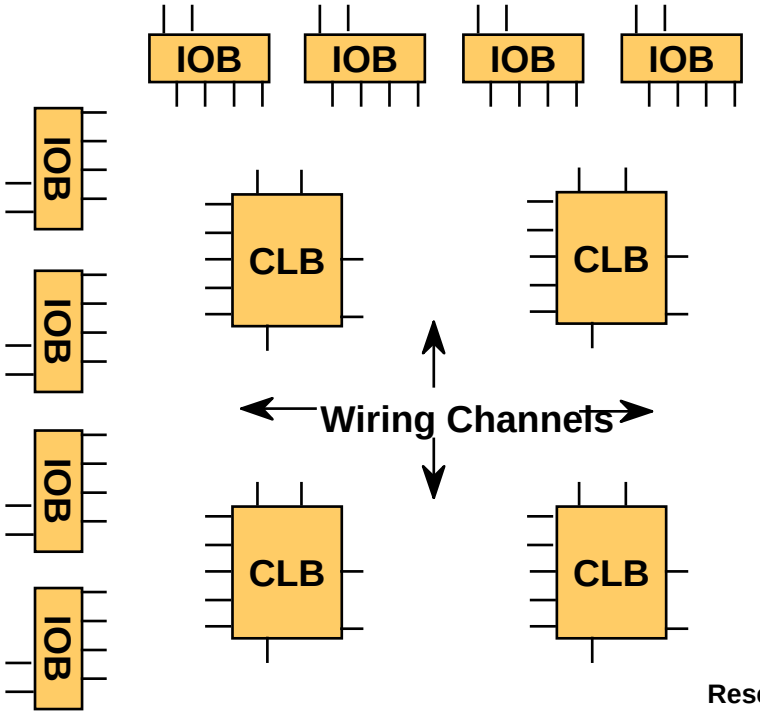


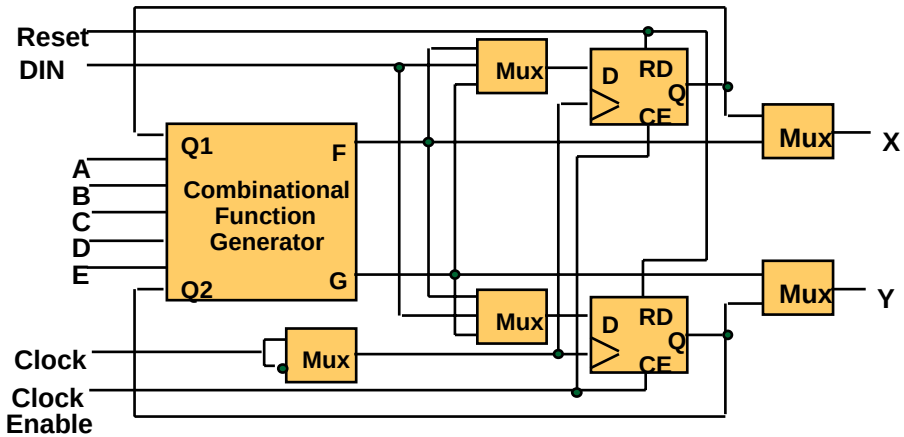
– Actel Programmable Gate Array





– Xilinx Logic Cell Array

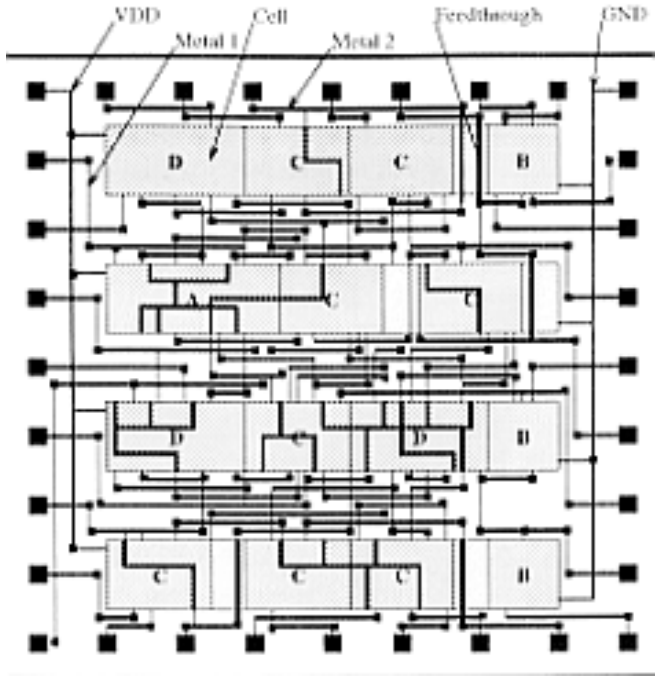


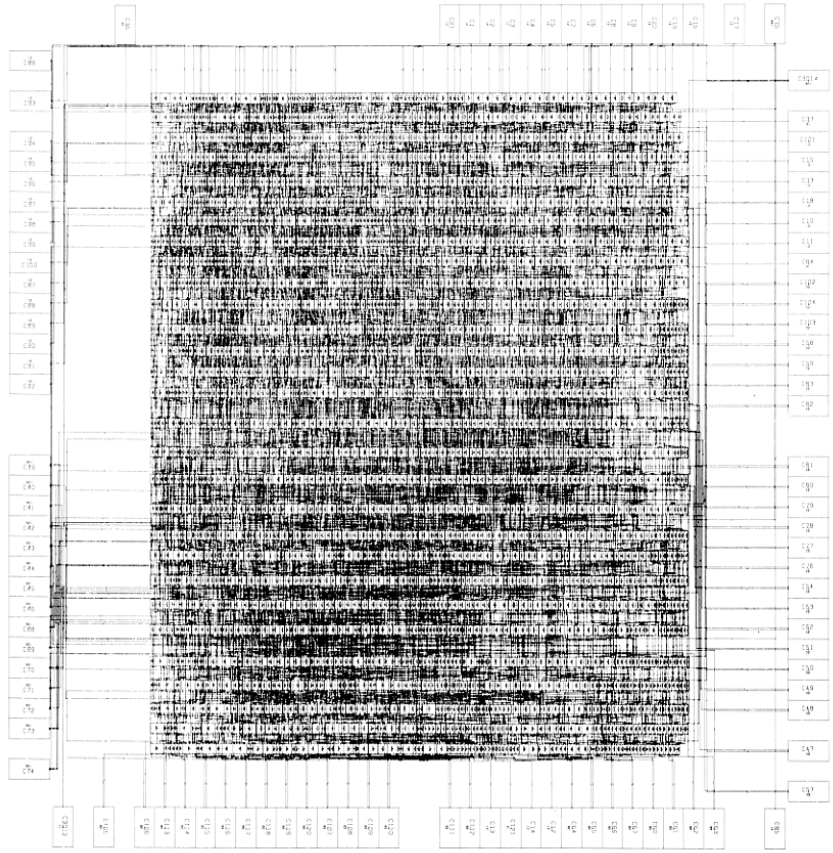


- **Full Custom Design**
  - **All transistors and the interconnects are drawn manually (with the help of a layout editor)**
  - **Can maximize performance with minimum area cost, if you are an expert**
  - **Good for a critical part of a design**
  - **Used for the design of DRAMs or general purpose microprocessors that are mass produced**
  - **Long design time (one or more years)**
  - **Requires experts in circuit design**
  - **Low level (circuit level, layout level, etc.) CAD tools are used**

- **Standard Cell**
  - **Various useful circuits (cells) are pre-designed conforming to a given rule (fixed interval between Vdd and Gnd) and stored in a library for reuse. --> standard cell library**
  - **Designers take cells from the library and connect them.**
  - **Cells are placed in multiple rows.**
  - **Cells in the same row abut against each other such that Vdds and Gnds are connected**
  - **Signal lines run thru routing channels**
  - **Unlike gate arrays, the routing channel width can vary and the area can be used more efficiently.**
  - **Fast design using CAD tools**
  - **Performance and area cost may not be as good as other approaches.**

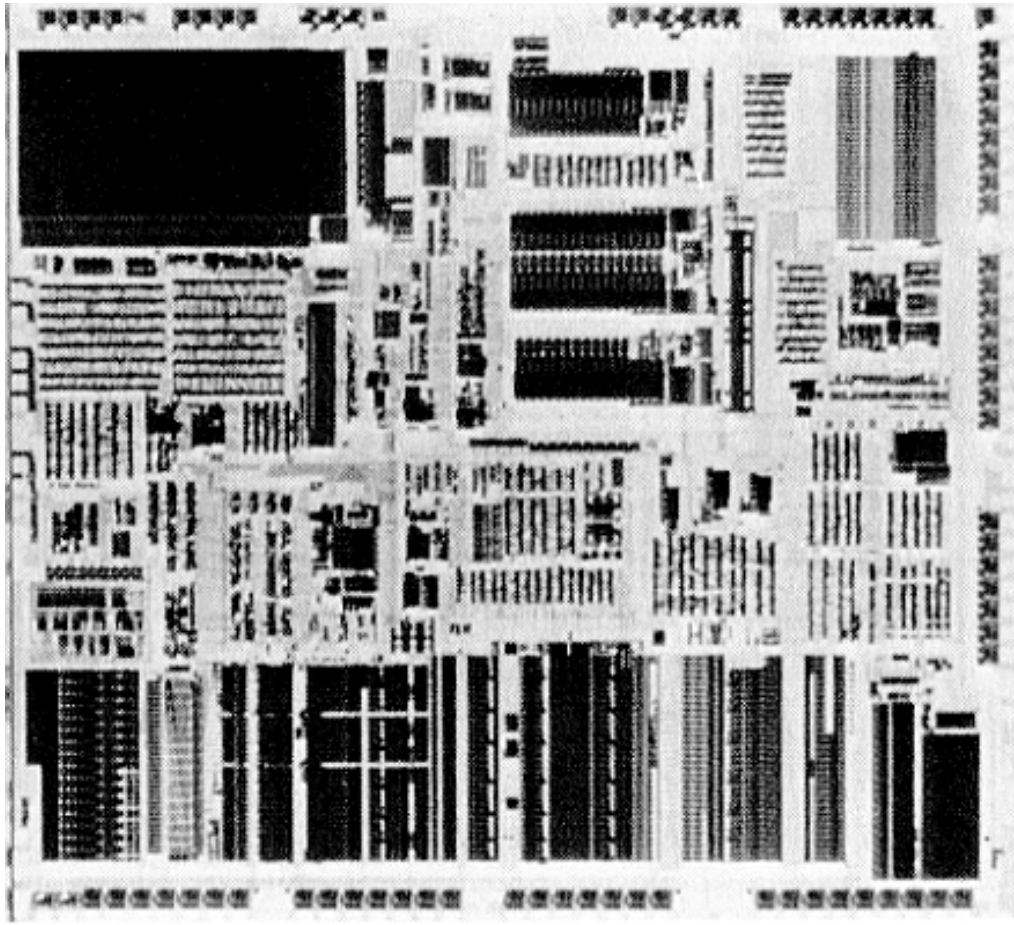
– Standard cell layout



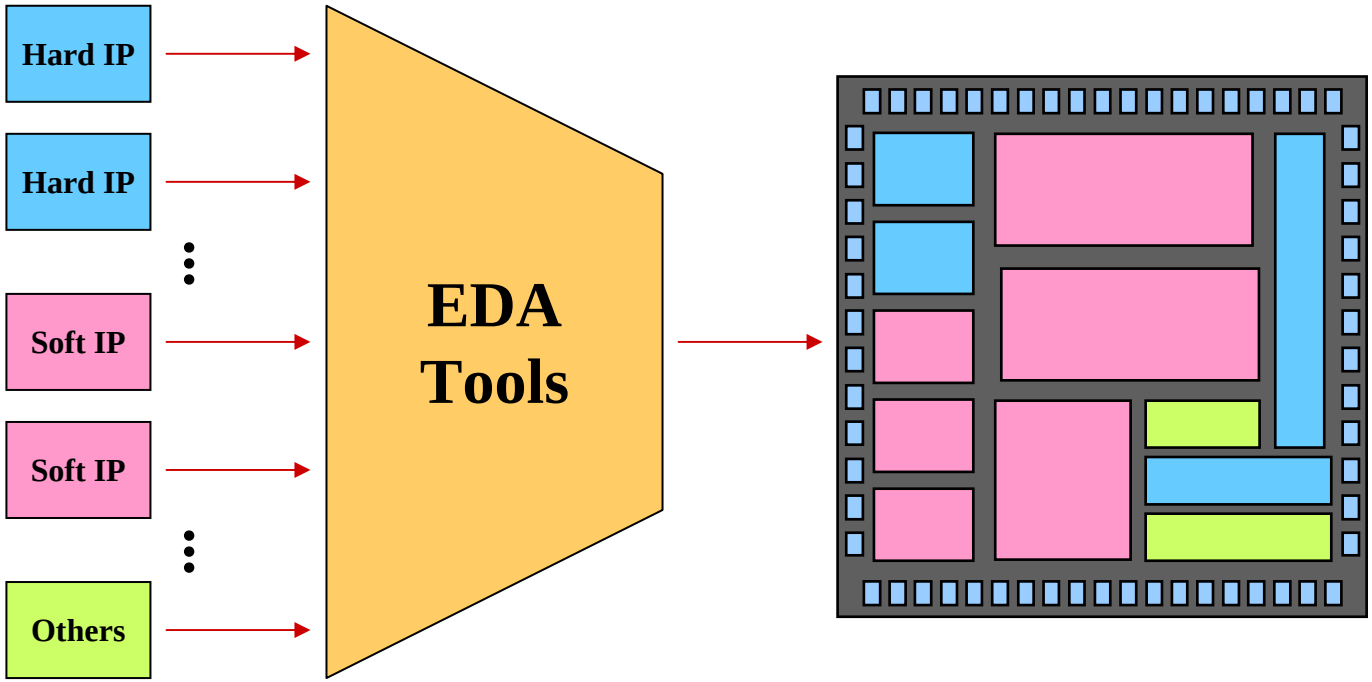


- **Macro-Cell**
  - **Random sized/shaped cells are taken from a cell library or automatically generated (module generation).**
  - **Used to design relatively big cells that may not be possible with standard cells**
  - **Can achieve better performance**
  - **Examples are RAM, ROM, PLA, etc.**
  - **Difficult placement and routing due to irregular size and/or shape**
- **These various styles can be mixed in a design.**

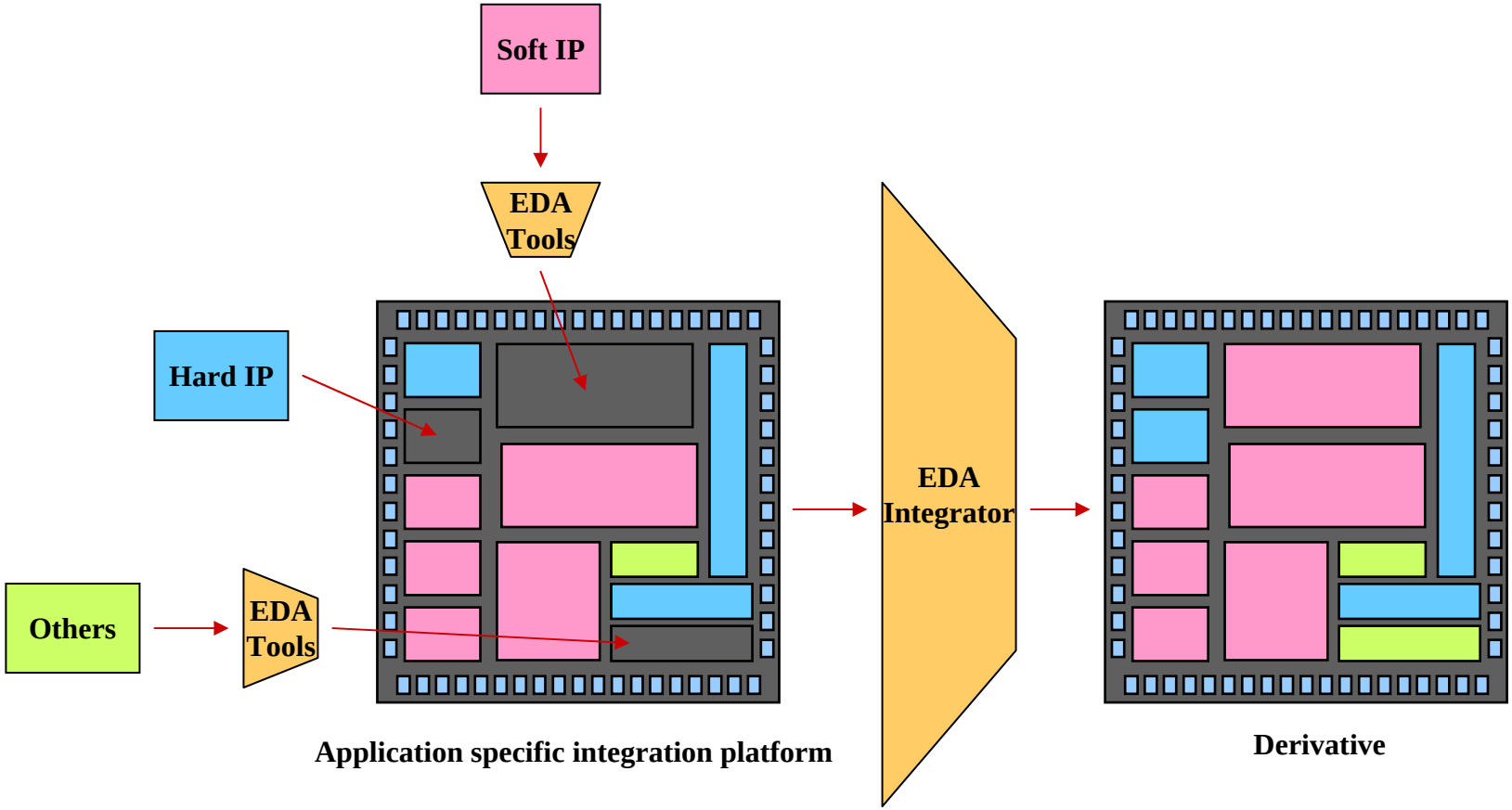
– **Example of a design with mixed styles**



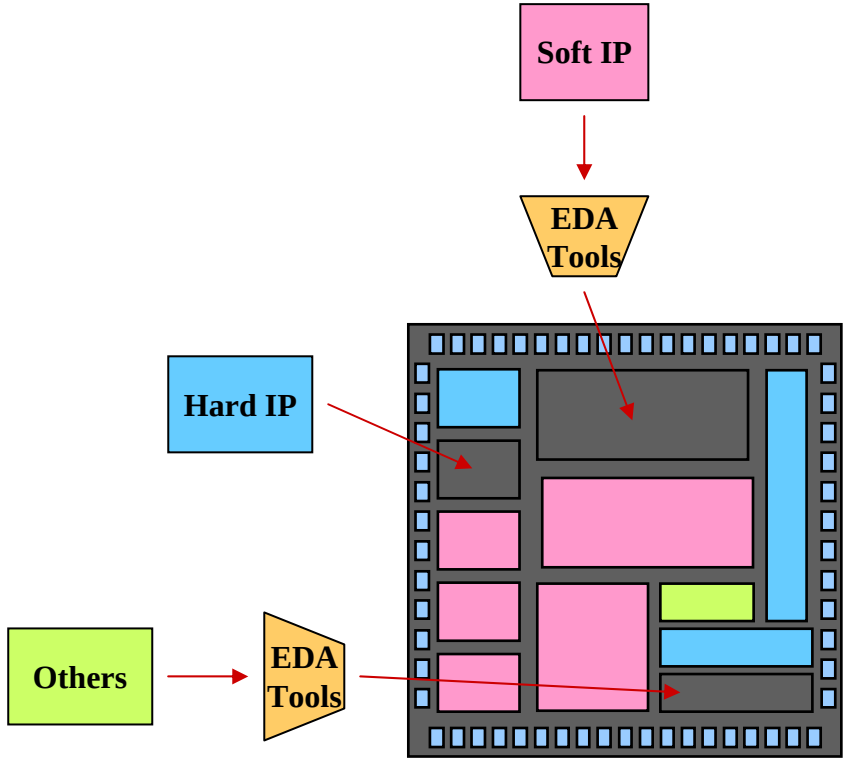
– IP-based design



– Platform-based design



– Plug and play



Application specific integration platform

– **VC interface**
  - **VSIA (Virtual Socket Interface Aliance)**
  - **OCP-IP (Open Core Protocol - International Partnership)**