Part II Electrical Properties of Materials

Chap. 7 Electrical Conduction in Metals and Alloys

Chap. 8 Semiconductors

Chap. 9 Electrical Properties of Polymers, Ceramics, Dielectrics, and Amorphous Materials

8.1 Band Structure

Hybridization of s- and p-states

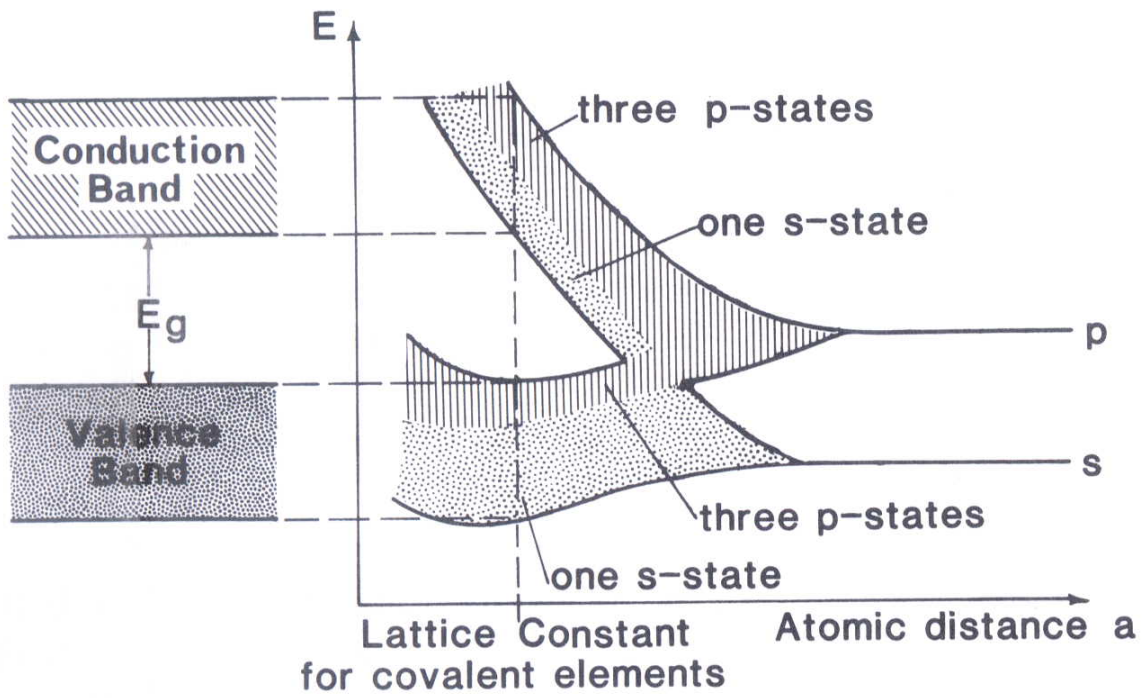


Figure 8.1. Sharp energy levels, widening into bands, and band overlapping with decreasing atomic distance for covalent elements. (Compare with Fig. 4.14.)

Two s+p bands, lower filled
higher empty for Ge, Si Group IV

8.1 Band Structure

Calculated band structure for Si

The valence band can accommodate $4N_a$ electrons: one lowest *s*-state and three *p*-states (4 *sp*- hybrids) and empty conduction band of 4 *sp*- hybrids

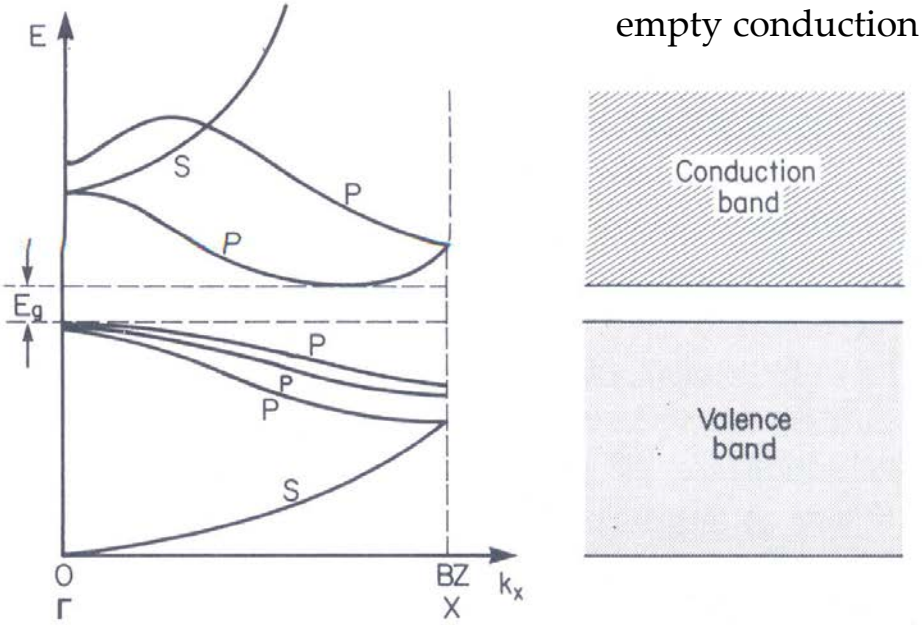


Figure 8.2. Schematic band structure of silicon in the k_x (or X) direction (plotted in the reduced zone scheme). The separation of the two highest *p*-states in the valence band is strongly exaggerated. Compare with the complete band structure of Fig. 5.23.

Eg (eV) at T=0 K
C : 5.48
Si : 1.17
Ge : 0.74
Sn(gray) : 0.08

The band gap energy (empirical equation)

$$E_{gT} = E_{g0} - \frac{\xi T^2}{T + \theta_D}, \qquad \xi \approx 5\times10^{-4}\,\text{eV/K} \qquad \theta_D, \text{DebyeTem.}$$

8.2 Intrinsic Semiconductors

At elevated temperatures, semiconductors become conducting.

The **Fermi Energy** in Semiconductors

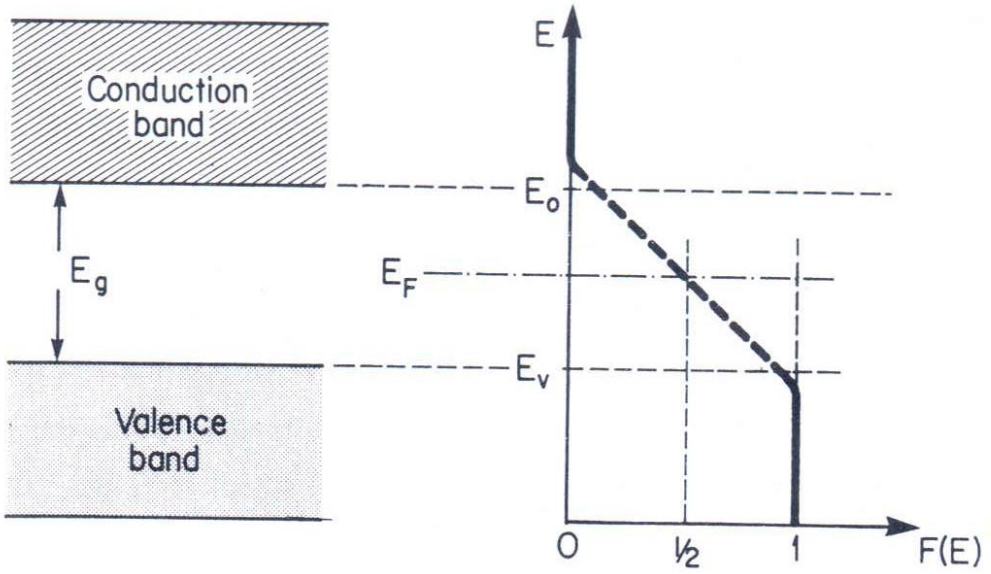


Figure 8.3. Schematic Fermi distribution function and Fermi energy for an intrinsic semiconductor for $T > 0$ K. The "smearing out" of the Fermi distribution function at E_0 and E_V is exaggerated. For reasons of convenience, the zero point of the energy scale is placed at the bottom of the conduction band.

For intrinsic semiconductors, $E_F = -E_g / 2$

For $T > 0$ K, the same amount of charge carriers can be found in the valence band as well as in the conduction band. → E_F should locate at halfway.

8.2 Intrinsic Semiconductors

Number of electrons in the conduction band

N^* : number of electrons having an energy equal to or smaller than a given energy E_n.

$dN^* = N(E)dE,$ for an energy interval between E and $E + dE$

$$N(E) = 2 \cdot Z(E) \cdot F(E) \qquad Z(E) = \frac{V}{4\pi^2}\left(\frac{2m}{\hbar^2}\right)^{3/2} E^{1/2}$$

$$F(E) = \frac{1}{\exp\left(\dfrac{E - E_F}{k_B T}\right) + 1} \approx \exp\left[-\left(\frac{E - E_F}{k_B T}\right)\right]$$

since $E - E_F \sim 0.5$eV and $k_B T \sim 0.025$eV at RT

$$N^* = \frac{V}{2\pi^2} \cdot \left(\frac{2m}{\hbar^2}\right)^{3/2} \int_0^\infty E^{1/2} \cdot \exp\left[-\left(\frac{E - E_F}{k_B T}\right)\right] dE$$

$$N^* = \frac{V}{2\pi^2} \cdot \left(\frac{2m}{\hbar^2}\right)^{3/2} \exp\left(\frac{E_F}{k_B T}\right) \int_0^\infty E^{1/2} \cdot \exp\left[-\left(\frac{E}{k_B T}\right)\right] dE.$$

8.2 Intrinsic Semiconductors

$$N^* = \frac{V}{2\pi^2}\left(\frac{2m}{\hbar^2}\right)^{3/2} \exp\left(\frac{E_F}{k_B T}\right)\frac{k_B T}{2}(\pi k_B T)^{1/2} = \frac{V}{4}\left(\frac{2mk_B T}{\pi\hbar^2}\right)^{3/2} \exp\left(\frac{E_F}{k_B T}\right).$$

Introducing $E_F = -E_g/2$ and effective mass ratio m^*_e/m_0, $N_e = N^*/V$

$$= \frac{V}{4}\left(\frac{2mk_B T}{\pi\hbar^2}\right)^{3/2} \exp\left(\frac{E_F}{k_B T}\right).$$

$$\therefore N_e = 4.84\times10^{15}\left(\frac{m_e^*}{m_0}\right)^{3/2} T^{3/2} \exp\left[-\left(\frac{E_g}{2k_B T}\right)\right]$$

Number of electrons in the conduction band per cm^3

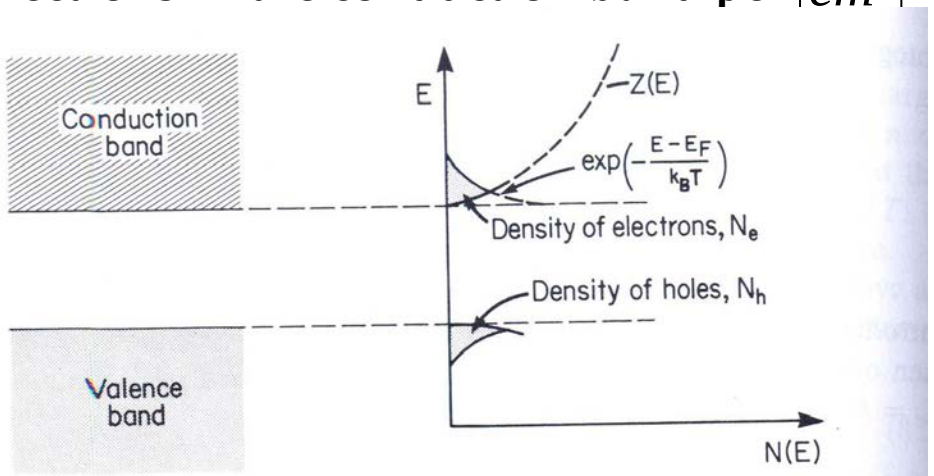


Figure 8.4. Density of electrons (N_e) and holes (N_h) for an intrinsic semiconductor

8.2 Intrinsic Semiconductors

Mobility $\mu = \dfrac{\upsilon}{\mathrm{E}},$

Ohm's law $j = \sigma \mathrm{E},$

$$j = N\upsilon e,$$

$$\sigma = N\frac{\upsilon}{\mathrm{E}}e = N\mu e.$$

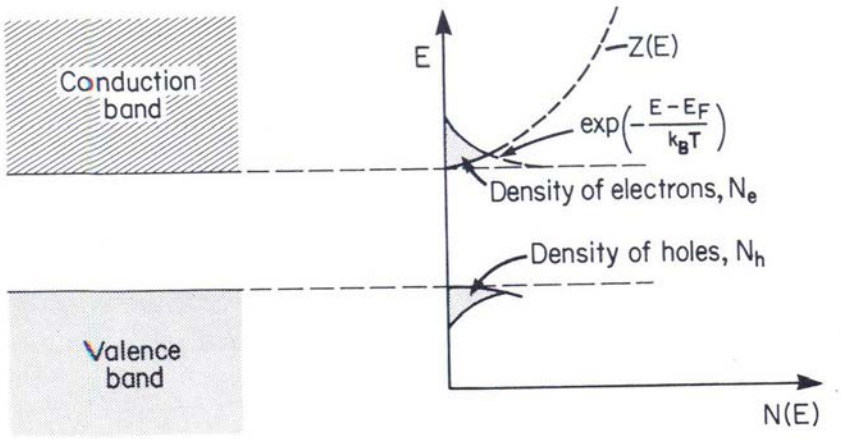


Figure 8.4. Density of electrons (N_e) and holes (N_h) for an intrinsic semiconductor

$$\sigma = N_e e\mu_e + N_h e\mu_h,$$

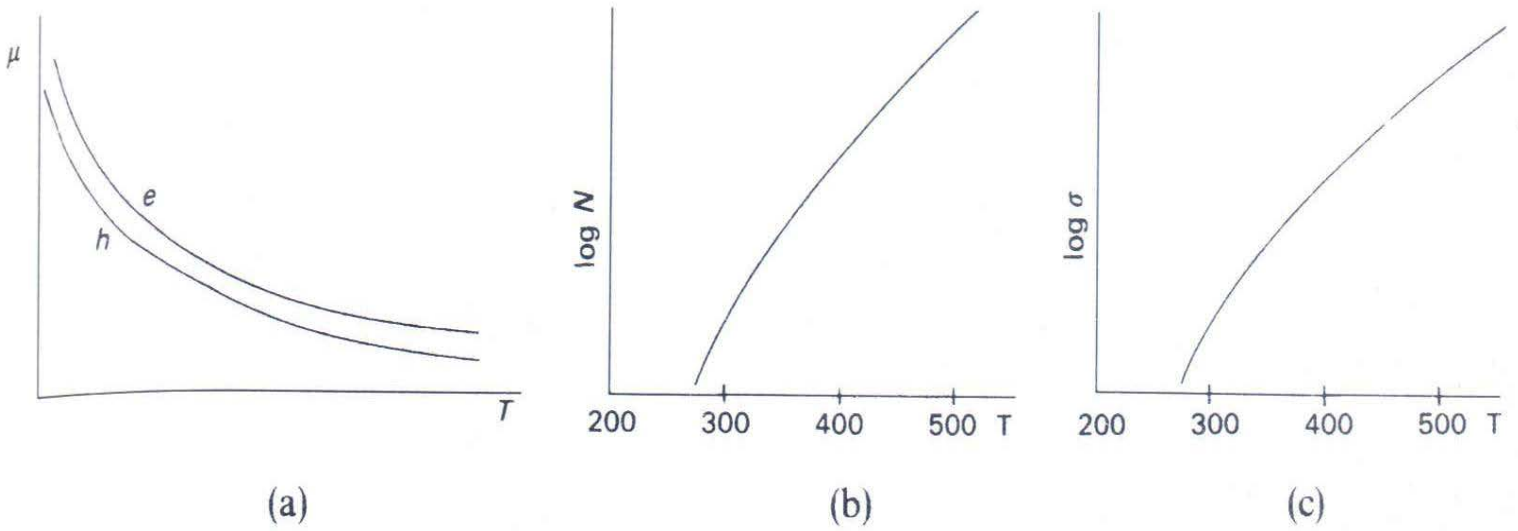
For intrinsic semiconductor, $N_e = N_h$

$$\sigma = 4.84\times10^{15}\left(\frac{m^*}{m_0}\right)^{3/2} T^{3/2} e(\mu_e + \mu_h)\exp\left[-\left(\frac{E_g}{2k_B T}\right)\right],$$

8.2 Intrinsic Semiconductors

$$\sigma = N_e e\mu_e + N_h e\mu_h,$$

$$\sigma = 4.84\times10^{15}\left(\frac{m^*}{m_0}\right)^{3/2} T^{3/2} e(\mu_e + \mu_h)\exp\left[-\left(\frac{E_g}{2k_B T}\right)\right],$$



Due to lattice vibration **Increasing the number of carriers**

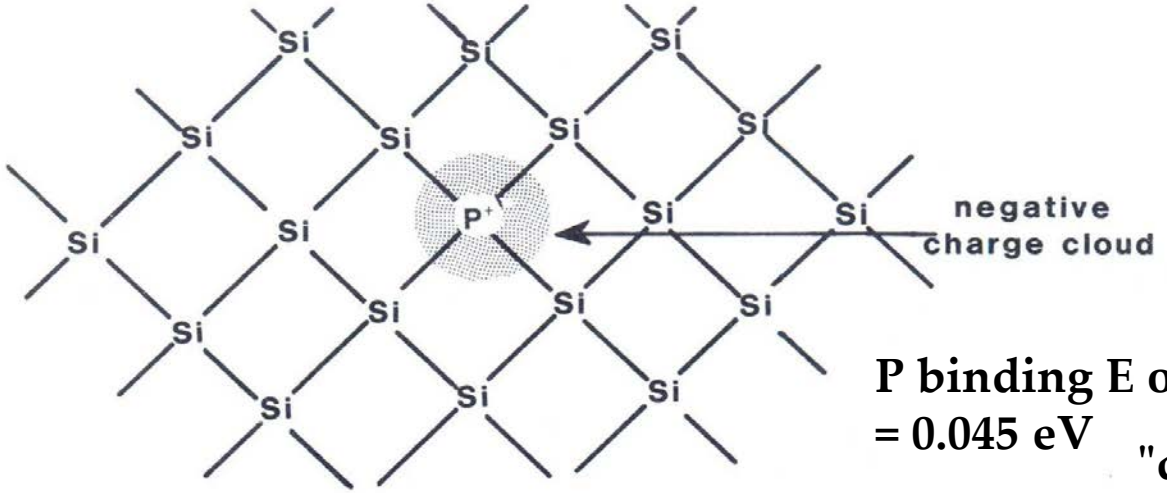
Figure 8.5. Schematic representation of the temperature dependence of (a) electron and hole mobilities, (b) number of carriers in an intrinsic semiconductor, and (c) conductivity for an intrinsic semiconductor. (T is given in Kelvin.)

8.3 Extrinsic Semiconductors

8.3.1 Donors and Acceptors

For intrinsic semiconductor, 10^9 electrons per cubic centimeter

Doping: adding small amounts of impurities (III or V) to intrinsic semiconductors
Dopant in a substitutional manner

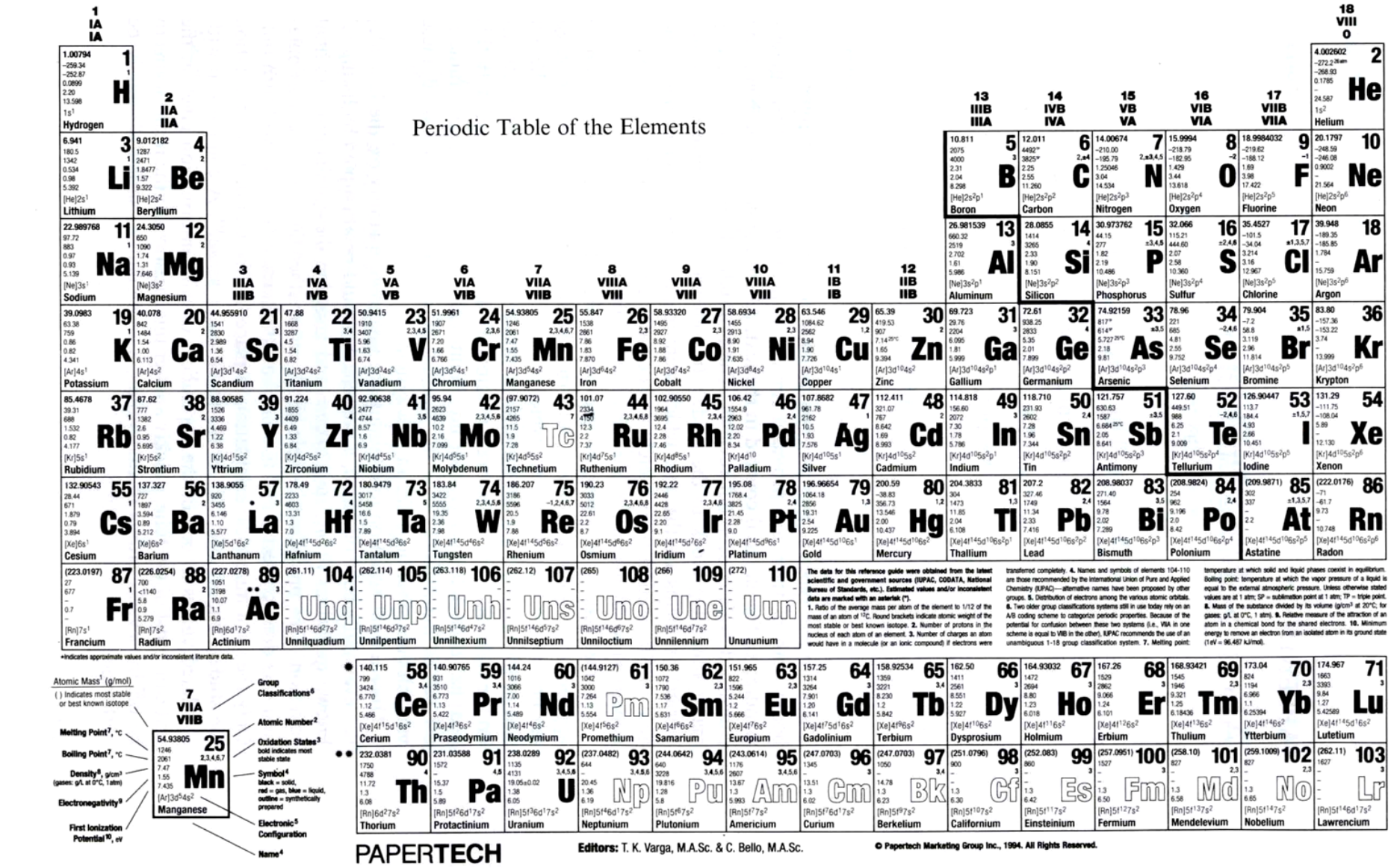


P binding E of the fifth electron = 0.045 eV

"donor electrons"

Figure 8.6. Two-dimensional representation of the silicon lattice. An impurity atom of group V of the periodic table (P) is shown to replace a silicon atom. The charge cloud around the phosphorus atom stems from the extra phosphorus electron. Each electron pair between two silicon atoms constitutes a covalent bond (electron sharing). The two electrons of such a pair are indistinguishable, but must have opposite spin to satisfy the Pauli principle.

8.3 Extrinsic Semiconductors



8.3 Extrinsic Semiconductors

8.3.2 Band Structure

Donor electrons
& thermally excited electrons

acceptor impurities
& thermally excited holes

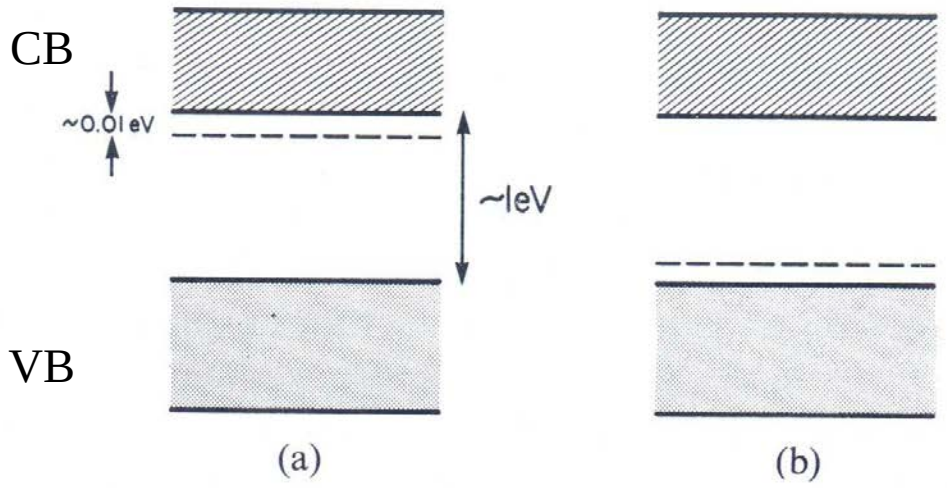


Figure 8.7. (a) Donor and (b) acceptor levels in extrinsic semiconductors.

13 IIIB IIIA	14 IVB IVA	15 VB VA
10.811 **5** 2075 4000 2.31 2.04 8.298 **B** $[He]2s^2p^1$ **Boron**	12.011 **6** 4492 3825 2.25 2.55 11.260 **C** $[He]2s^2p^2$ **Carbon**	14.00674 **7** −210.00 −195.79 1.25046 3.04 14.534 **N** $[He]2s^2p^3$ **Nitrogen**
26.981539 **13** 660.32 2519 2.702 1.61 5.986 **Al** $[Ne]3s^2p^1$ **Aluminum**	28.0855 **14** 1414 3265 2.33 1.90 8.151 **Si** $[Ne]3s^2p^2$ **Silicon**	30.973762 **15** 44.15 277 1.82 2.19 10.486 **P** $[Ne]3s^2p^3$ **Phosphorus**
69.723 **31** 29.76 2204 6.095 1.81 5.999 **Ga** $[Ar]3d^{10}4s^2p^1$ **Gallium**	72.61 **32** 938.25 2833 5.35 2.01 7.899 **Ge** $[Ar]3d^{10}4s^2p^2$ **Germanium**	74.92159 **33** 817 614 5.727 25°C 2.18 9.81 **As** $[Ar]3d^{10}4s^2p^3$ **Arsenic**
114.818 **49** 156.60 2072 7.30 1.78 5.786 **In** $[Kr]4d^{10}5s^2p^1$ **Indium**	118.710 **50** 231.93 2602 7.28 1.96 7.344 **Sn** $[Kr]4d^{10}5s^2p^2$ **Tin**	121.757 **51** 630.63 1587 6.684 25°C 2.05 8.641 **Sb** $[Kr]4d^{10}5s^2p^3$ **Antimony**
204.3833 **81** 304 1473 11.85 2.04 6.108 **Tl** $[Xe]4f^{14}5d^{10}6s^2p^1$ **Thallium**	207.2 **82** 327.46 1749 11.34 2.33 7.416 **Pb** $[Xe]4f^{14}5d^{10}6s^2p^2$ **Lead**	208.98037 **83** 271.40 1564 9.78 2.02 7.289 **Bi** $[Xe]4f^{14}5d^{10}6s^2p^3$ **Bismuth**

Impurity states; donor or acceptor levels

For Si or Ge smiconductors,

n-type, major carrier: electrons
donor impurities: P, As, Sb

p-type, major carrier: holes
acceptor impurities: B, Al, Ga, In

8.3.3 Temperature Dependence of the Number of Carriers

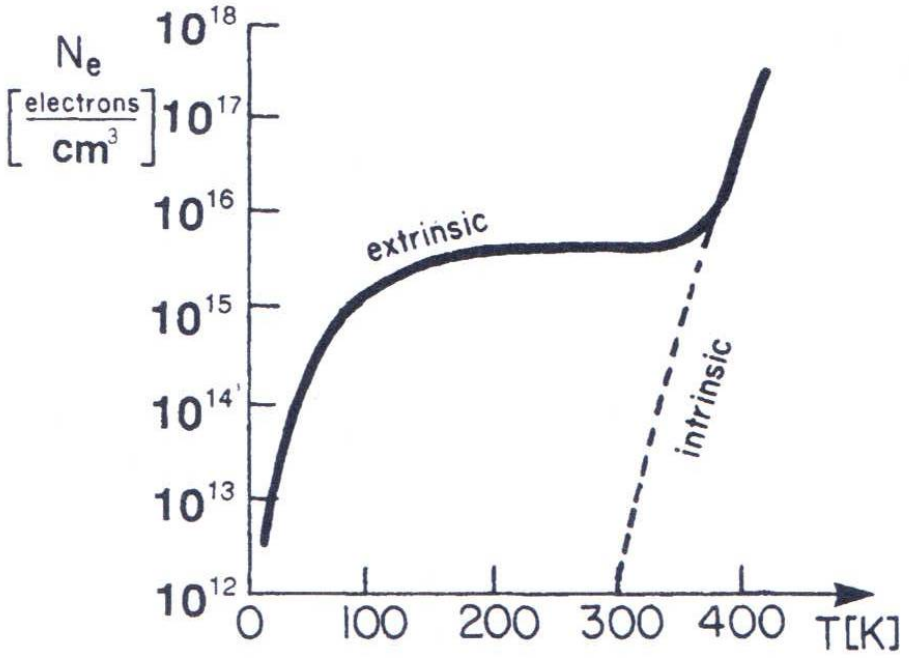


Figure 8.8. Schematic representation of the number of electrons per cubic centimeter in the conduction band versus temperature for an extrinsic semiconductor with low doping.

8.3 Extrinsic Semiconductors

8.3.4 Conductivity

$$\sigma = N_{de} e \mu_e ,$$

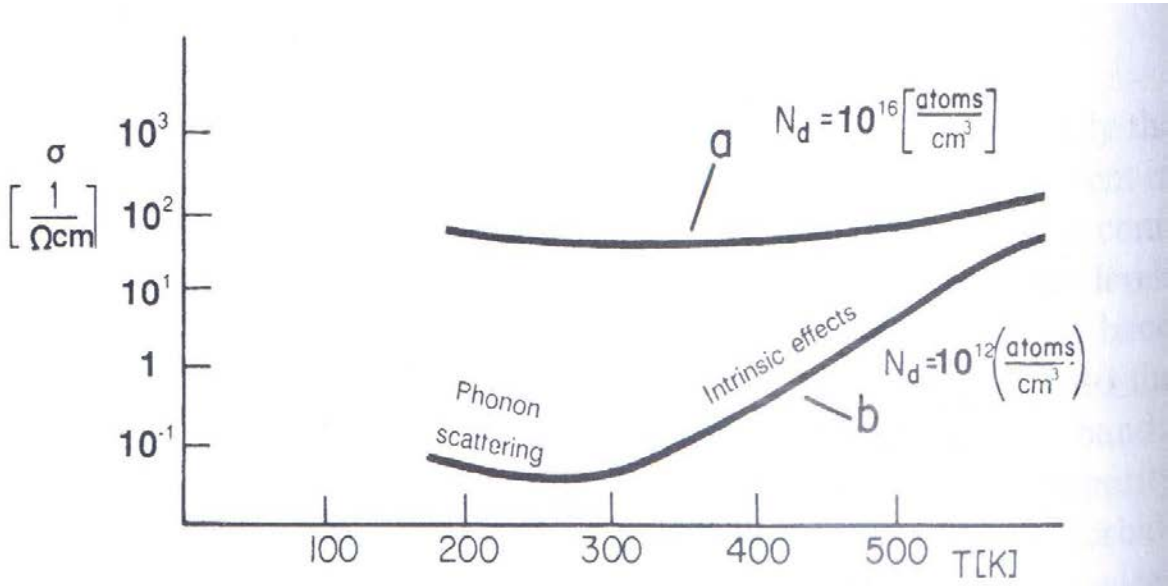


Figure 8.9. Conductivity of two extrinsic semiconductors, (a) high doping and (b) low doping. N_d = number of donor atoms per cubic centimeter.

- For low doping and at low temperature, the conductivity decreases with increasing temperature : lattice vibration → decrease mobility. At higher temperature: conductivity increase : intrinsic effects → increase number of carriers

- For high doping : temperature dependence on conductivity is less pronounced due to the already higher number of carrier.

8.3 Extrinsic Semiconductors

8.3.5 Fermi Energy

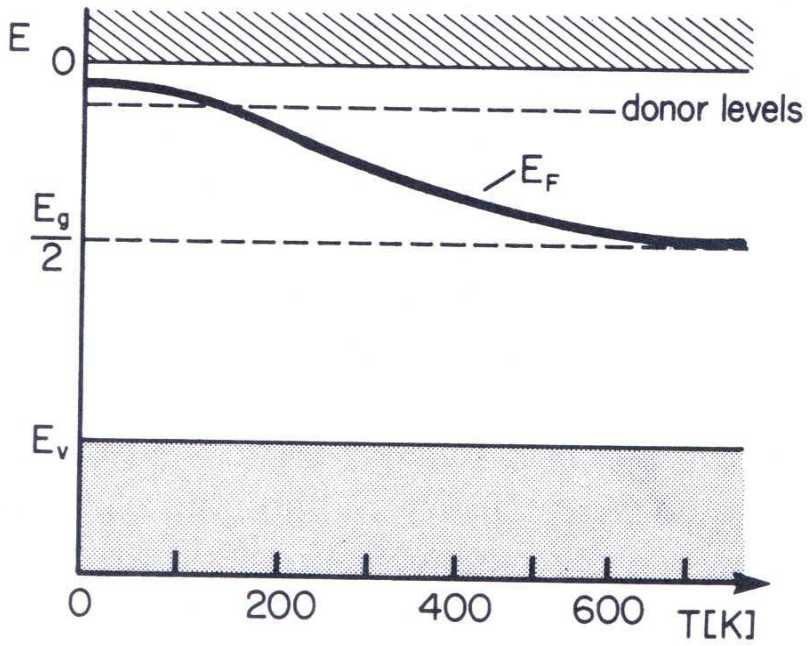


Figure 8.10. Fermi level of an *n*-type semiconductor as a function of temperature. $N_d \approx 10^{16}$ (atoms per cubic centimeter).

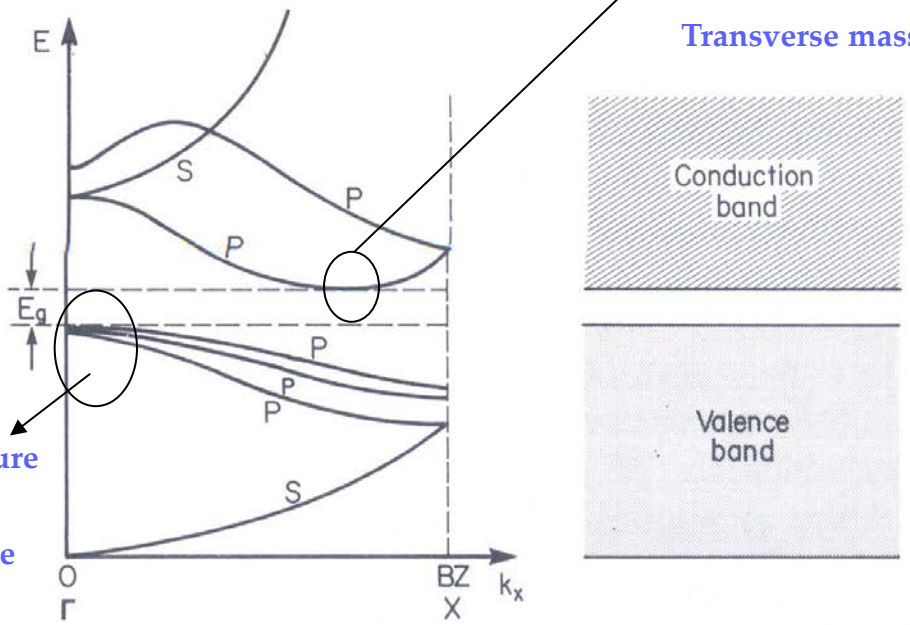
***n*-type semiconductor, $N_d = 10^{16}$ atoms per cubic centimeter**

8.4 Effective Mass

In 3-d, a spheroid shape:

Longitudinal mass m_l^*

Transverse mass m_t^*



2 heavy holes : smaller curvature

1 light hole : larger curvature

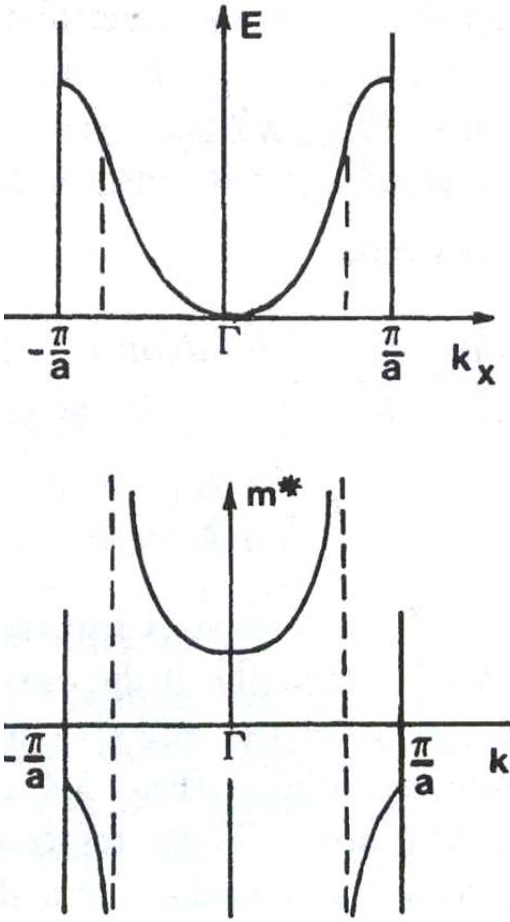


Figure 8.2. Schematic band structure of silicon in the k_x (or X) direction (plotted in the reduced zone scheme). The separation of the two highest p-states in the valence band is strongly exaggerated. Compare with the complete band structure of Fig. 5.23.

$$m^* = \hbar^2 \left(\frac{d^2 E}{dk^2} \right)^{-1} .$$

8.5 Hall Effect

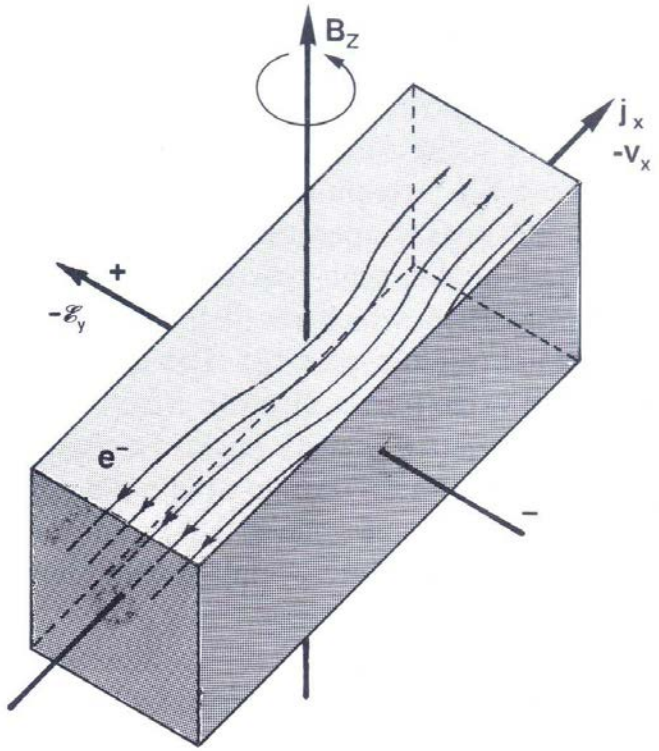


Figure 8.11. Schematic representation of the Hall effect in an *n*-type semiconductor (or a metal in which electrons are the predominant current carriers).

$$F_{\mathrm{H}} = -e\mathrm{E}_y$$

$$F_{\mathrm{L}} = \upsilon_x B_z e,$$

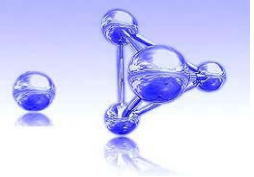
$$\mathrm{E}_y = \upsilon_x B_z. \quad \textit{Hall field}$$

$$j_x = -N\upsilon_x e$$

$$N = -\frac{j_x B_z}{e\mathrm{E}_y} = -\frac{I_x B_z L_y}{A_x e V_y}$$

$$\mathrm{E}_y = R_H j_x B_z$$

Hall constant $$R_H = -\frac{1}{Ne}$$



8.6 Compound Semiconductors

GaAs (III-V compound)

- Larger band gap compared to Si
- Larger electron mobility due to smaller electron effective mass (Fig 5.24)
- Direct band gap (chap 12): optical properties

Applications

- High-frequency devices
- Laser / light-emitting diodes (LED)

8.6 Compound Semiconductors

Other compound semiconductors

(applications: optoelectronic devices)

Group III-V elements

- GaP, GaN, InP, InAs, InSb, AlSb

Group II-VI elements

- ZnO, ZnS, ZnSe, CdS, CdTe, HgS

Group IV-VI

- PbS, PbSe, and PbTe

Ternary or quaternary alloys

- $Al_xGa_{1-x}As$, $Al_xGa_{1-x}As_ySb_{1-y}$, $GaAs_{1-x}P_x$: LEDs
  $GaAs_{1-x}As$ also used in modulation-doped field-effect transistors (MODFET)

Silicon carbide: Group IV-IV

- Band gap 3eV, very high temperature(700^oC) device
- Emit light in the blue end of the visible spectrum

8.7 Semiconductor Devices

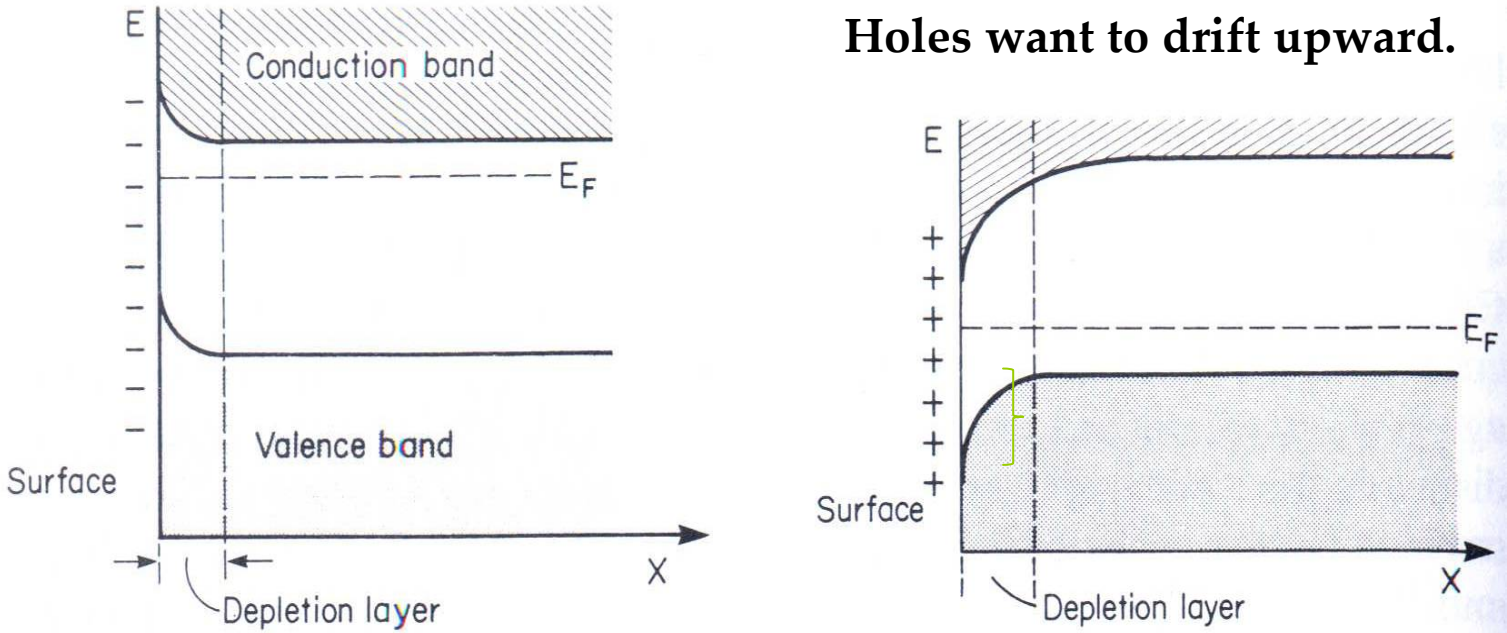
8.7.1 Metal-Semiconductor Contacts

Assuming the surfaces of an *n*- and *p*-type semiconductor have been somehow charged negatively and positively, respectively,

.

Electrons like to roll downhill.

Holes want to drift upward.



(Space charge region)

Figure 8.12. (a) Band diagram for an *n*-type semiconductor whose surface has been negatively charged. (b) Band diagram for a *p*-type semiconductor, the surface of which is positively charged. *X* is the distance from the surface.

8.7 Semiconductor Devices

8.7.2 Rectifying Contacts (Schottky Barrier Contacts)

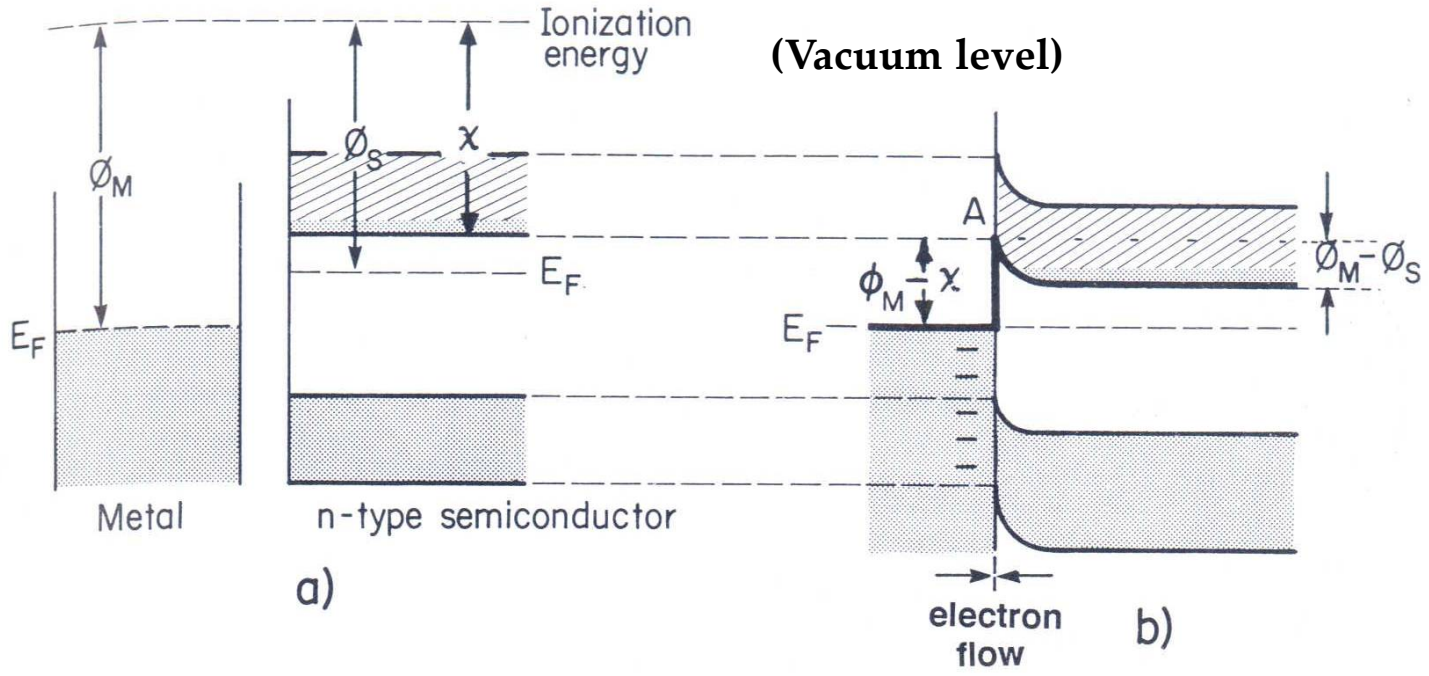


Figure 8.13. Energy bands for a metal and an *n*-type semiconductor (a) before and (b) after contact. $\phi_M > \phi_S$. The potential barrier is marked with heavy lines. χ is the *electron affinity*.

- **Diffusion current:** In equilibrium state, electrons from both sides cross the potential barrier.
- **Drift current:** The e-h pair, thermally created in or near the depletion layer, shows an immediate movement to lower energy state. The electron in the conduction band is swept down the barrier while the hle in the valence band is swept up the barrier.

8.7 Semiconductor Devices

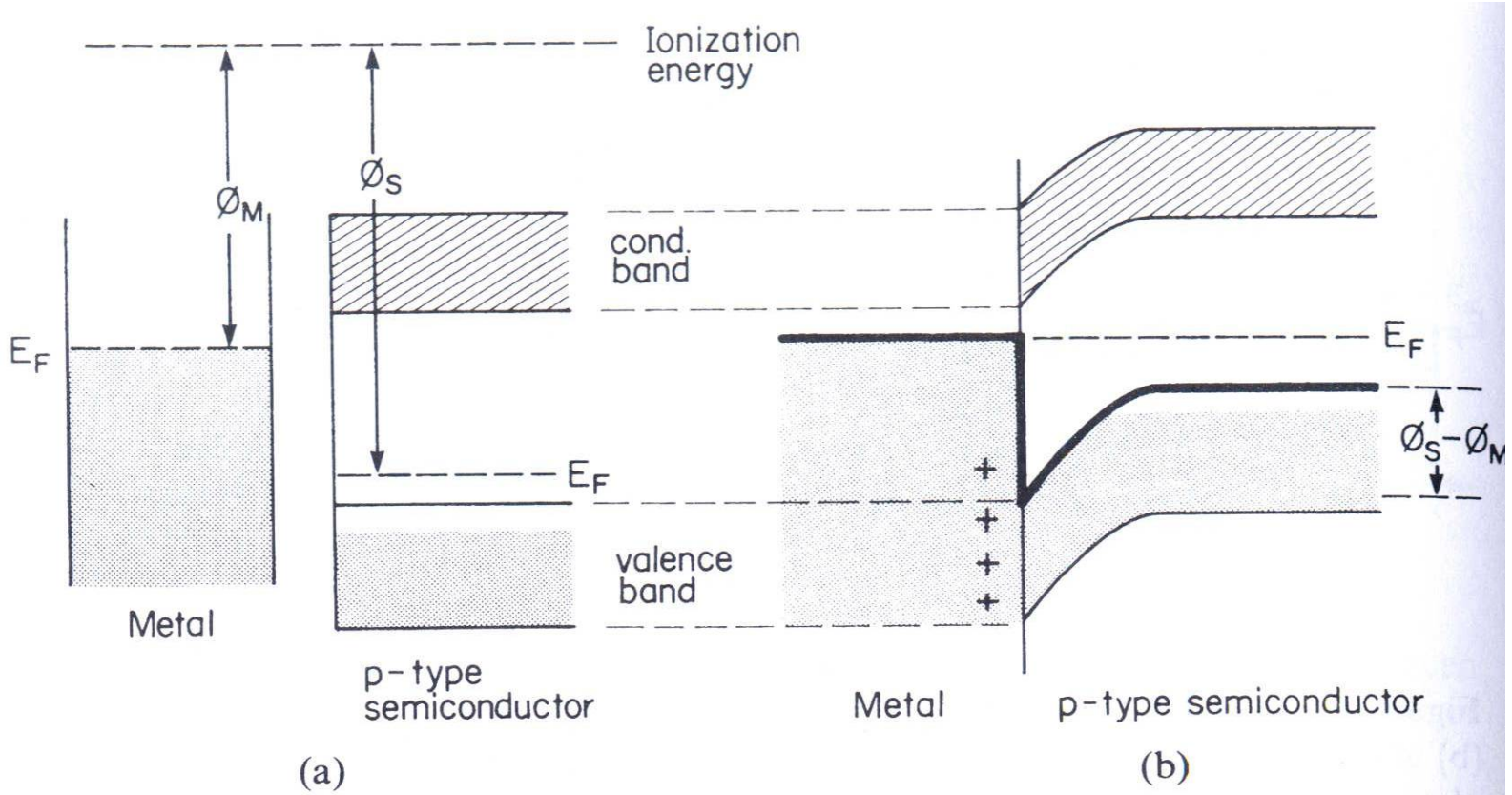


Figure 8.14. Energy bands for a metal and a *p*-type semiconductor (a) before and (b) after contact. $\phi_M < \phi_S$.

8.7 Semiconductor Devices

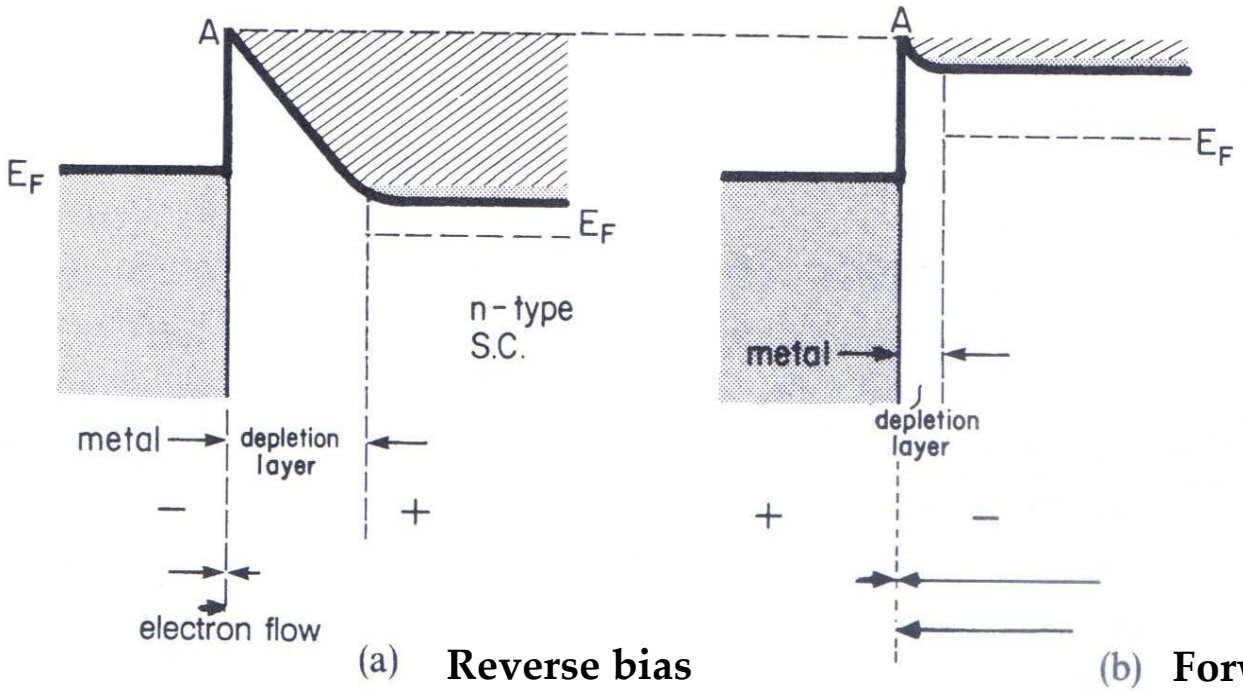


Figure 8.15. Metal–semiconductor contact with two polarities: (a) reverse bias and (b) forward bias. The number of electrons that flow in both directions and the net current is indicated by the length of the arrows. The potential barriers are marked by heavy lines.

8.7 Semiconductor Devices

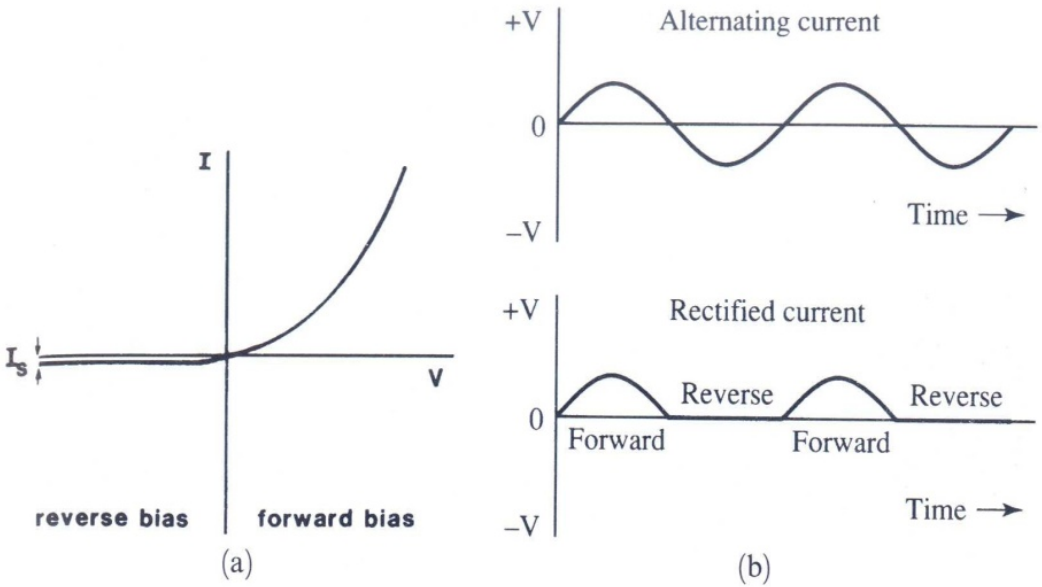
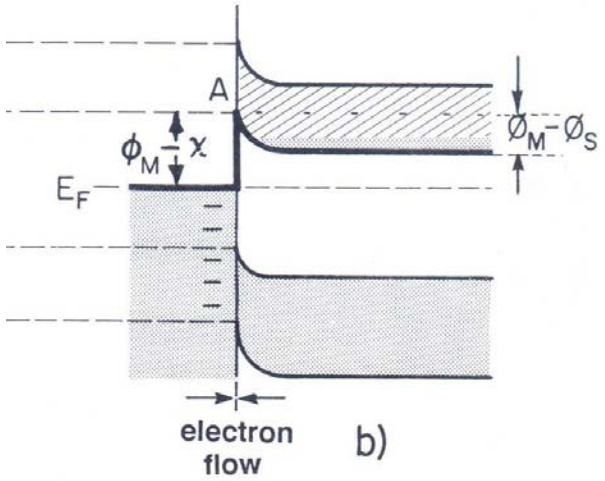


Figure 8.16. (a) Characteristic of a rectifier. The reverse current is grossly exaggerated! (b) Voltage versus time curves to demonstrate the behavior of an alternating current and a current for which the negative voltage has been eliminated.

참고) **Figure 8.13**



$$I_{MS} = ACT^2 \exp\left[-\left(\frac{\phi_M - \chi}{k_B T}\right)\right], \quad I_{SM} = ACT^2 \exp\left[-\left(\frac{\phi_M - \phi_S - eV}{k_B T}\right)\right],$$

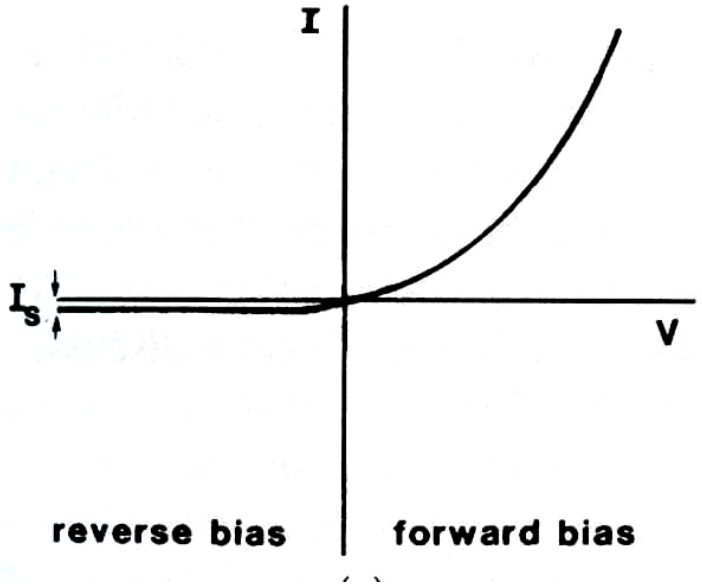
8.7 Semiconductor Devices

$\boxed{\phi_S \approx \chi}$ **for low enough temperatures**

$I_{net} = I_{SM} - I_{MS}$ **Consists of saturation current and a voltage-dependent term**

$$I_S = ACT^2 \exp\left[-\left(\frac{\phi_M - \phi_S}{k_B T}\right)\right]$$

$$I_{net} = I_S\left[\exp\left(\frac{eV}{k_B T}\right) - 1\right].$$



A few advantages of M/S rectifier over *p-n* diode
- No annihilation of electrons and holes
since a single charge carrier , electron or hole, is involved
- Better heat removal by the metal, suitable for high-power devices

8.7.3 Ohmic Contacts (Metallizations)

Ohmic contact: no barrier exists for the flow of electrons in either direction (Fig 8.17c)

$\phi_M < \phi_S$

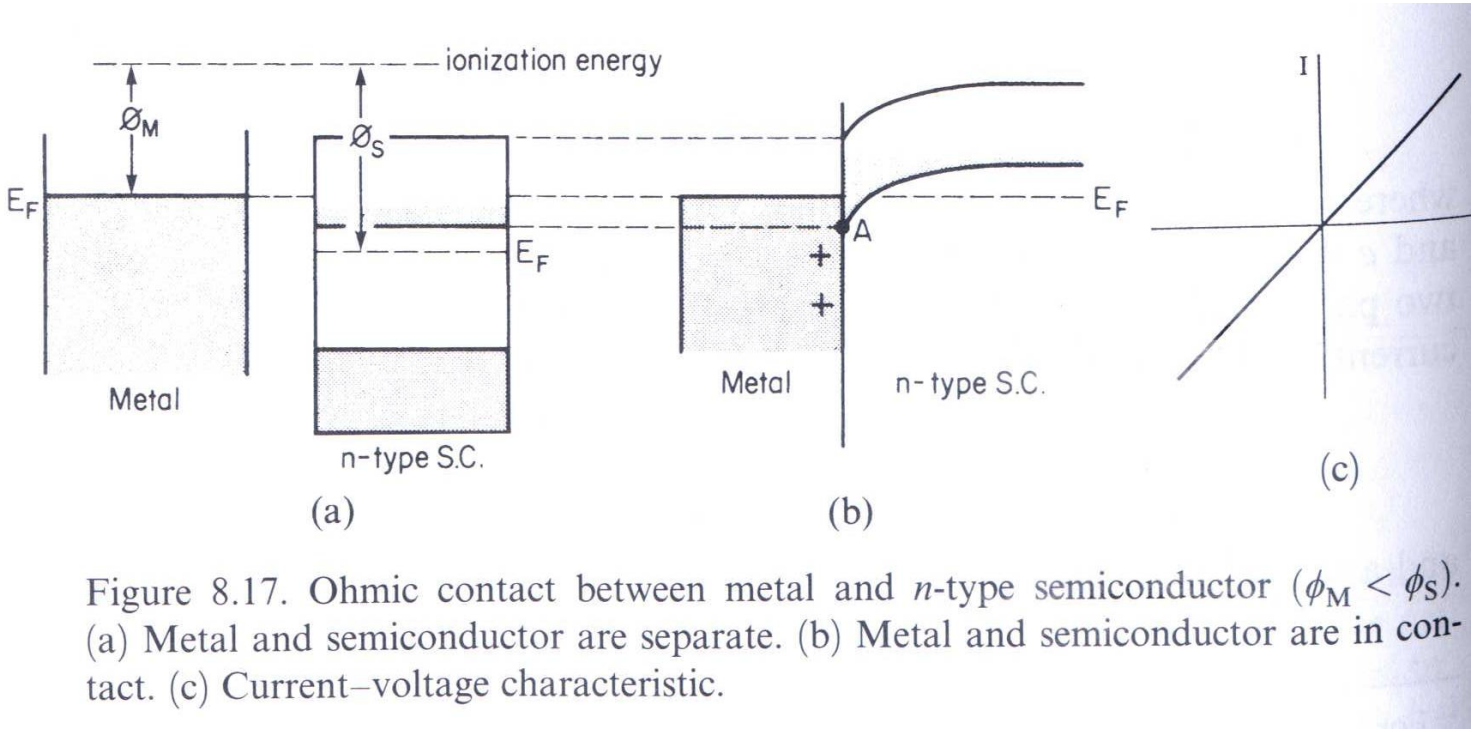


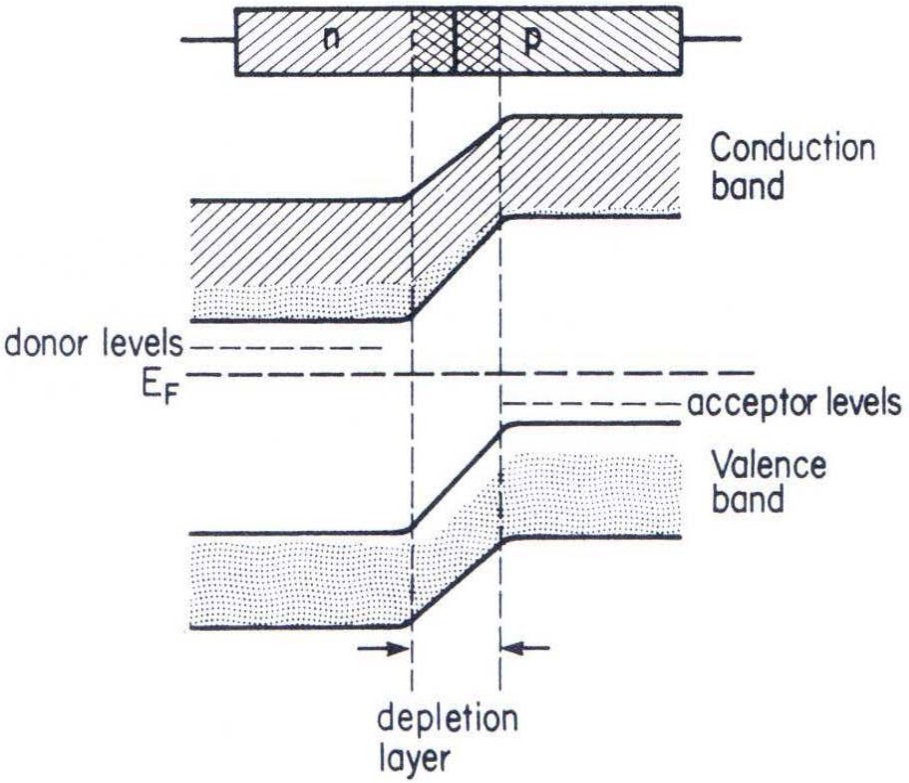
Figure 8.17. Ohmic contact between metal and *n*-type semiconductor ($\phi_M < \phi_S$). (a) Metal and semiconductor are separate. (b) Metal and semiconductor are in contact. (c) Current–voltage characteristic.

For the case of metal / n-type semiconductor contact, and $\phi_M < \phi_S$, electron flow from metal to semiconductor, charging metal positively. (cf, another case : metal / n-type semiconductor contact, and $\phi_M > \phi_S$)

The band of semiconductor bends "downward" and no barrier

8.7 Semiconductor Devices

8.7.4 *p-n* Rectifier (Diode)



After p-n contact : electron flow from higher level (*n*-type) "down" into p-type so that p-side is negatively charged.

Conduction band: electron in the p-region diffuse "down" into *n* -region, in equilibrium state the number of electrons crossing the junction in both directions is identical.

Figure 8.18. Schematic band diagram for a *p–n* junction (diode) in equilibrium.

8.7 Semiconductor Devices

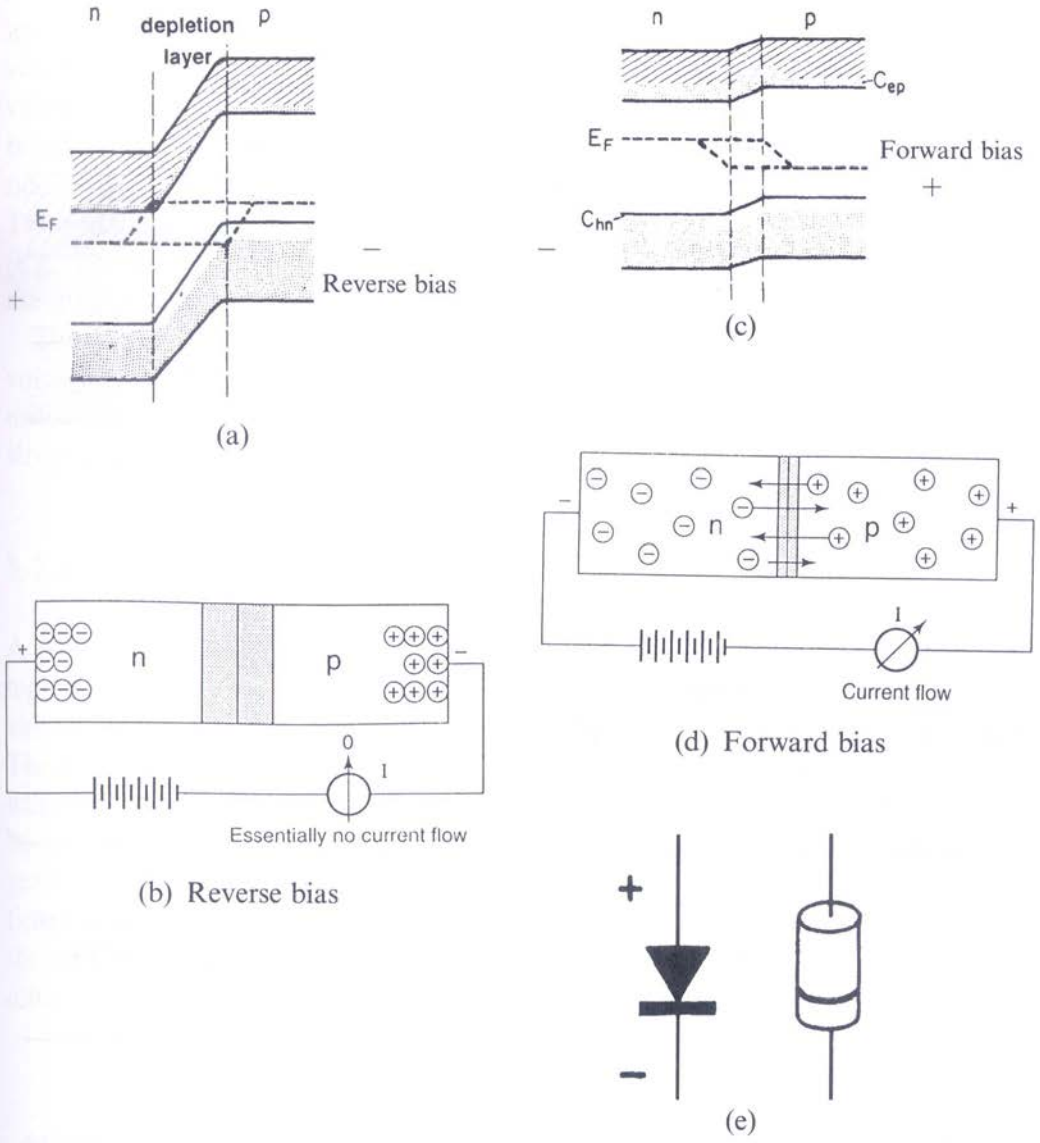


Figure 8.19. (a) + (b) Reverse and (c) + (d) forward biasing of a *p–n* junction (diode). (e) Symbol of a *p–n* rectifier in a circuit and designation of polarity in an actual rectifier.

Ideal diode law:

$$I_S = Ae\left(\frac{C_{ep}D_{ep}}{L_{ep}} + \frac{C_{hn}D_{hn}}{L_{hn}}\right)$$

C_{hn}: concentration of holes in the *n*-region,

C_{ep} : concentration of electrons in the *p*-region,

D: diffusion constant, *L*: diffusion length

Einstein relation:

$$D_{ep} = \frac{\mu_{ep} k_B T}{e}$$

The minority carrier diffusion length

$$L_{ep} = \sqrt{D_{ep} \cdot \tau_{ep}},$$

8.7 Semiconductor Devices

8.7.5 Zener Diode

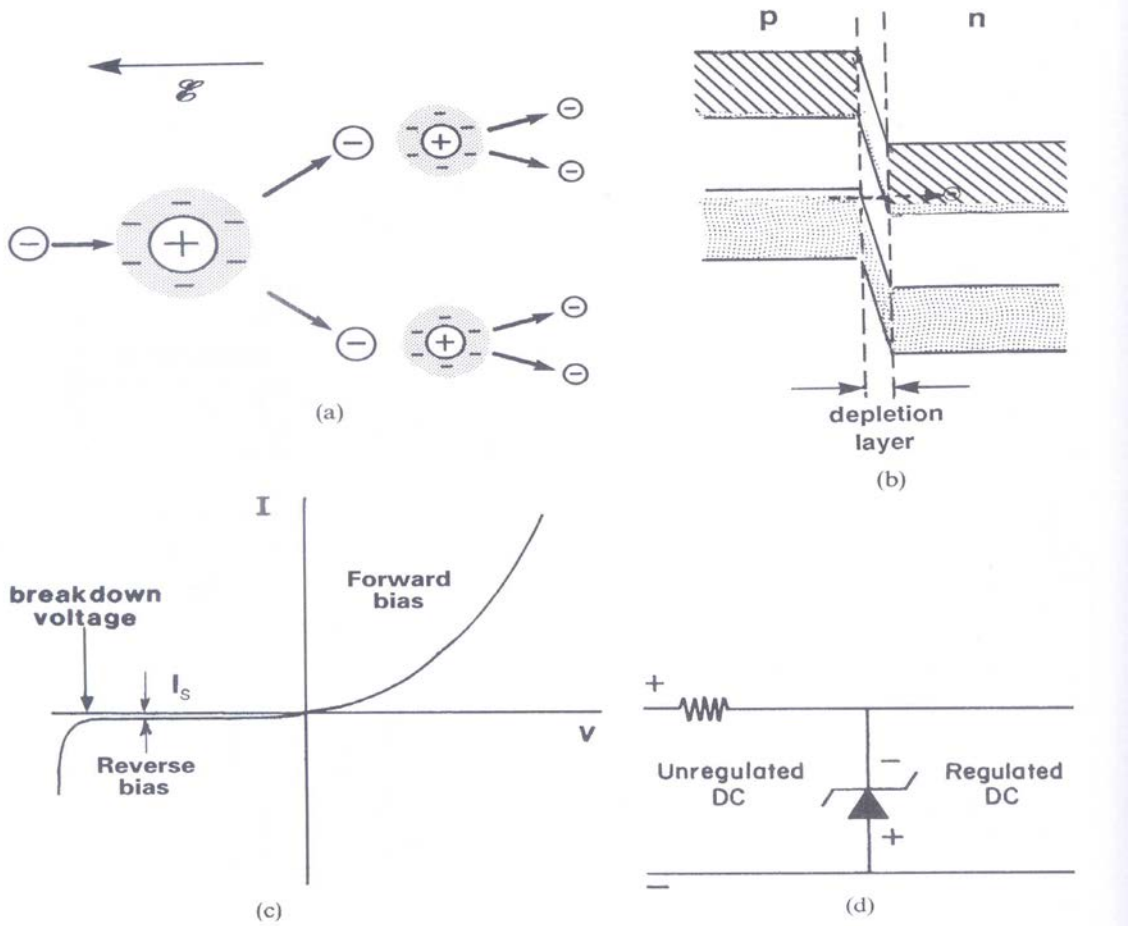


Figure 8.20. (a) Electron avalanche created at breakdown voltage. (b) Tunneling (Zener breakdown). (c) Voltage–current characteristic of a p–n diode exhibiting a breakdown voltage at a large reverse voltage. As in Fig. 8.16(a), I_s is shown grossly exaggerated. (d) Zener diode in a circuit for voltage regulation.

- **Breakdown:** when the reverse voltage is increased above a critical value, high electric field causes some electrons to become accelerated with a velocity at which **impact ionization** occurs → **avalanching** process

- **Zener breakdown (Tunneling):** another breakdown process; when the doping is heavy and thus the barrier width becomes very thin (< 10nm), applying high enough reverse voltage causes the bands to shift to the degree that some electron in the valence band of *p*-side are apposite to empty states in the conduction band of *n*-side and these electron can tunnel through the depletion layer (Fig 8.20b) ; a circuit protection device (Fig 8.20d).

8.7 Semiconductor Devices

8.7.6 Solar Cell (Photodiode)

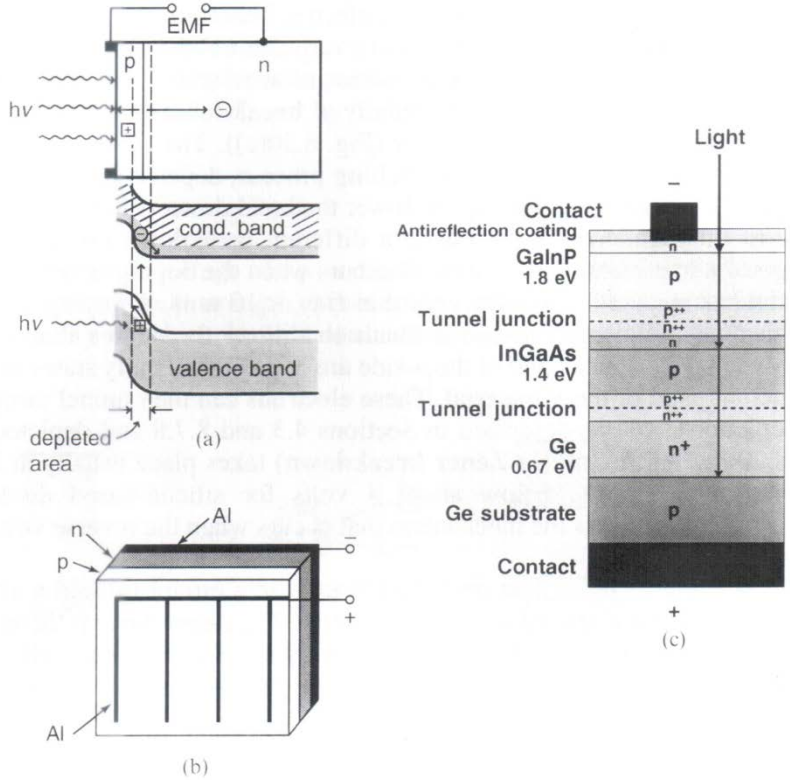


Figure 8.21. Solar cells; (a) Side view; the *p*-region is only about 1 μm thick. (b) Front view. (c) Simplified schematic of a multilayer solar cell.

a *p-n* junction diode

1. Light of high energy fall on or near the depleted area
2. Electrons are lifted from the valence band into the conduction band, leaving holes in the valence band.
3. The electron in the depleted area immediately "roll down" into the *n*-region, whereas the holes are swept into the *p*-region

8.7.6 Solar Cell (Photodiode)

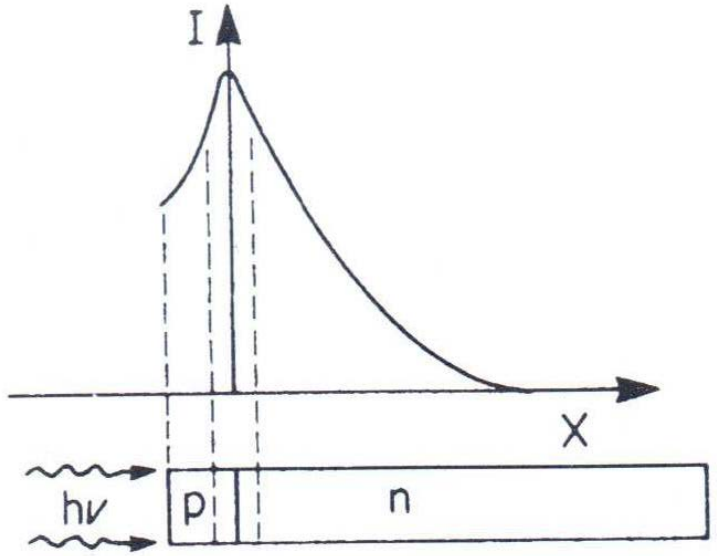


Figure 8.22. Schematic representation of the contribution of electrons and holes to the photocurrent (I) with respect to the distance x from the p–n junction.

Quantum Efficiency

$$\eta = 1 - \frac{\exp(-\alpha W)}{1+\alpha L},$$

W, L: the width and length of depletion region

α: a parameter that determines the degree of photon absorption by the electrons

8.7.7 Avalanche Photodiode

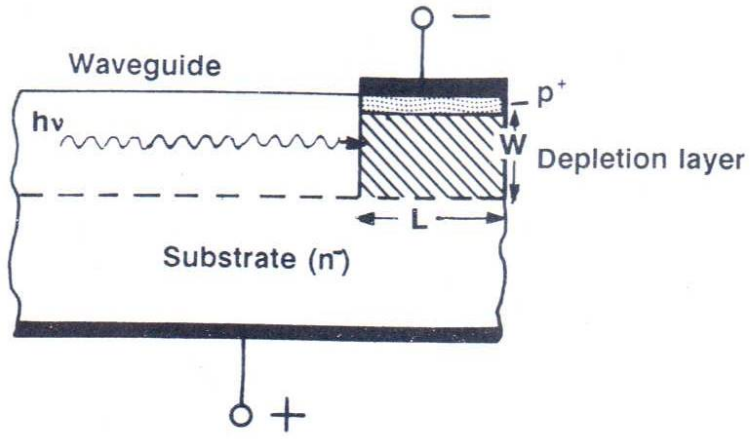
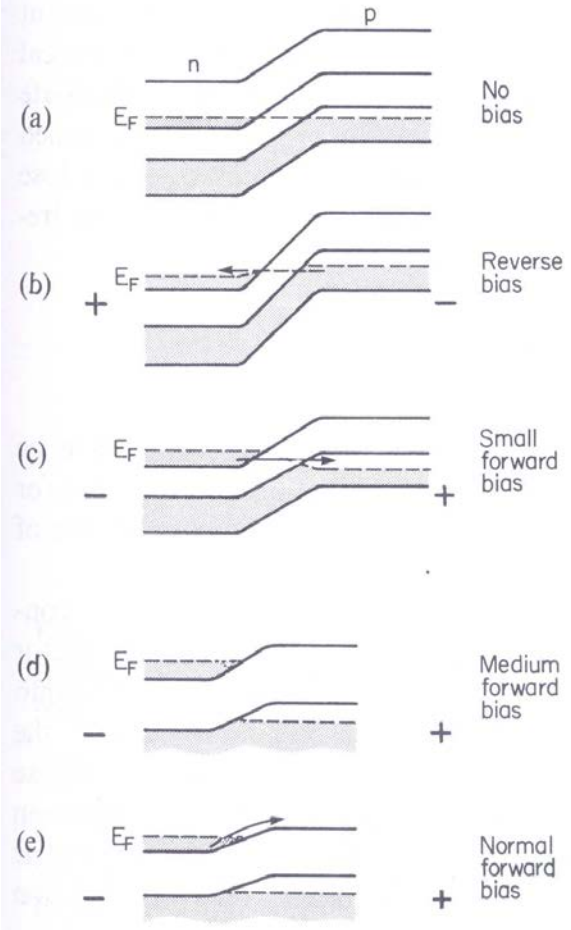


Figure 8.23. Schematic of a transverse-type photodiode that is connected to a light-carrying medium such as an optical fiber or a waveguide ($L \approx 100\,\text{nm}$).

Operated in a high reverse bias mode, at near-breakdown voltage.
Suitable for low-light-level applications because of its high signal-to-noise ratio, and for very high frequencies.

8.7.8 Tunnel Diode



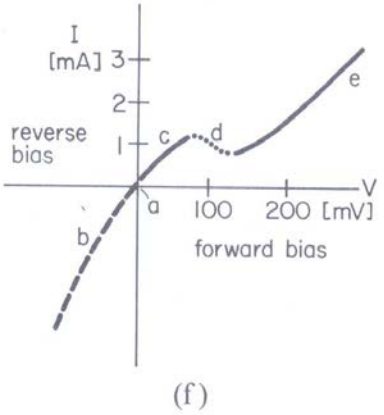


Figure 8.24. (a)–(e) Schematic energy band diagrams for highly doped *n*- and *p*-type semiconductors (tunnel diode). (a) No bias. (b) Reverse bias. (c) Small forward bias. (d) Medium forward bias. (e) "Normal" forward bias. (f) Voltage–current characteristic for a tunnel diode.

A *p*-*n* junction diode - depleted area is very narrow ; → heavy doping Fermi energy extends into the valence band of *p*-type semiconductor.

- The voltage is increase to 100mV (in Fig 8.24d), the potential barrier might be decreased so much that, opposite to the filled *n*-conduction state, no tunneling take place; current decreases with increasing forward voltage: "**negative current-voltage characteristic**": c-d region

8.7 Semiconductor Devices

8.7.9 Transistors

For signal amplification

Smaller and higher resistivity

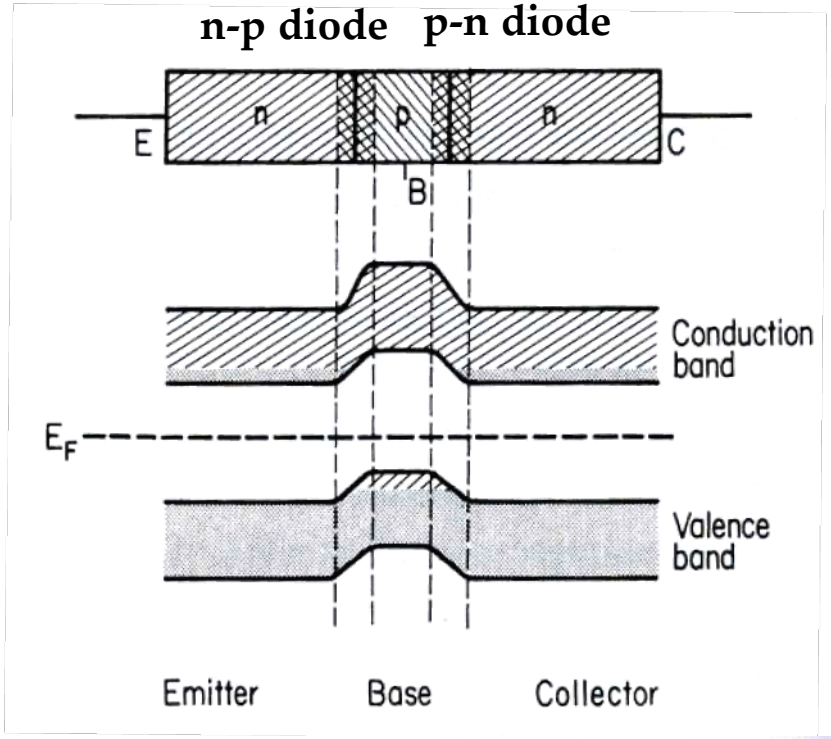


Figure 8.25. Schematic band diagram of an unbiased *n–p–n* bipolar junction transistor.

Unbiased n-p-n bipolar junction transistor

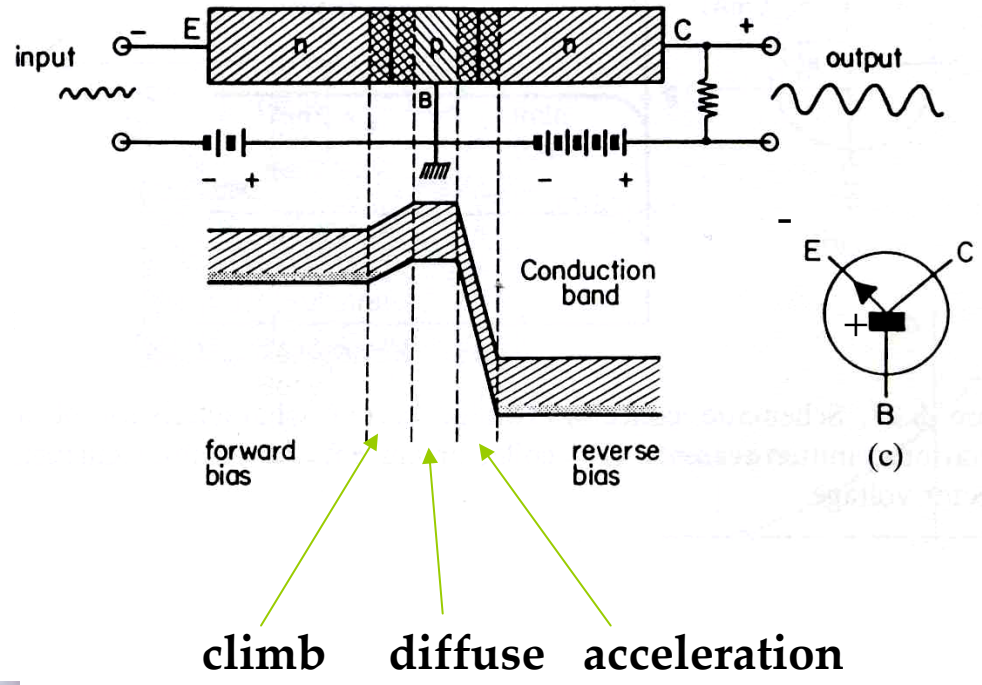


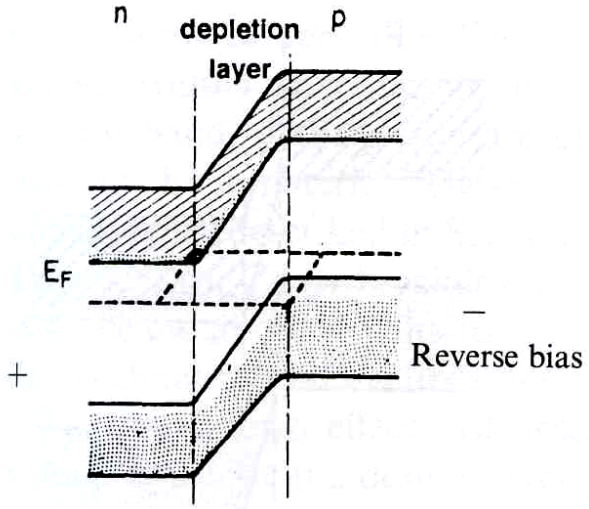
Figure 8.26. (a) Biasing of an *n–p–n* bipolar transistor. (b) Schematic band diagram (partial) of a biased *n–p–n* bipolar transistor. (c) Symbol used for a bipolar *n–p–n* transistor.

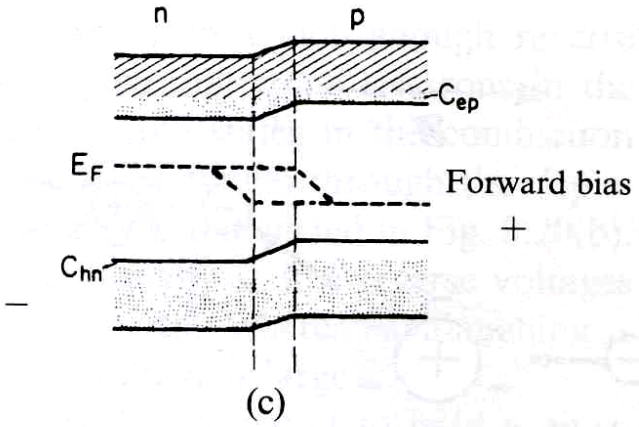
Electron flow from E to C can be controlled by the bias voltage on the Base.

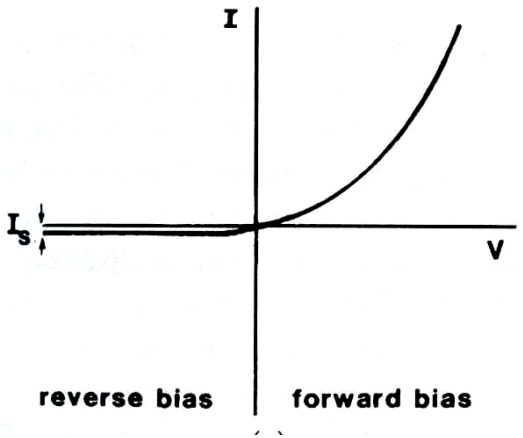
8.7 Semiconductor Devices

* Diode $p-n$

참고) Figure 8.19



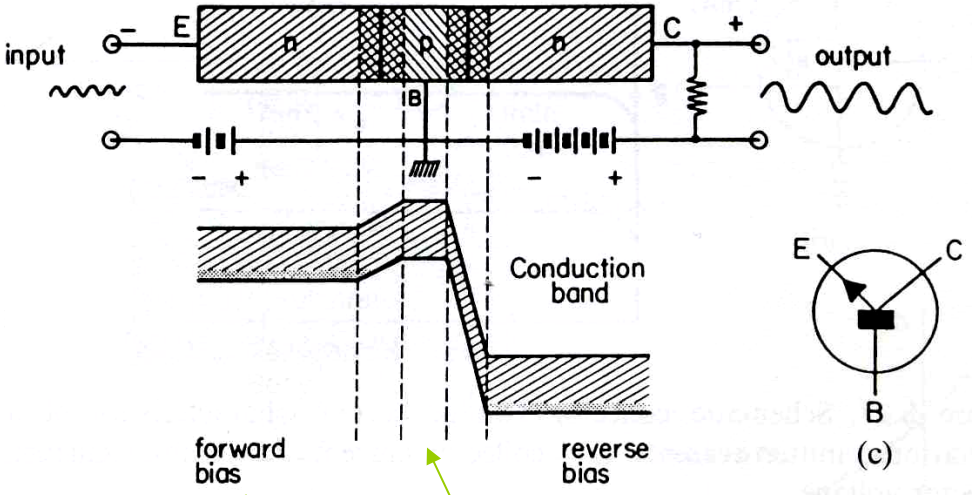




8.7 Semiconductor Devices

Transistors : amplification of music or voice
electronic switch (on & off) for logic and memory

(1) Bipolar : current flow through n-type as well as through p-type



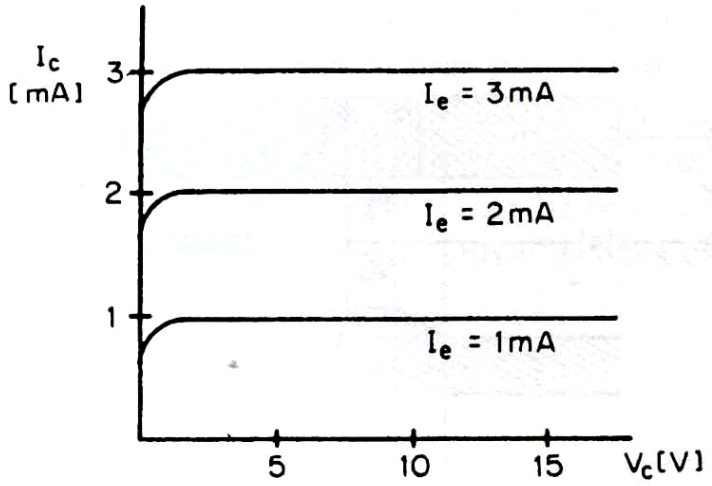


Figure 8.27. Schematic collector voltage-current characteristics of a transistor for various emitter currents. I_c=collector current, I_e=emitter current, and V_c=collector voltage.

Heavily doped **# of holes kept to a minimum(light doping) or thin**

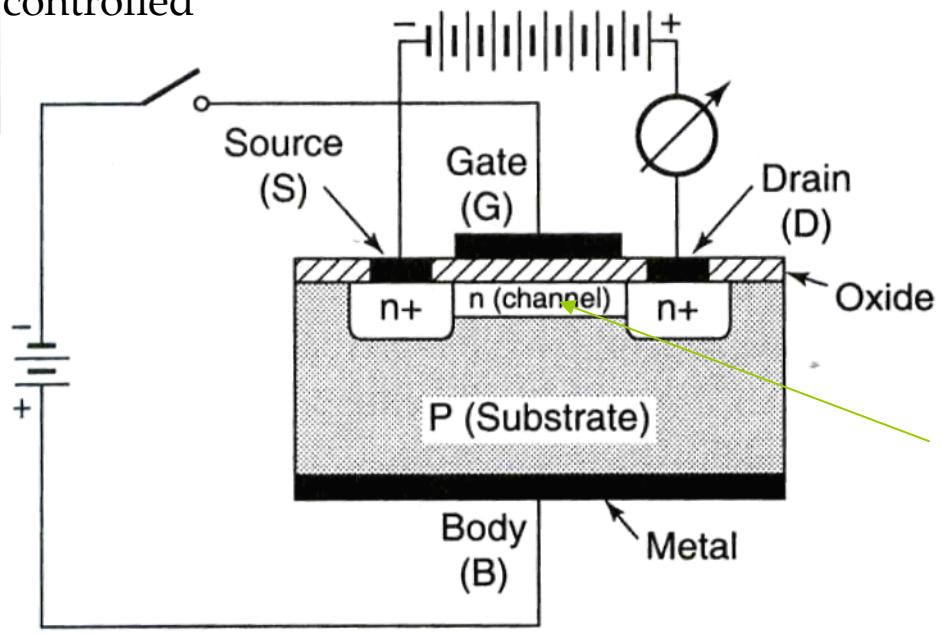
doping level is not critical

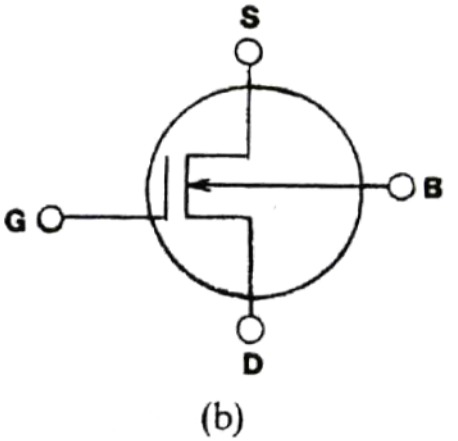
Figure 8.26. (a) Biasing of an *n–p–n* bipolar transistor. (b) Schematic band diagram (partial) of a biased *n–p–n* bipolar transistor. (c) Symbol used for a bipolar *n–p–n* transistor.

8.7 Semiconductor Devices

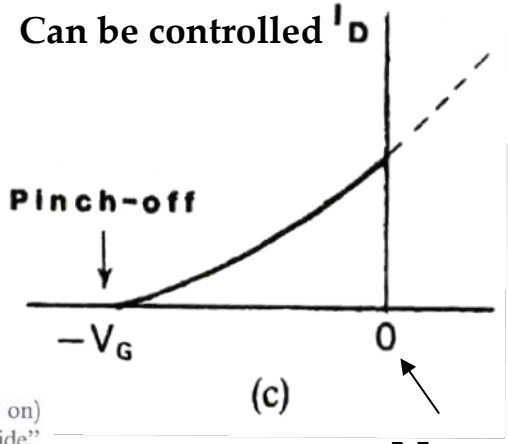
(2) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)

Electric field can be controlled





Can be controlled



Unipolar : current flow only through n-type

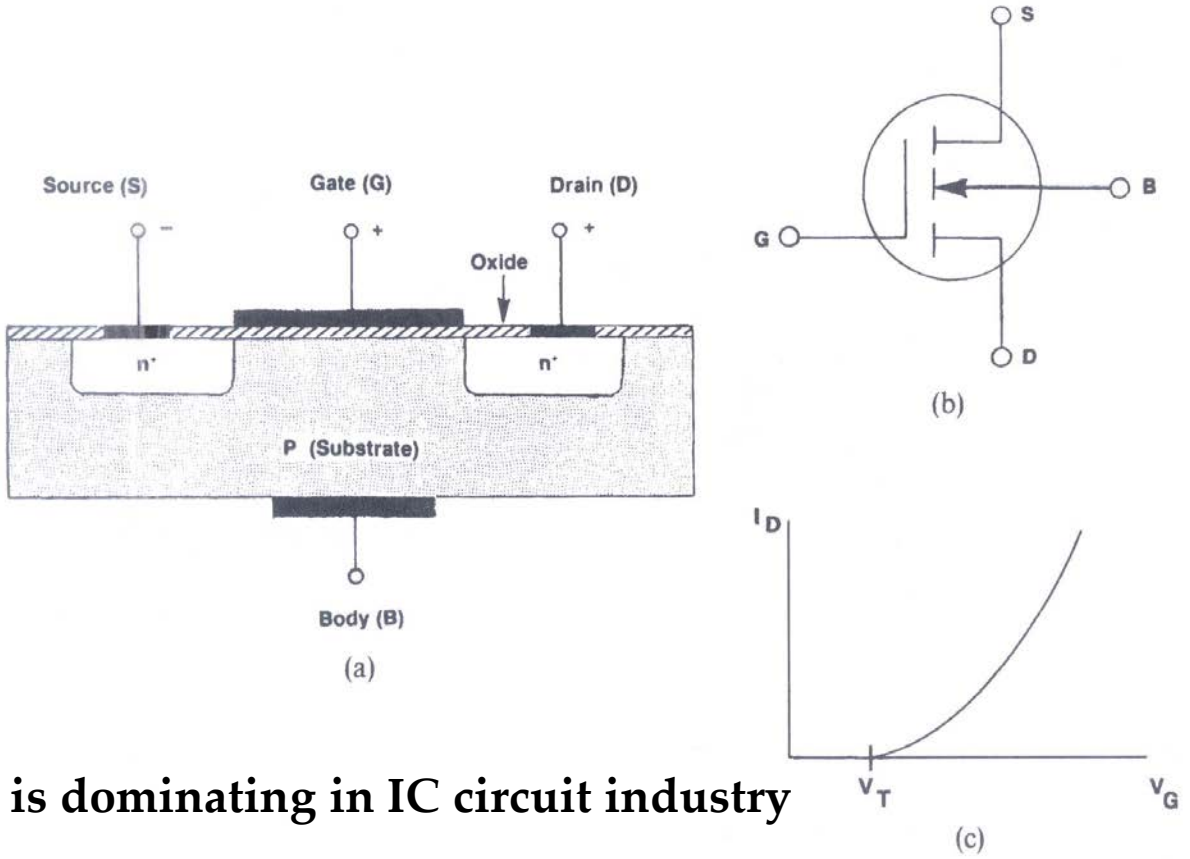
Two types: depletion-type MOSFET

Normally on

Figure 8.28. (a) Schematic representation of an *n*-channel depletion- (normally on) type MOSFET. The dark areas symbolize the (aluminum) metallizations. The "oxide" layer may consist of SiO_2, nitrides (Si_3N_4), oxinitrides (Si_3N_4–SiO_2), or multilayers of these substances. This layer is about 10 nm thick. The gate voltage is applied between terminals G and B. Quite often the B and S terminals are interconnected. (b) Circuit symbol for *n*-channel depletion-type MOSFET. (c) Gate voltage/Drain current characteristic ("Transfer" characteristic). For positive gate voltages (dashed portion of the curve) the device can operate in the "enhancement mode" (see Fig. 8.29(c)).

8.7 Semiconductor Devices

* Enhancement-type MOSFET



This type is dominating in IC circuit industry

Normally off

Figure 8.29. (a) Enhancement (normally-off)-type *n*-channel MOSFET. For details, see the caption of Fig. 8.28. (b) Circuit symbol. (The broken line indicates that the path between S and D is normally interrupted.) (c) Gate voltage (V_G)/drain current (I_D) characteristic. V_T is the threshold gate voltage above which a drain current sets in.

8.7 Semiconductor Devices

N-MOSFET
P-MOSFET

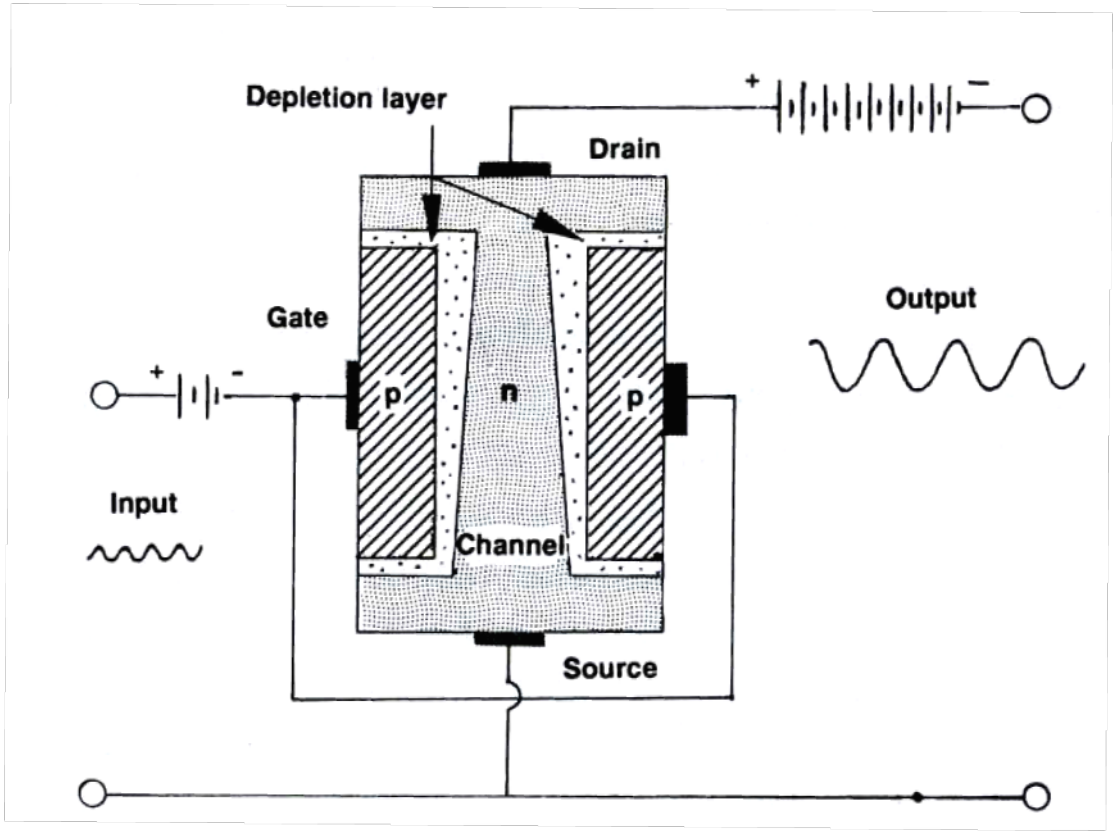
If both are integrated on one chip and wired in series, this technology is labeled CMOSFET (complementary MOSEFT)

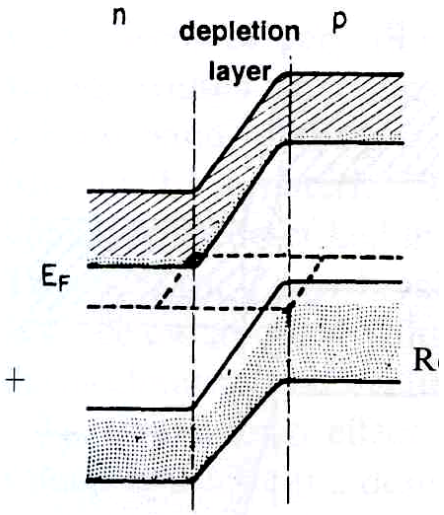
For information processing, low operating voltage, low power short channel for high speed.

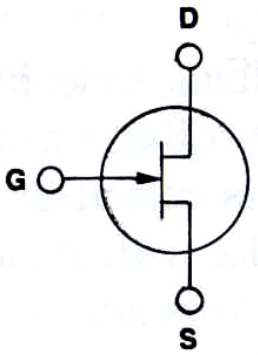
MOSFET = MOST (metal-oxide-semiconductor transistor)
= MISFET (metal-insulator-semiconductor field-effect transistor)

8.7 Semiconductor Devices

(2) Junction Field-Effect Transistor (JFET)



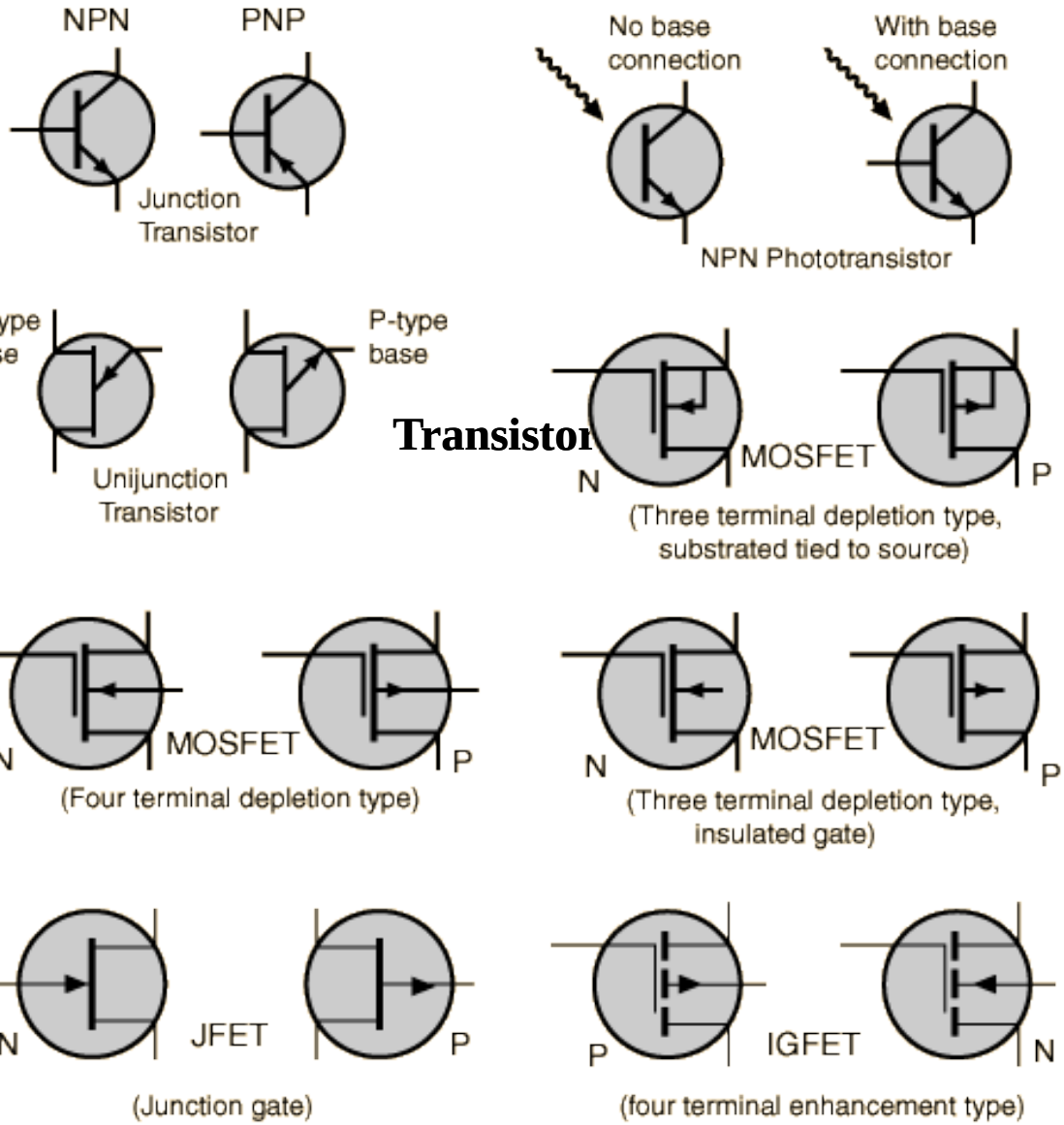




Normally on, depletion type

Figure 8.30. (a) Schematic representation of an *n*-channel junction field-effect transistor. The dark areas symbolize the metal contacts (e.g., aluminum). (b) Circuit symbol for an *n*-channel JFET. *Note*: In a *p*-channel JFET the arrow point away from the channel.

8.7 Semiconductor Devices



8.7 Semiconductor Devices

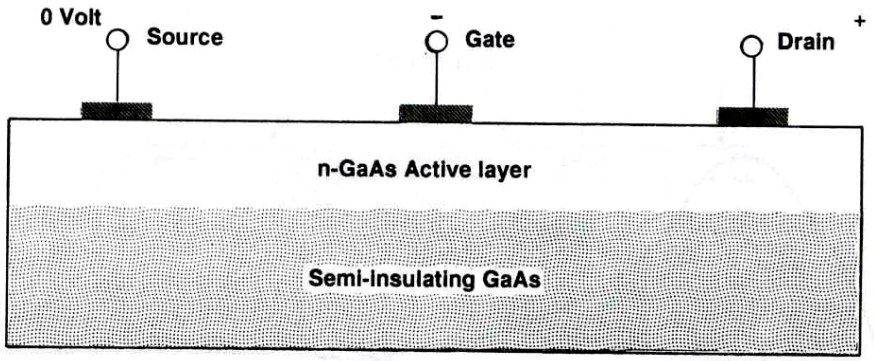


Figure 8.31. Schematic representation of a GaAs MESFET (Metal-semiconductor field-effect transistor). Source and drain metallizations (dark areas) are selected to form ohmic contacts with the *n*-doped GaAs. The gate metal forms, with the *n*-doped GaAs, a Schottky –barrier contact.

MESFET(GaAs Metal-Semiconductor FET)

- Higher switching speed. ($\mu_{GaAs} \sim 6\ \mu_{Si}$)

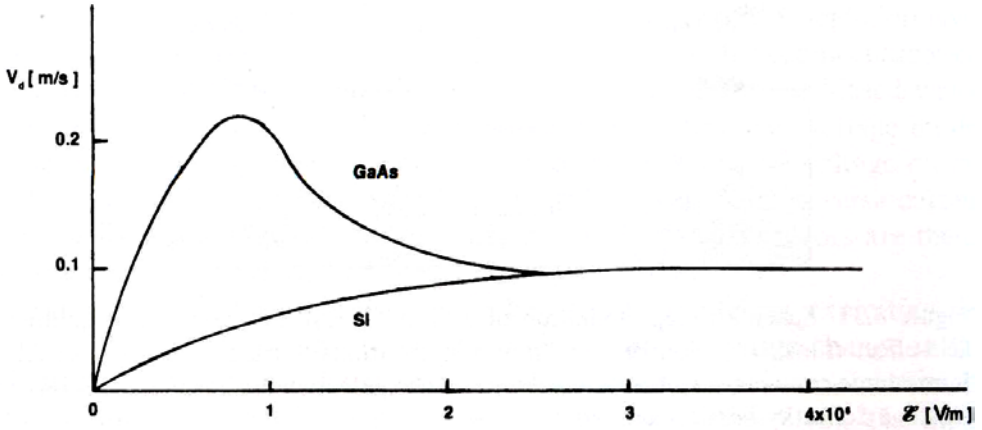
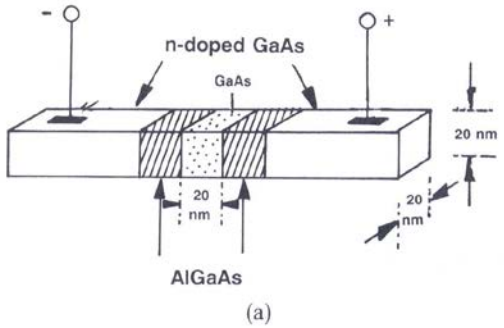


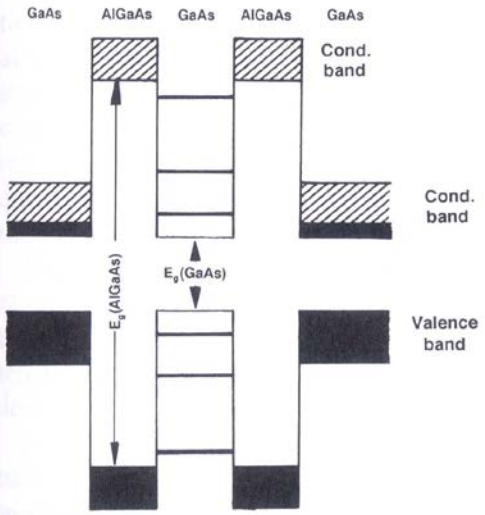
Figure 8.32. Average electron drift velocity as a function of electric field strength for GaAs and silicon.

8.7 Semiconductor Devices

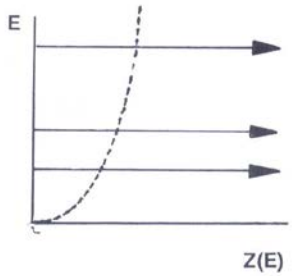
8.7.10 Quantum Semiconductor Devices



(a)



(b)



(c)

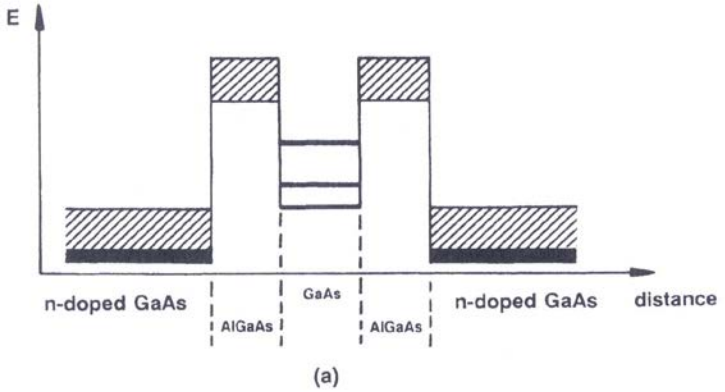
Figure 8.33. (a) Schematic representation of a quantum dot structure. (b) Energy levels for GaAs for the quantum dot structure depicted in (a). (*Note*: The gap energy difference between GaAs ($E_g = 1.42$ eV) and AlGaAs is greatly exaggerated. This difference may be as small as 0.2 eV.) (c) Discontinuous density of energy states for a quantum dot structure. The dashed parabola indicates the density of states for a bulk crystal, as is known from Fig. 6.4.

-To explain the nature of a quantum device: recall "the behavior of one electron in a potential well (Sec 4.2)"

- ***Size quantization*** : dimensions of the crystalline solid are reduced to the size of the wavelength of electron (e.g., 20nm for GaAs ; → density of state, Z(E) is quantized

- A small-band gap material is sandwiched between two layers of a "wide-band gap material (Fig 8.33a,b): the configuration for which all three dimensions of the center materials have values near the electron wavelength, is called **quantum dot** (**quantum wire** for 2-d, **quantum well** for 1-d confinement) → potential barrier between two GaAs region

8.7 Semiconductor Devices



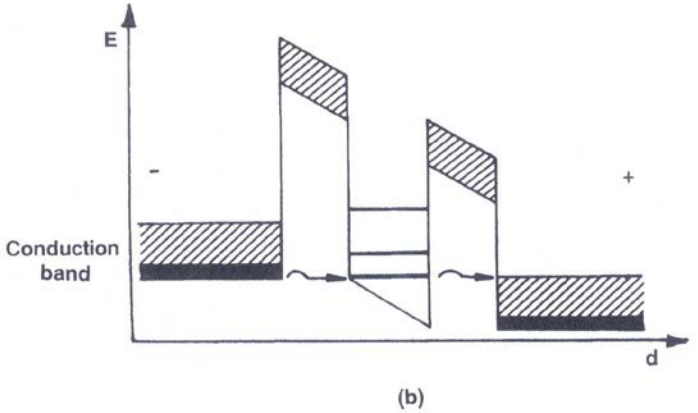


Figure 8.34. Parts of two energy band structures for the quantum device shown in Fig. 8.33. For simplicity, only the conduction bands are shown. (a) No applied voltage. (b) With applied voltage, which facilitates electron tunneling from the conduction band of the *n*-doped GaAs into an empty energy level of the center GaAs region.

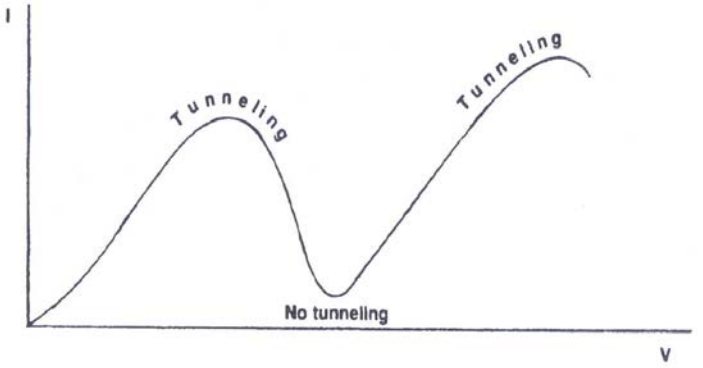


Figure 8.35. Current–voltage characteristic of a quantum dot device as depicted in Figs. 8.33 and 8.34.

- Fig 8.34: If a large voltage is applied to the device, the conduction band of the *n*-doped GaAs is raised to a level at which its conduction electrons are at the same height as an empty energy state of the center GaAs region.

→ At this point, the electrons are capable of tunneling though the potential barrier formed by the AlGaAs region and thus reach one of these discrete energy state.

8.7 Semiconductor Devices

8.7.11 Semiconductor Device Fabrication

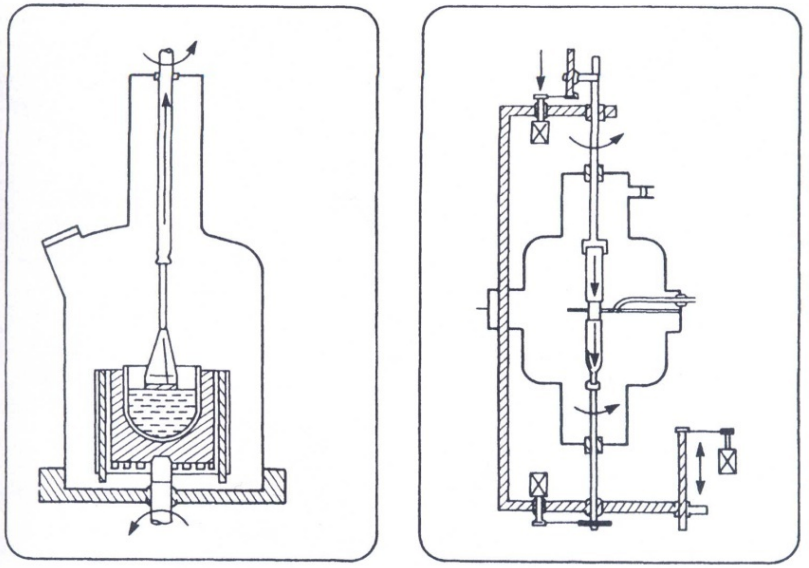
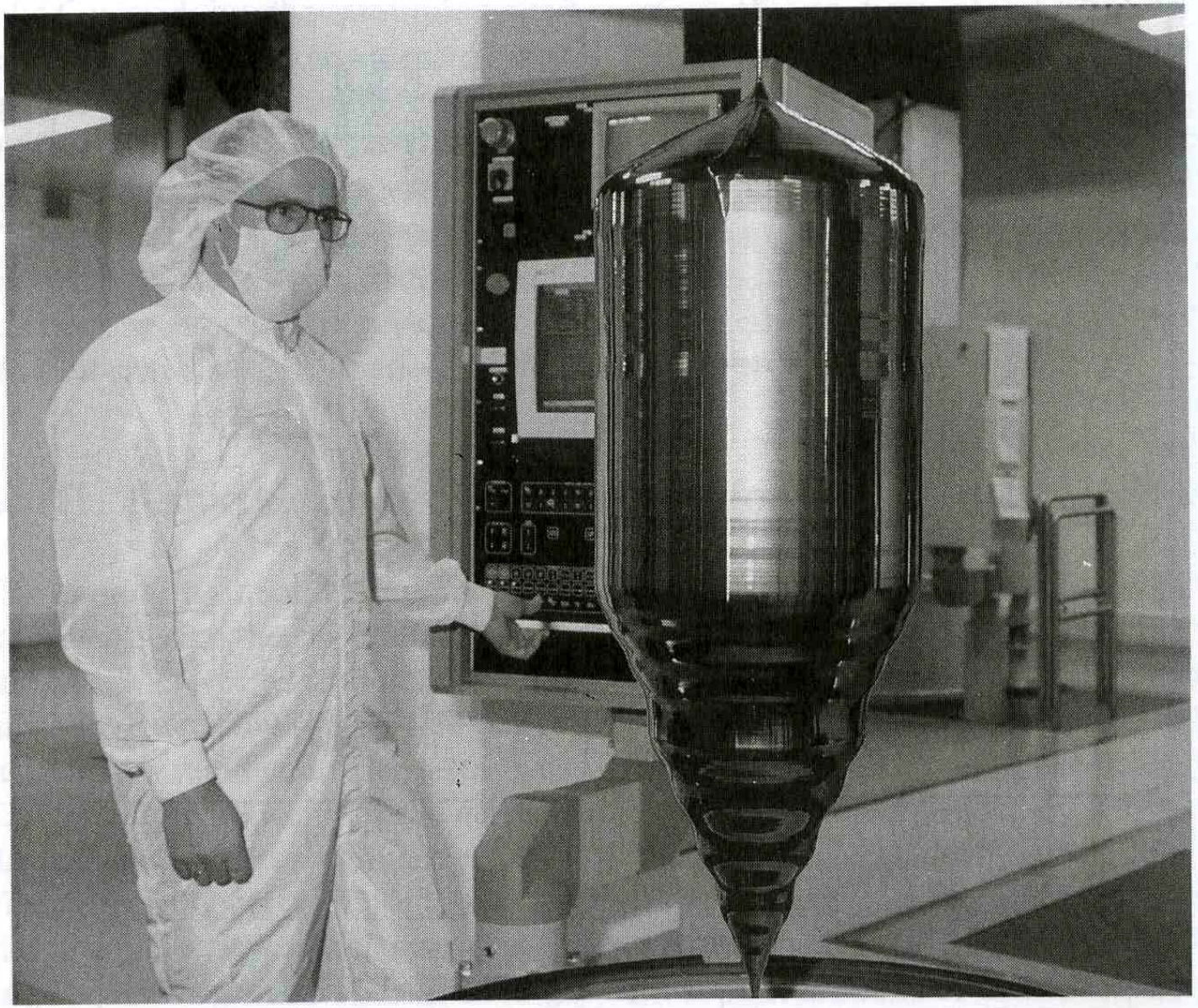


Figure 8.36. *Techniques for single-crystal growth. (a) Czochralski method. Heating* is performed by radio frequency coils or (for big crucibles) by resistance heating. (b) Float zone method. (c) Bridgman method (demonstrated for GaAs). (d) A 300 mm (12 inch) silicon single crystal is removed from the crucible. (Courtesy Wacker Siltronic AG)

8.7 Semiconductor Devices



8.7 Semiconductor Devices

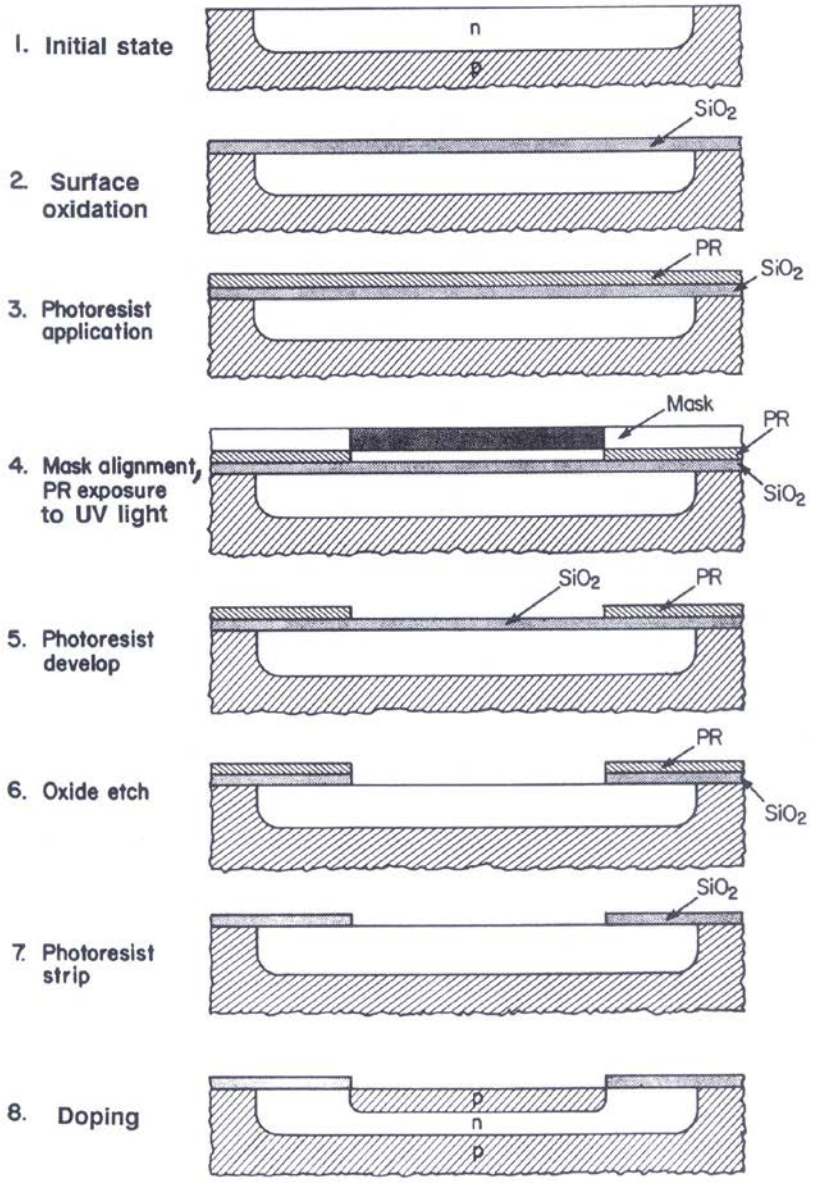


Figure 8.37. Photoresist (PR) masking sequence to obtain a *p–n–p* bipolar transistor

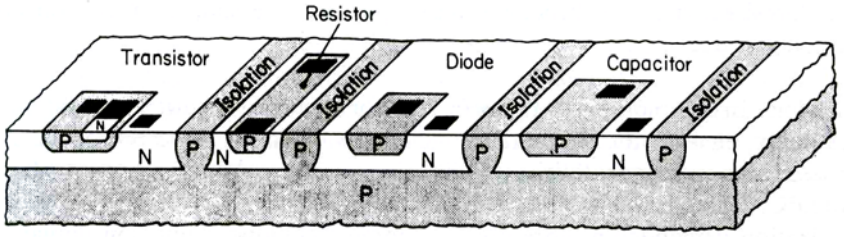


Figure 8.38. Basic component of integrated circuits (bipolar). The dark areas are the contact pads.

Device fabrication on the wafers

- Surface oxidation,
- Photolithography
- Oxide Etch
- Photoresist Strip
- Doping
- Metallization
- Packaging

8.7 Semiconductor Devices

8.7.12 Digital Circuits and Memory Devices

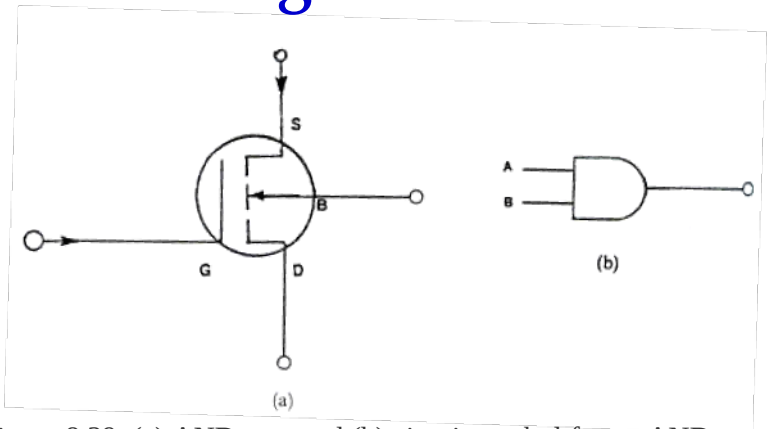


Figure 8.39. (a) AND gate and (b) circuit symbol for an AND gate. (Compare to Fig. 8.29)

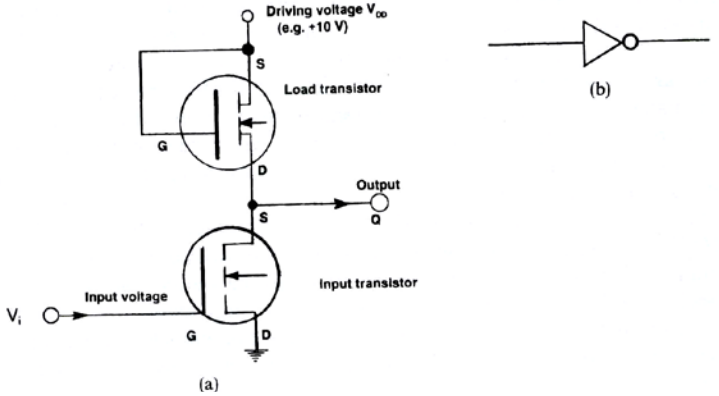


Figure 8.40. Inverter made of two "normally-off" (*n*-channel, enhancement-type) MOSFETs (NOT gate). (a) circuit; (b) symbol in wiring diagram. (V_{DD} means "Drain power supply voltage".) The load transistor may be replaced by a (poly-silicon) resistor or an enhancement-type *p*-channel MOSFET.

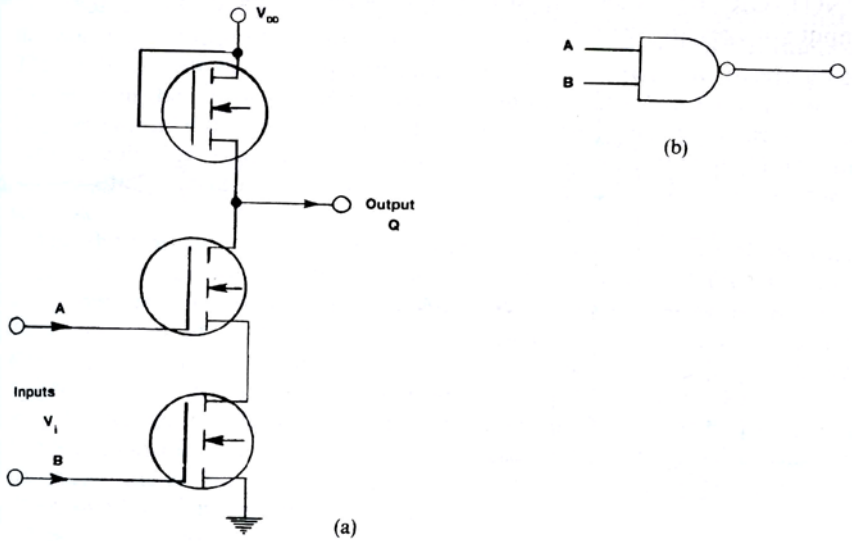


Figure 8.41. (a) NAND gate and (b) circuit symbol for an NAND digital function.

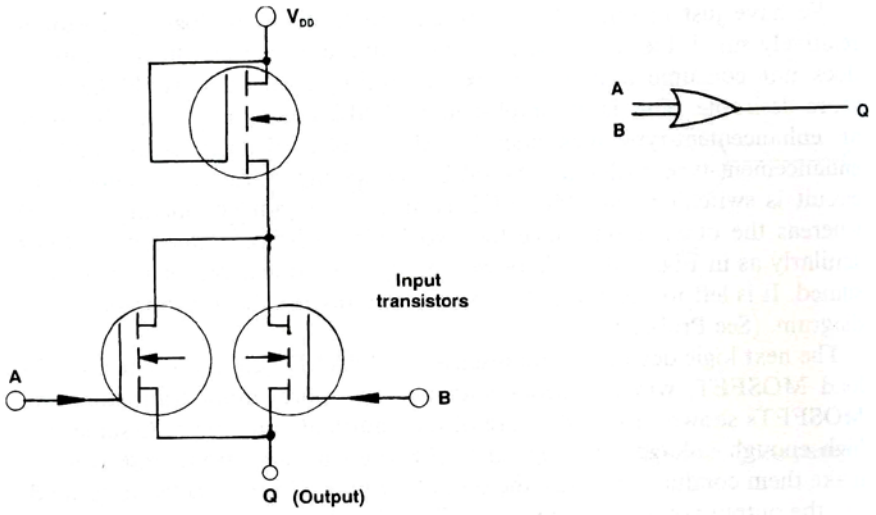


Figure 8.42. OR logic circuit with circuit symbol

8.7 Semiconductor Devices

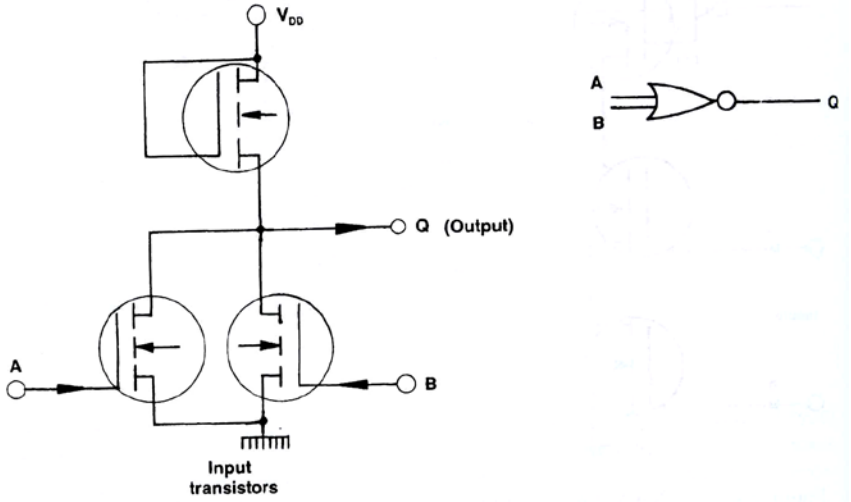


Figure 8.43. NOR logic circuit with circuit symbol

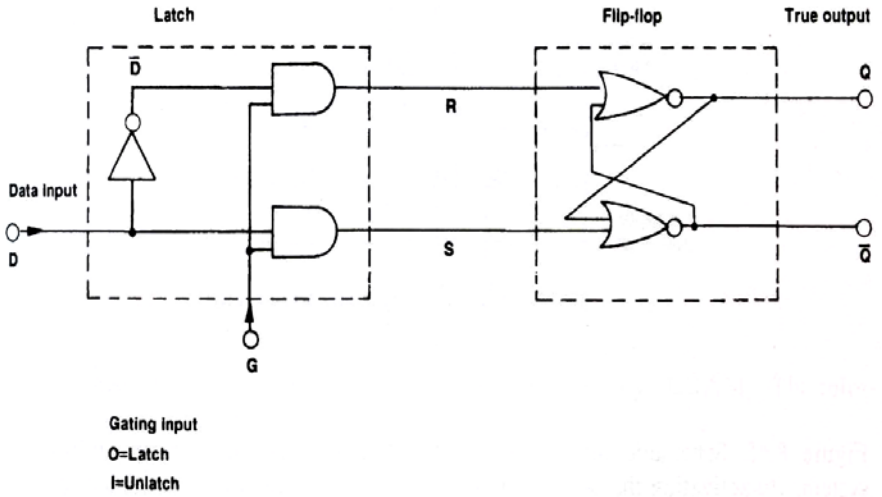


Figure 8.44. SRAM memory device called *R-S flip-flop with latch*. (The bar on a letter signifies the complement information.)

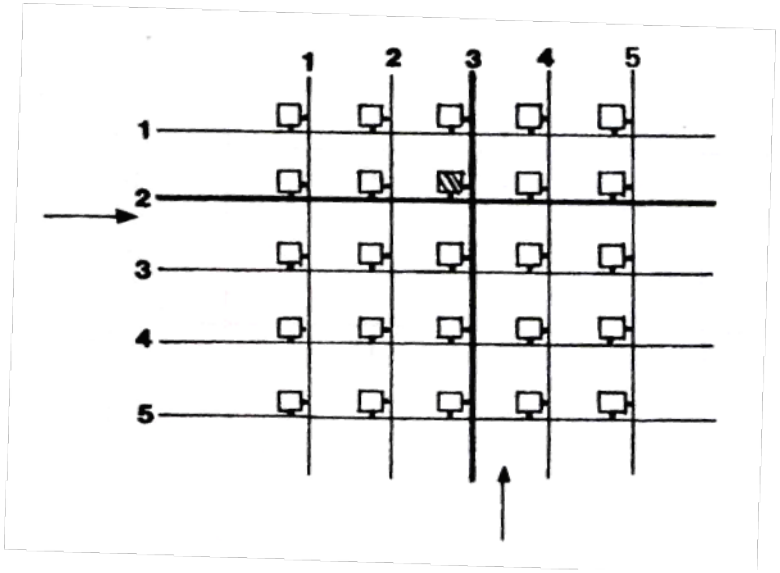


Figure 8.45. Schematic representation of a two-dimensional memory addressing system. By activating the #2 row wire and the #3 column wire, the content of the cross-hatched memory element (situated at their intersection) can be changed.

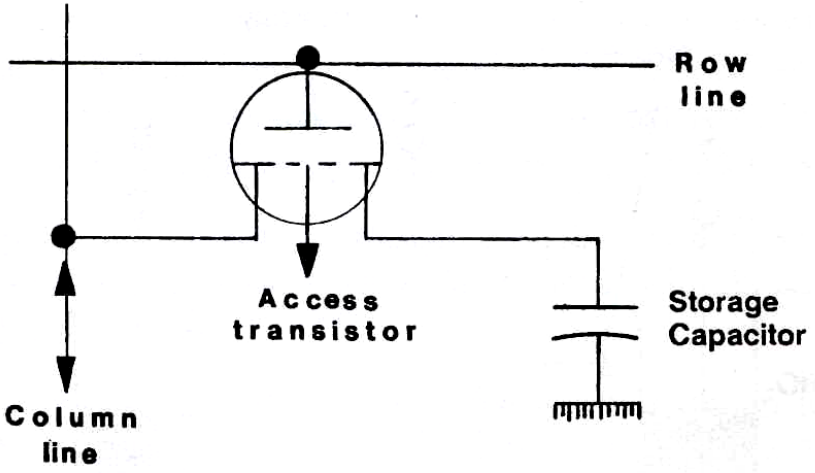


Figure 8.46. One-transistor dynamic random-access memory (DRAM). The information flows in and out through the column line.

8.7 Semiconductor Devices

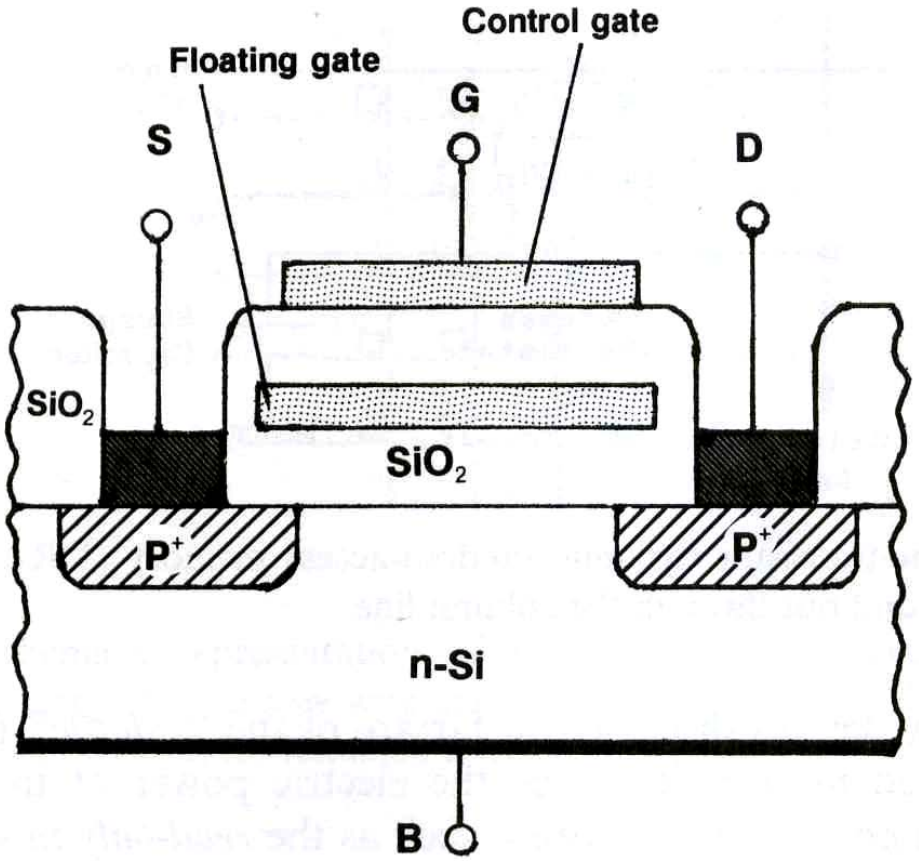


Figure 8.47. Electrically erasable-programmable read-only memory device (EEPR-OM), also called stacked-gate avalanche-injected MOS (SAMOS), or, with some modifications, flash memory device.