Chapter 6
The Operational Amplifier

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Amplifier Properties

Operational Amp.

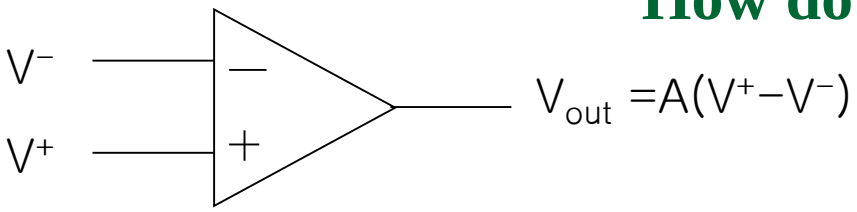
1947 – Ragazza : Diff. Equation Solver

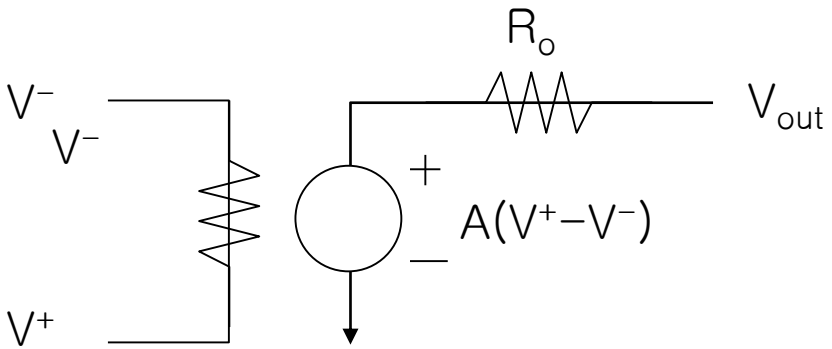
1962 – Module형 OP Amp.

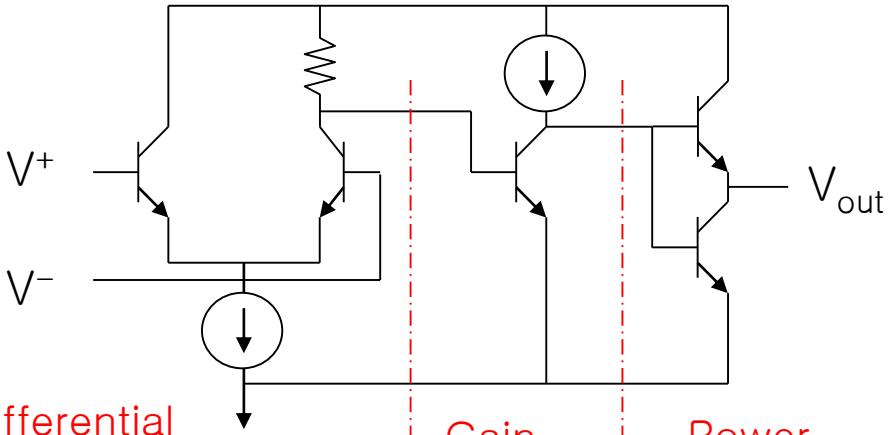
1970 – Chip

Ideal Op. Amp.	ideally	means
gain(open-loop)	∞	**≥ 10^4**
open-loop BW	∞	**Dominant Pole at 10Hz**
CMRR	∞	**≥ 70dB**
Ri	∞	**≥ 10MΩ**
Ro	**0**	**< 500Ω**
I B	**0**	**< 0.5μA**
Vos	**0**	**< 10mV**
Ios	**0**	**< 0.2μA**

How do we achieve these properties?







741인 경우

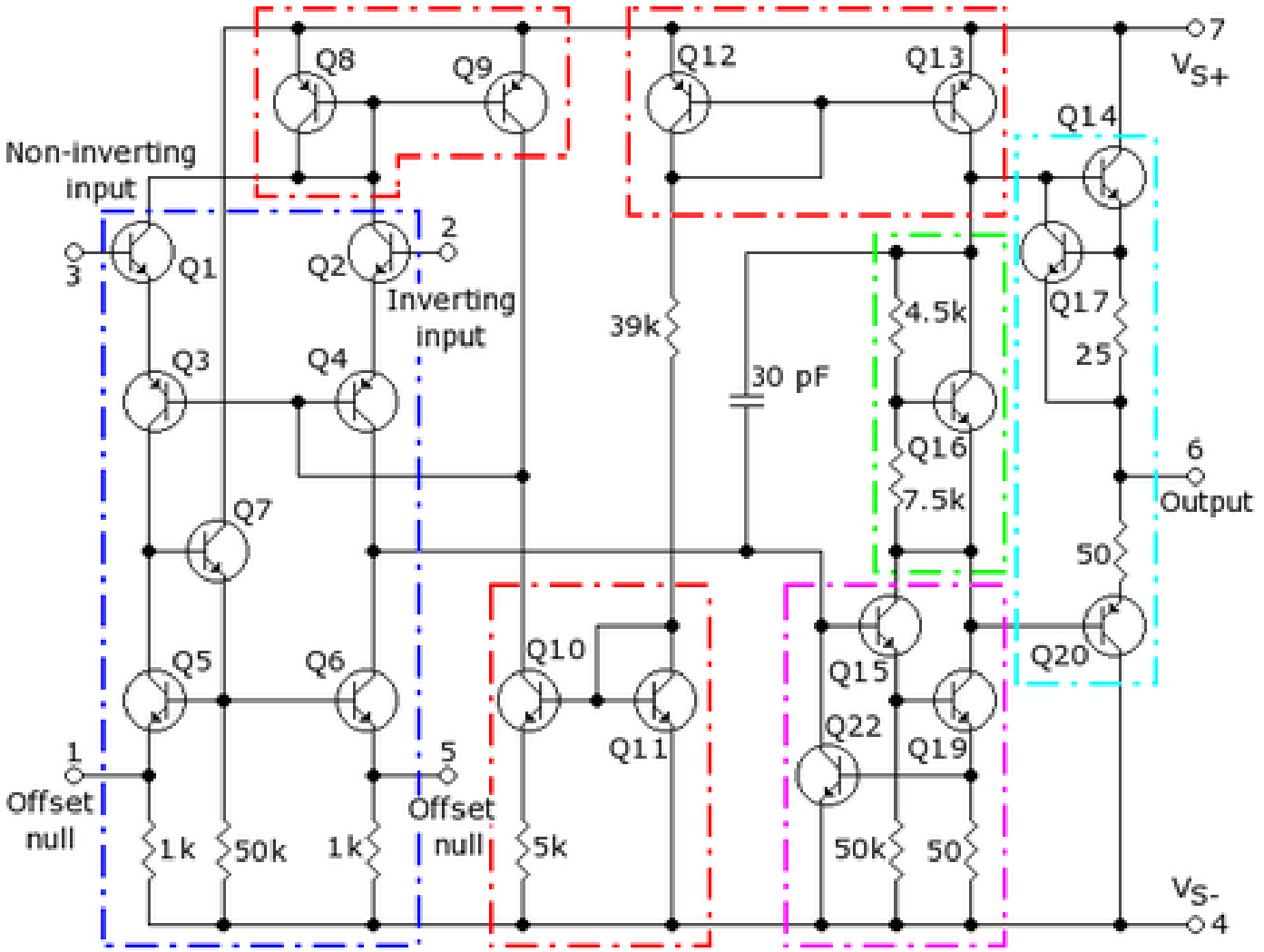
(Stage 1) R=1.6MΩ
Gain=1200

(Stage 2) V_{tg} gain=220

(Stage 3) Ro=60Ω
V_{tg} gain=1

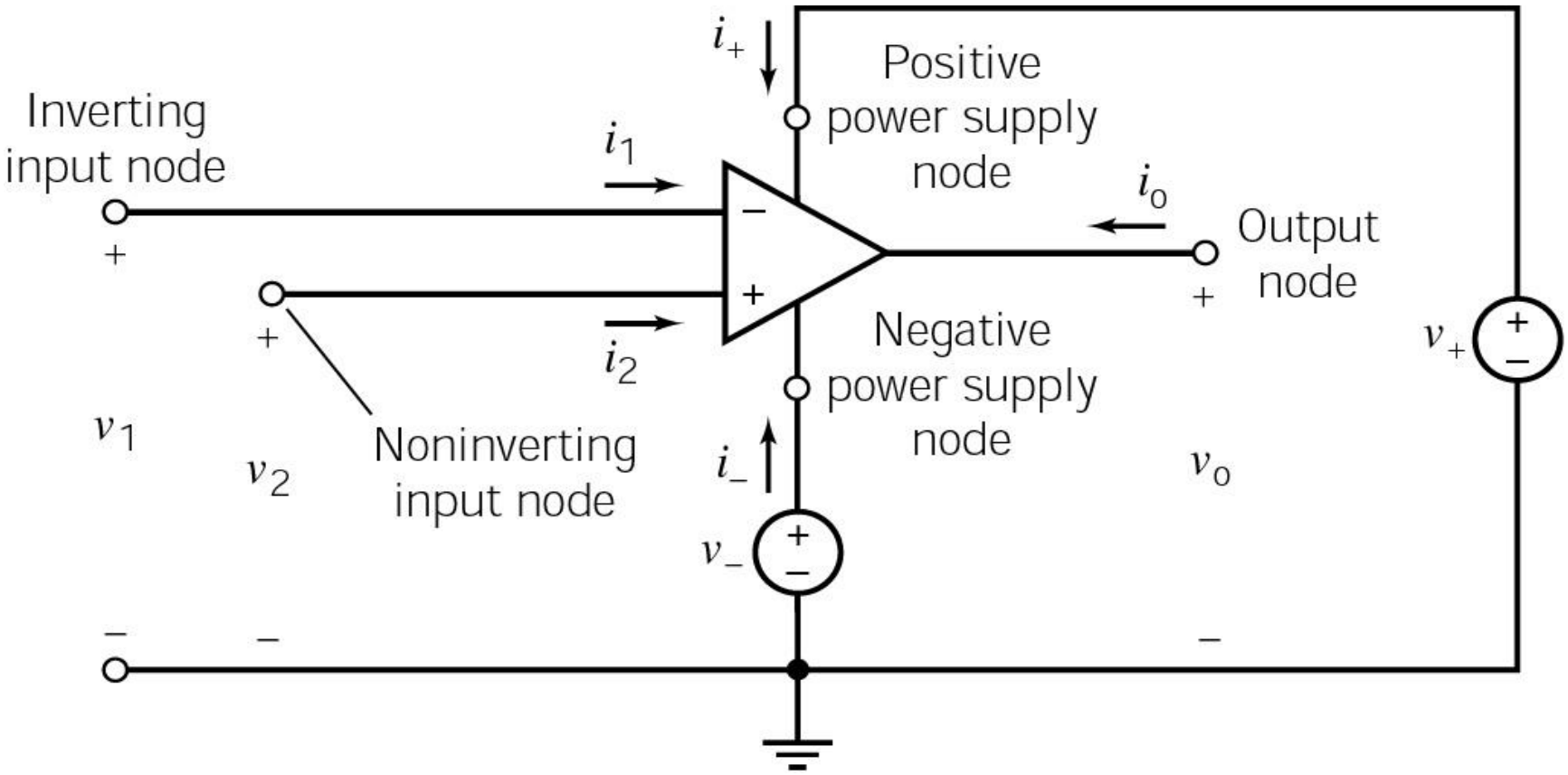
Overall Gain=108dB

Internal Circuitry



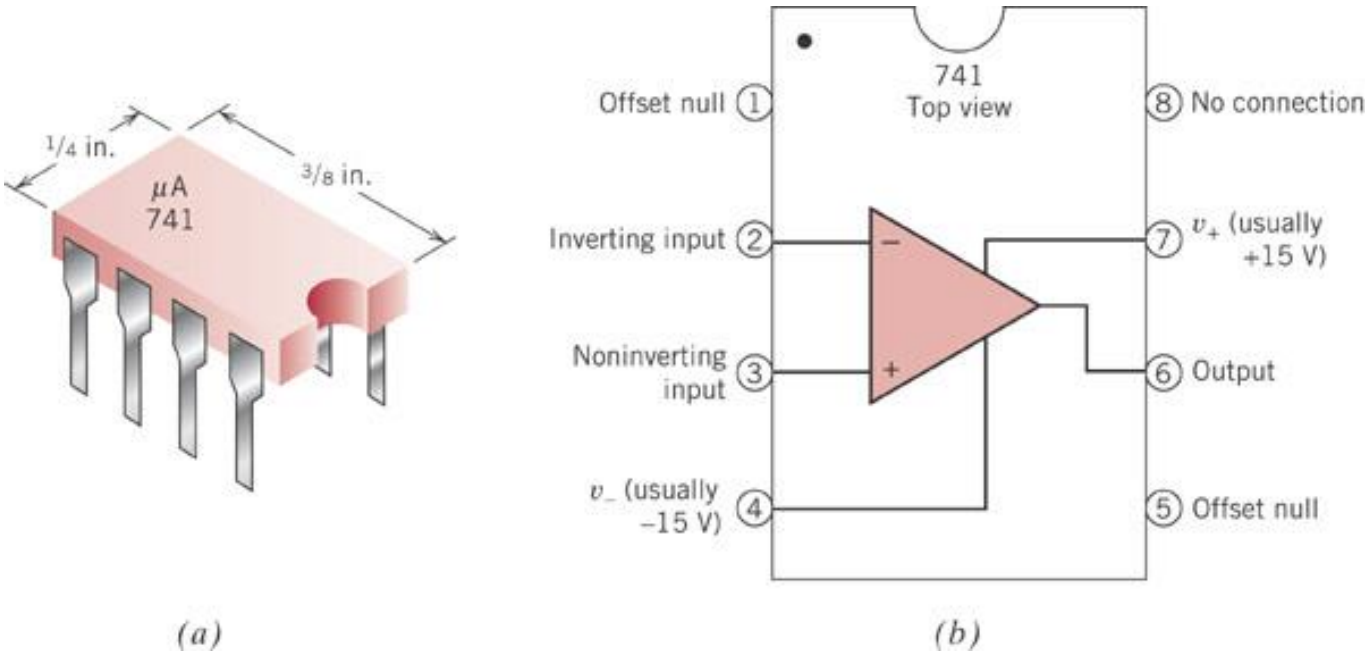
Notation

An op amp, including power supplies v_+ and v_-.



The Operational Amplifier

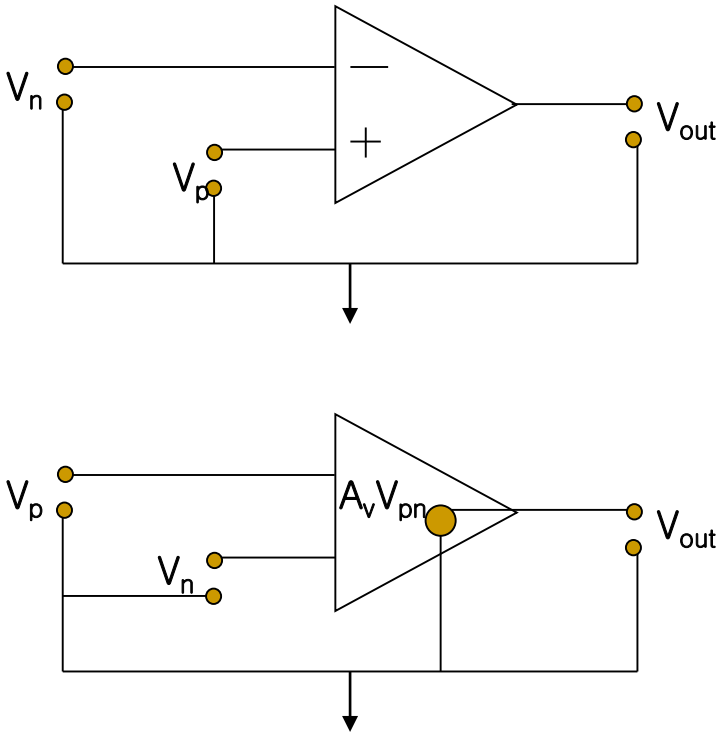
- μA741 op amp



a. A uA 741 IC has eight connecting pins.

b. The Correspondence between the circled pin numbers of the IC and the nodes of the op amp.

OP amp



$V_{out}=A_v v_{pn}=A_v(v_p-v_n)$

A_v : open loop gain

ideally infinite,

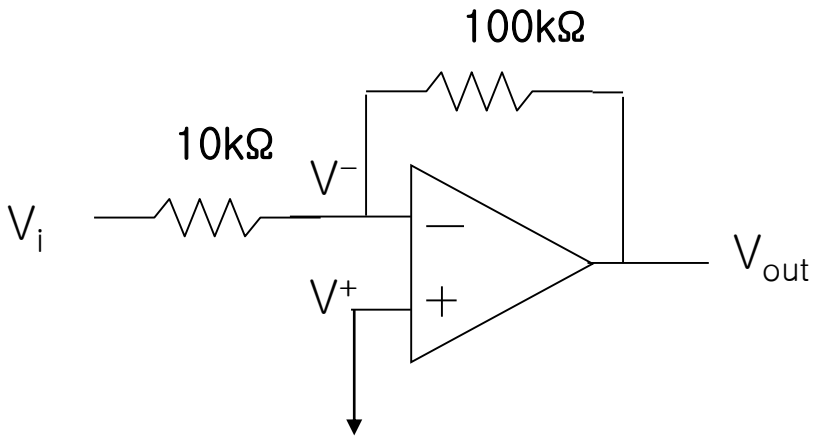
about 10^6 in real.

For ideal OP Amp(infinite A_v),

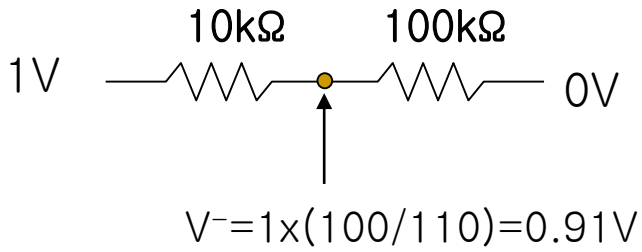
$i_p=i_n=0$,

$v_p=v_n$ (When the amp is in linear region, and almost always with a negative feedback connection)

negative feedback used in OP amp circuits

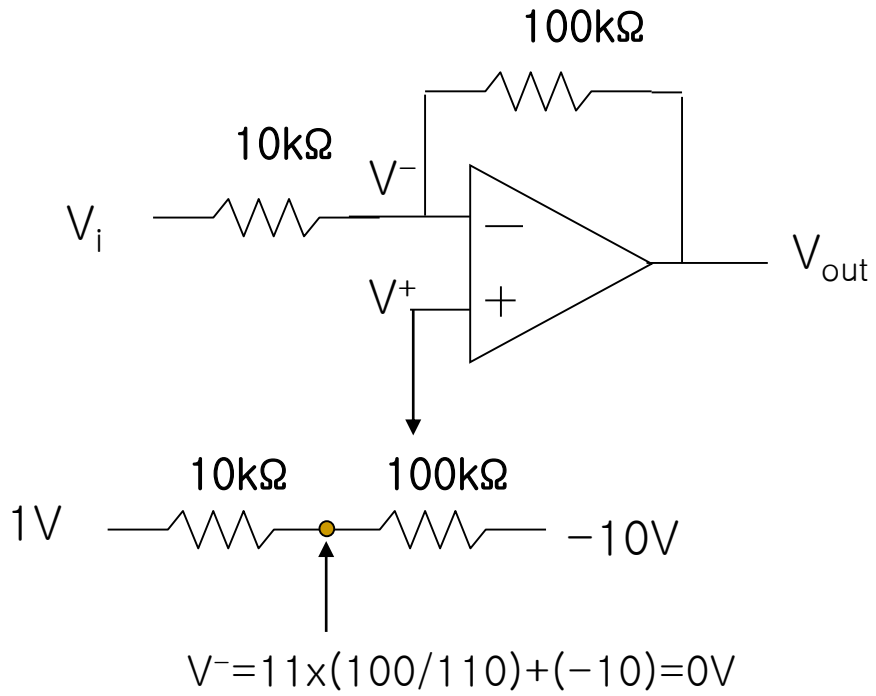


Suppose V_{in} =1V and V_{out} does not cooperate and for example sits at 0V, then



Op amp would sense this huge voltage difference at input and bring V_{out} to go negative. Because of negative feedback, this circuit will try to make the input voltage difference to zero.

negative feedback (2)

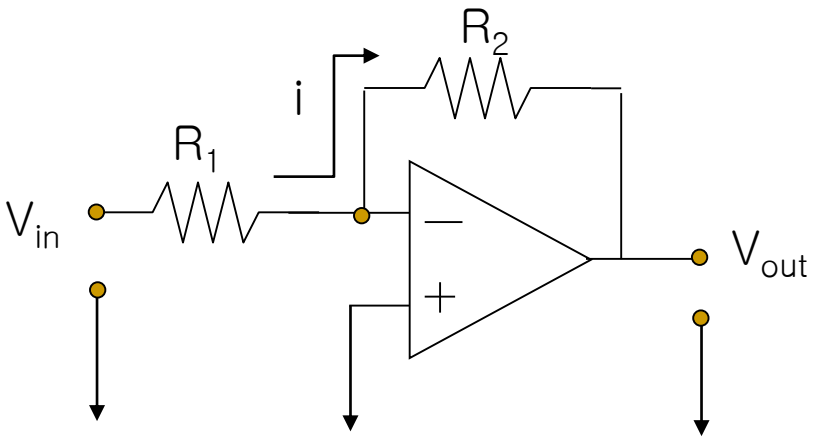


At that regulated point (output voltage=−10V) both op amp inputs are at same voltage.

With all circuits utilizing OP amps, negative feedback is essential, thus the inverting input terminal is used for feedback.

-inverting amplifier

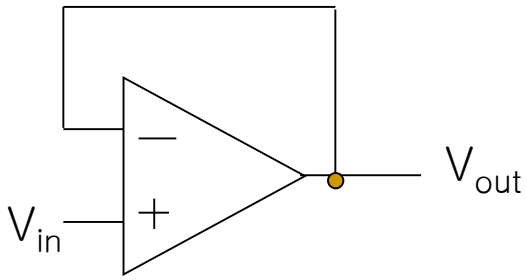
해석착안점: virtual ground, KCL



$$v_{out} = v_{in}(-\frac{R_2}{R_1})$$

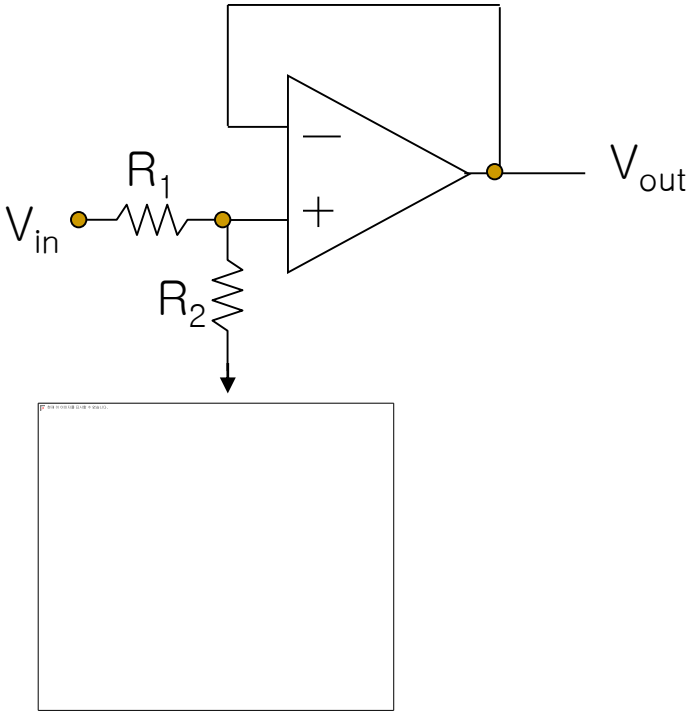
$$G = \frac{v_{out}}{v_{in}} = -\frac{R_2}{R_1}$$

-Unity buffer(voltage follower)



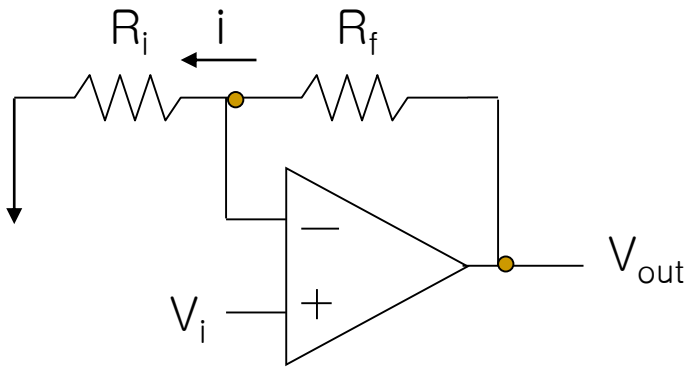
$V_{out} = V_{in}$

$G=1$



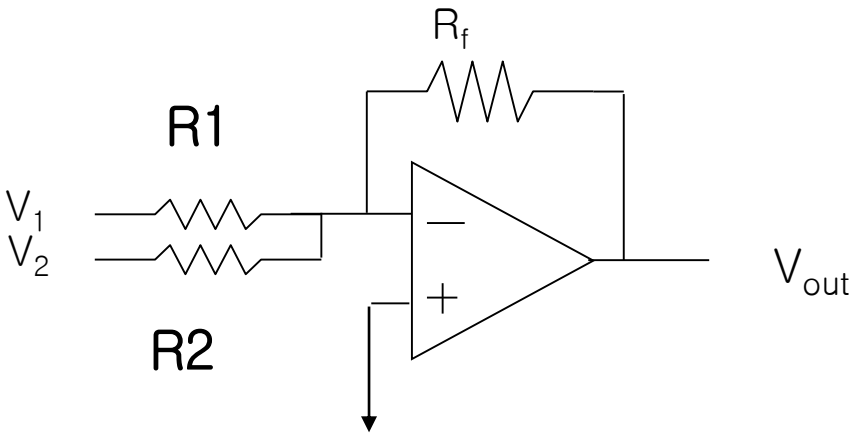
Unity buffers drive a current into a load without drawing any current from the input source since $i_{in}=i_p=0$. This is particularly important feature for physiological measurements.

Noninverting amp
(Gain>1)



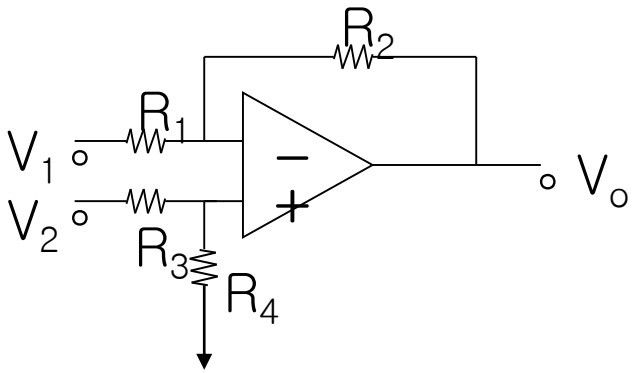
$$V_o = i \bullet (R_{i+}R_f)$$
$$V_i = i \bullet R_i$$
$$\rightarrow A_v = \frac{R_{i+}R_f}{R_i}$$

Inverting summer



$$v_{out} = \left(\frac{-R_f}{R_1}\right)v_1 + \left(\frac{-R_f}{R_2}\right)v_2$$

Subtractor



$V^+ = V2 \cdot [R4/(R3+R4)]$

$V^- = (V0-V1) \cdot [R1/(R1+R2)] + V1$

$V^+ = V^-$ 로 부터,

$Vo = [R4/(R3+R4)] \cdot [1+(R2/R1)] \cdot V2 - (R2/R1)V1$

If, $R_3/R_4 = R_1/R_2$ -> $V_0 = (R_2/R_1)(V_2-V_1)$

$G_d = R_2/R_1$

The Ideal Operational Amplifier

- The op amp output voltage and current must satisfy three conditions in order for an operational amplifier to be linear, that is:

$$|v_o| \le v_{sat}$$
$$|i_o| \le i_{sat}$$
$$\left|\frac{dv_o(t)}{dt}\right| \le SR$$

Eq 6.3.1

  - The saturation voltage, v_{sat}, the saturation current, i_{sat}, and the slew rate limit, SR, are parameters of an op amp.
  - For example, if a uA741 op amp is biased using +15V and -15V power supplies, then

$$v_{sat} = 14 \text{ V}, \quad i_{sat} = 2 \text{ mA}, \quad SR = 500{,}000 \ \frac{\text{V}}{\text{S}}$$

Eq 6.3.2

The Ideal Operational Amplifier

- The ideal op amp is a simple model of an op amp that is linear.

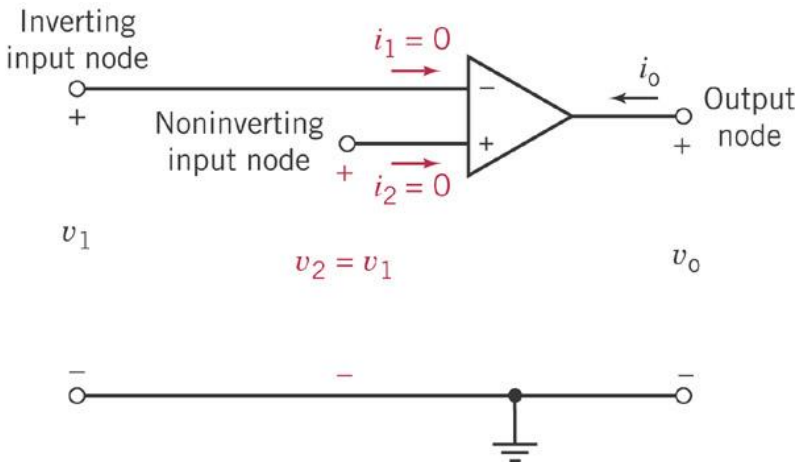
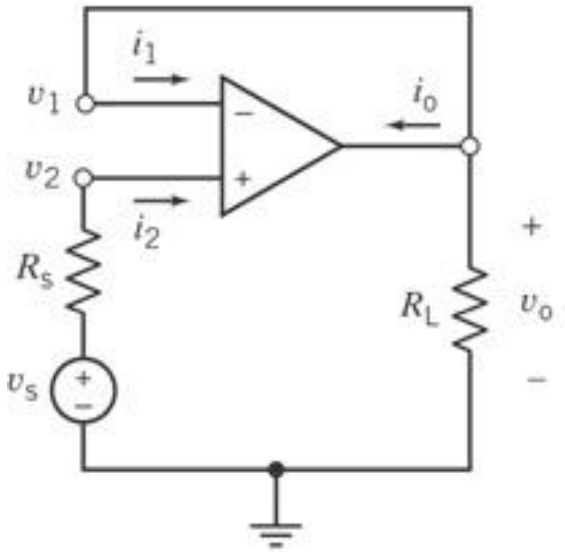


Table 6.3-1 Operating conditions for an ideal operational amplifier	
Variable	Ideal condition
Inverting node input current	$i_1=0$
Noninverting node input current	$i_2=0$
Voltage difference between inverting node voltage v1 and noninverting node voltage v2	$v_2-v_1=0$

Example 6.3-1 Ideal operational amplifier

- Consider the circuit shown in Figure 6.3-2a. Suppose the operational amplifier is a uA741 operational amplifier. Model the operational amplifier as an ideal operational amplifier. Determine how the output voltage, v_o, is related to the input voltage, v_s.



Solution

- Figure 6.3-2b shows the circuit when the operational amplifier of Figure 6.3-2a is modeled as an ideal operational amplifier.
  1. The inverting input node and output node of thee operational amplifier are connected by a short circuit, so the node voltage at these nodes are equal:

$$v_1 = v_o$$

  2. The voltages at the inverting and noninverting nodes of an ideal op amp are equal

$$v_2 = v_1 = v_o$$

  3. The currents into the inverting and noninverting nodes of an operational amplifier are zero, so

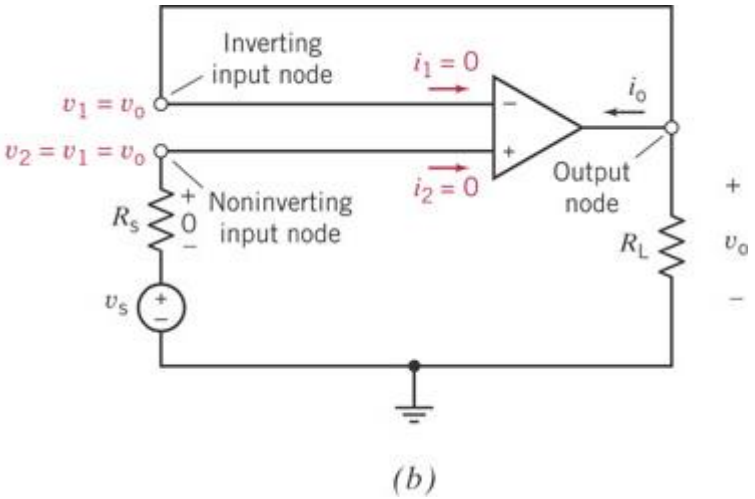
$$i_1 = 0, \quad i_2 = 0$$

  4. The current in resistor R_s is i_2=0, so the voltage across R_s is 0V. The voltage across R_s is v_s-v_2= v_s -v_o; hence

$$v_s - v_o = 0$$

or

$$v_s = v_o$$



Solution (cont'd)

- Apply KCL at the output node of the operational amplifier to get

$$i_1 + i_o + \frac{v_o}{R_L} = 0$$

Since $i_1=0$

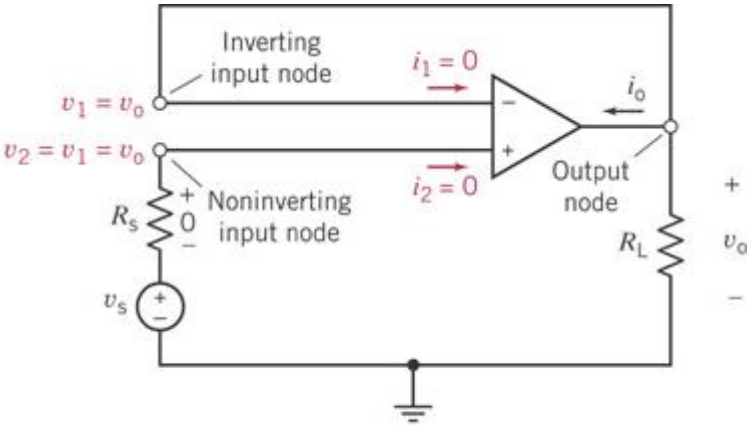
$$i_o = -\frac{v_o}{R_L}$$

now Eqs. 6.3-1 and 6.3-2 require

$$|v_s| \le 14\text{V}$$

$$\left|\frac{v_s}{R_L}\right| \le 2\text{mA}$$

$$\left|\frac{d}{dt}v_s\right| \le 500{,}000\,\frac{\text{V}}{\text{s}}$$



(b)

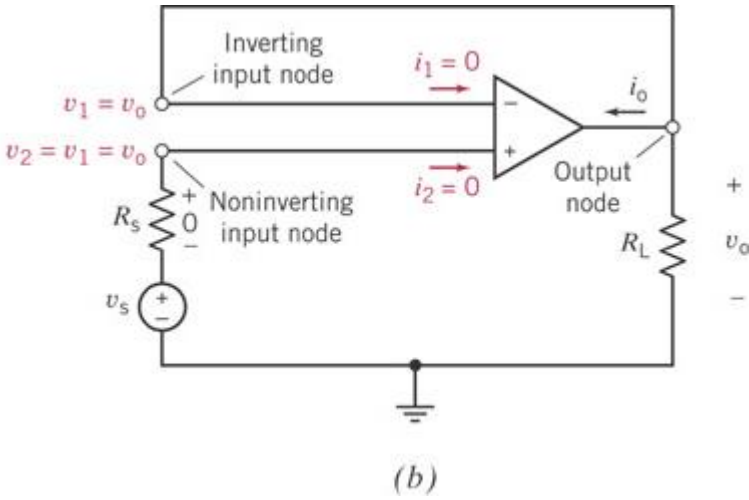
Solution (cont'd)

- For example, when v_s=10V and R_L=20kΩ

$$|v_s| = 10\text{V} < 14\text{V}$$

$$\left|\frac{v_s}{R_L}\right| = \frac{10\text{V}}{20\text{k}\Omega} = \frac{1}{2}\text{mA} < 2\text{mA}$$

$$\left|\frac{d}{dt}v_s\right| = 0 < 500{,}000\,\frac{\text{V}}{\text{s}}$$



- This is consistent with the use of the ideal operational amplifier. On the other hand, when v_s=10V and R_L=2kΩ, then

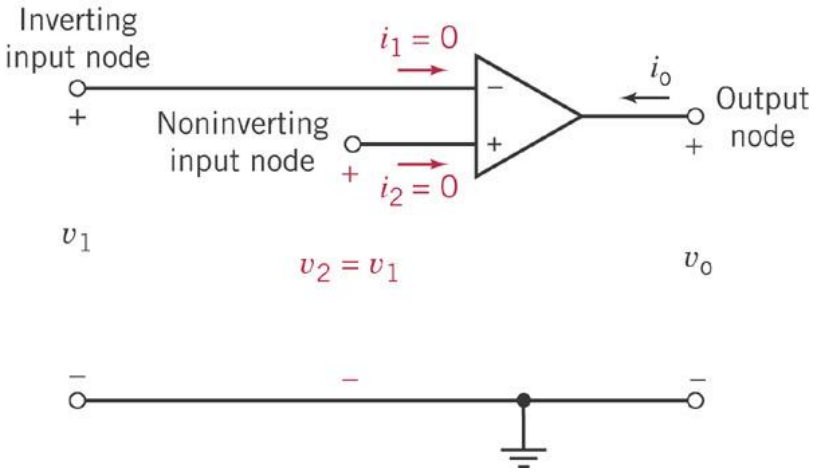
$$\frac{v_s}{R_L} = 5\text{mA} > 2\text{mA}$$

- So it is not appropriate to model the uA741 as an ideal operational amplifier when v_s=10V and R_L=2kΩ. Then v_s=10V, we require R_L>5kΩ in order to satisfy Eq. 6.3-1

Node analysis of circuits containing ideal operational amplifiers

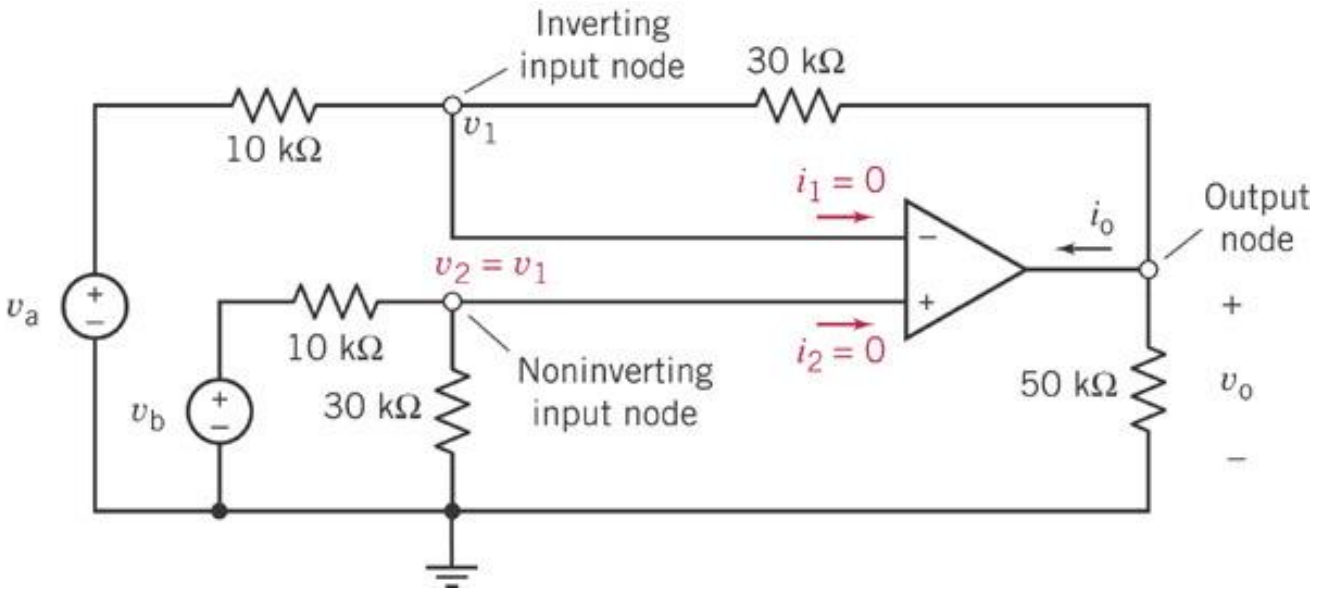
- It is convenient to use node equations to analyze circuits containing ideal op amps. There are three things to remember.

1. **The node voltage at the input nodes of ideal op amp are equal.**
2. **The currents in the input leads of an ideal op amp are zero.**
3. **The output current of the op amp is not zero**



Example 6.4-1 Difference Amplifier

- The circuit shown in Figure 6.4-1 is called a difference amplifier . The operational amplifier has been modeled as an ideal operational amplifier. Use node equations to analyze this circuit and determine v_o in terms of the two source voltages, v_a and v_b.



Solution

- The node equation at the noninverting node of the ideal operational amplifier is

$$\frac{v_2}{30000}+\frac{v_2-v_b}{10000}+i_2=0$$

Since $v_2=v_1$ and $i_2=0$, this equation becomes

$$\frac{v_1}{30000}+\frac{v_1-v_b}{10000}=0$$

Solving for v_1, we have $v_1=0.75v_b$

The node equation at the inverting node of the ideal operational amplifier is

$$\frac{v_1-v_a}{10000}+\frac{v_1-v_o}{30000}+i_1=0$$

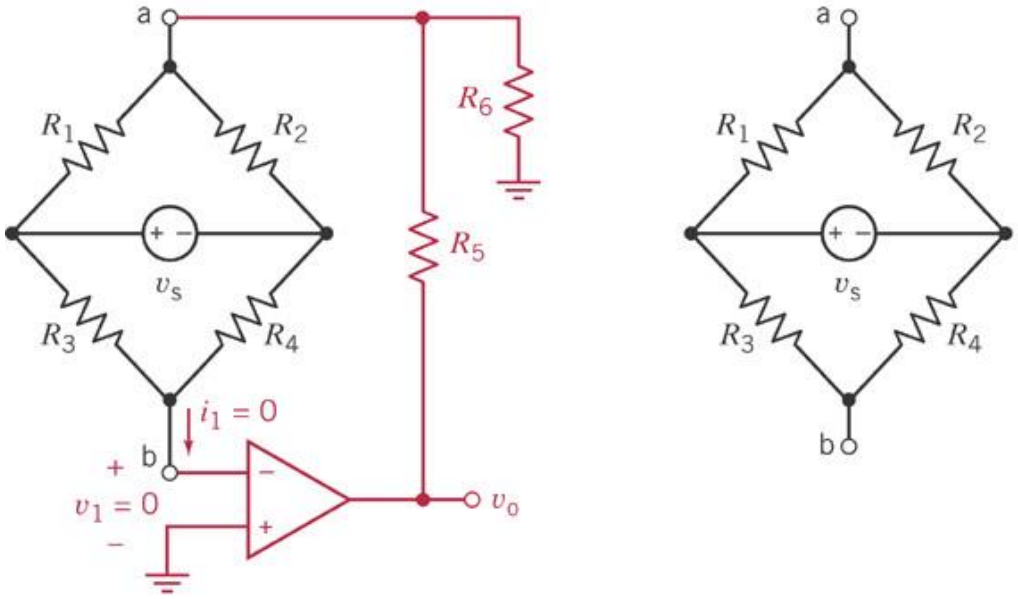
Since $v_1=0.75v_b$ and $i_1=0$, this equation becomes

$$\frac{0.75v_b-v_a}{10000}+\frac{0.75v_b-v_o}{30000}=0$$

Solving for v_o, we have $v_o=3(v_b-v_a)$

Example 6.4-2 Analysis of a Bridge Amplifier

- Next, consider the circuit shown in Figure 6.4-2a. This circuit is called a bridge amplifier. The part of the circuit that is called a bridge is shown in Figure 6.4-2b. The operational amplifier and resistors R5 and R6 are used to amplify the output of the bridge. The operational amplifier in Figure 6.4-2s has been modeled as an ideal operational amplifier. As a consequence, v1=0 and i1=0 as shown. Determine the output voltage, vo, in terms of the source voltage, vs.



Solution

- First, notice that the node voltage va is given by

$$v_a = v_1 + v_{oc} + R_t i_1$$

Since v1=0 and i1=0

$$v_a = v_{oc}$$

Now, writing the node equation at node a

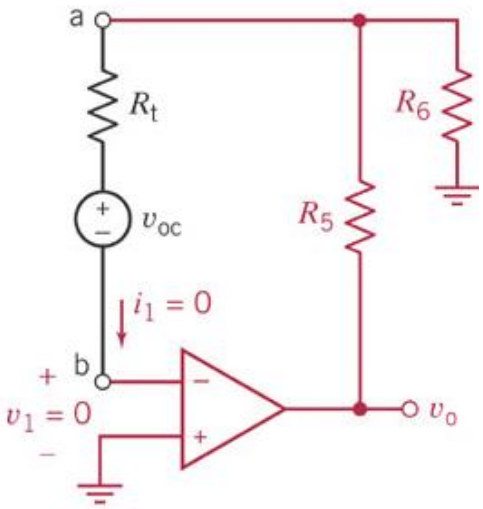
$$i_1 + \frac{v_a - v_o}{R_5} + \frac{v_a}{R_6} = 0$$

Since va=voc and i1=0

$$\frac{v_{oc} - v_o}{R_5} + \frac{v_{oc}}{R_6} = 0$$

Solving for vo, we have

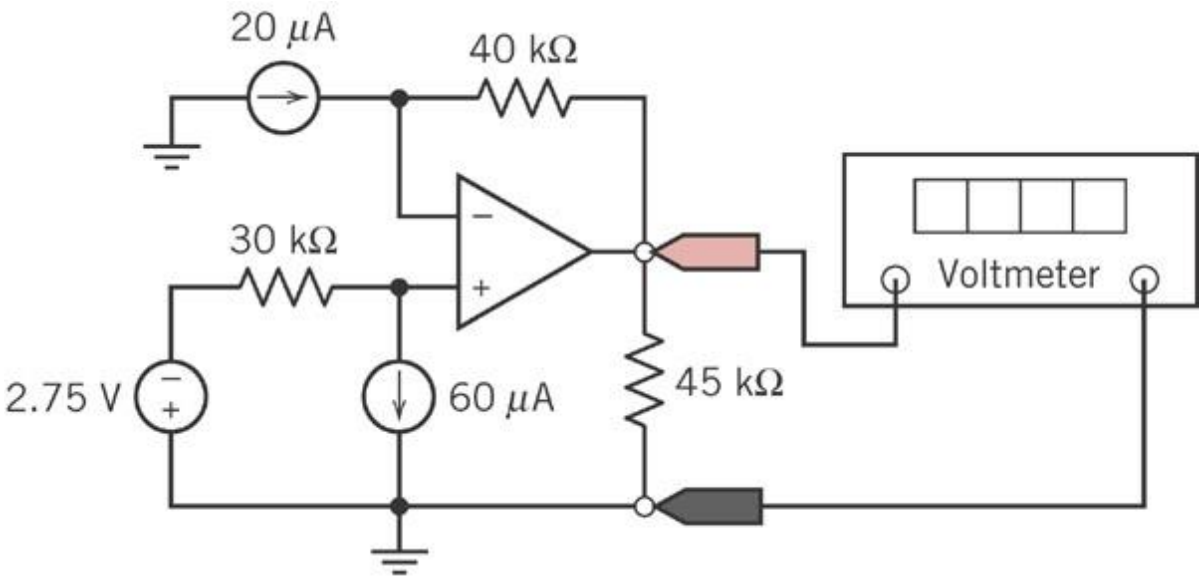
$$v_o = \left(1 + \frac{R_5}{R_6}\right) v_{oc} = \left(1 + \frac{R_5}{R_6}\right)\left(\frac{R_2}{R_1 + R_2} - \frac{R_4}{R_3 + R_4}\right) v_s$$



(d)

Example 6.4-3 Analysis of an op amp circuit using node equations

- Consider the circuit shown in Figure 6.4-3. Find the value of the voltage measured by the voltmeter.



Solution

- The output of this circuit is the voltage measured by the voltmeter. The output voltage is related to the node voltages by

$$v_m = v_4 - 0 = v_4$$

The inputs to this circuit are the voltage of the voltage source and the currents of the current source. The voltage of the voltage source is related to the node voltages at the nodes of the voltage source by

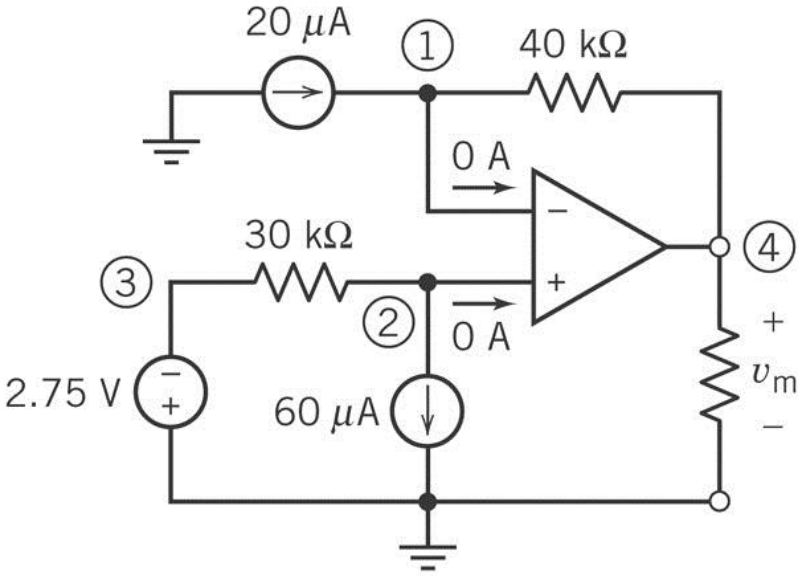
$$0 - v_3 = 2.75 \quad \Rightarrow \quad v_3 = -2.75\text{V}$$

Apply KCL to node 2 get

$$\frac{v_3 - v_2}{30000} = 0 + 60\times10^{-6} \quad \Rightarrow \quad v_3 - v_2 = 1.8\text{V}$$

using v3=-2.75V gives

$$v_2 = -4.55\text{V}$$



Solution (cont'd)

- The noninverting input of the op amp is connected to node 2. The node voltage at the inverting input of an ideal op amp is equal to the node voltage at the noninverting input. The inverting input of the op amp is connected to node 1. Consequently

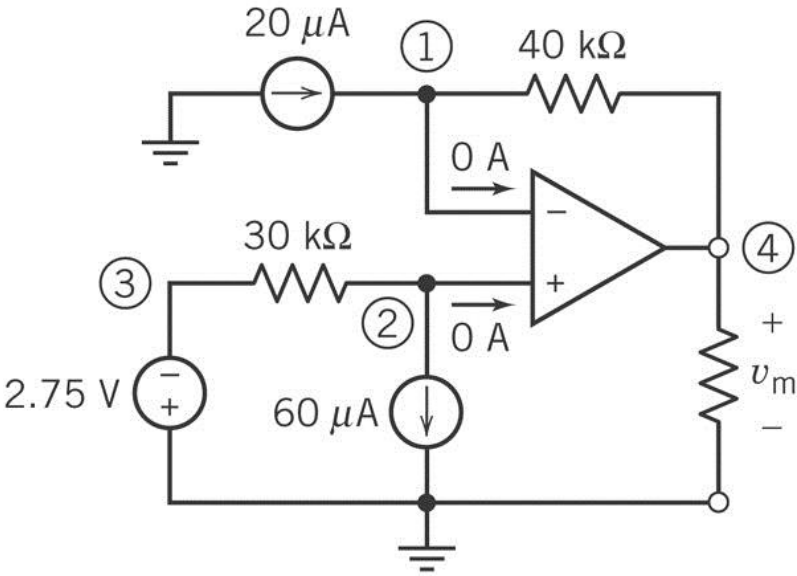
$$v_1 = v_2 = -4.55\text{V}$$

Apply KCL to node 1 to get

$$20\times10^{-6} = 0 + \frac{v_1 - v_4}{40000} \quad \Rightarrow \quad v_1 - v_4 = 0.8\text{V}$$

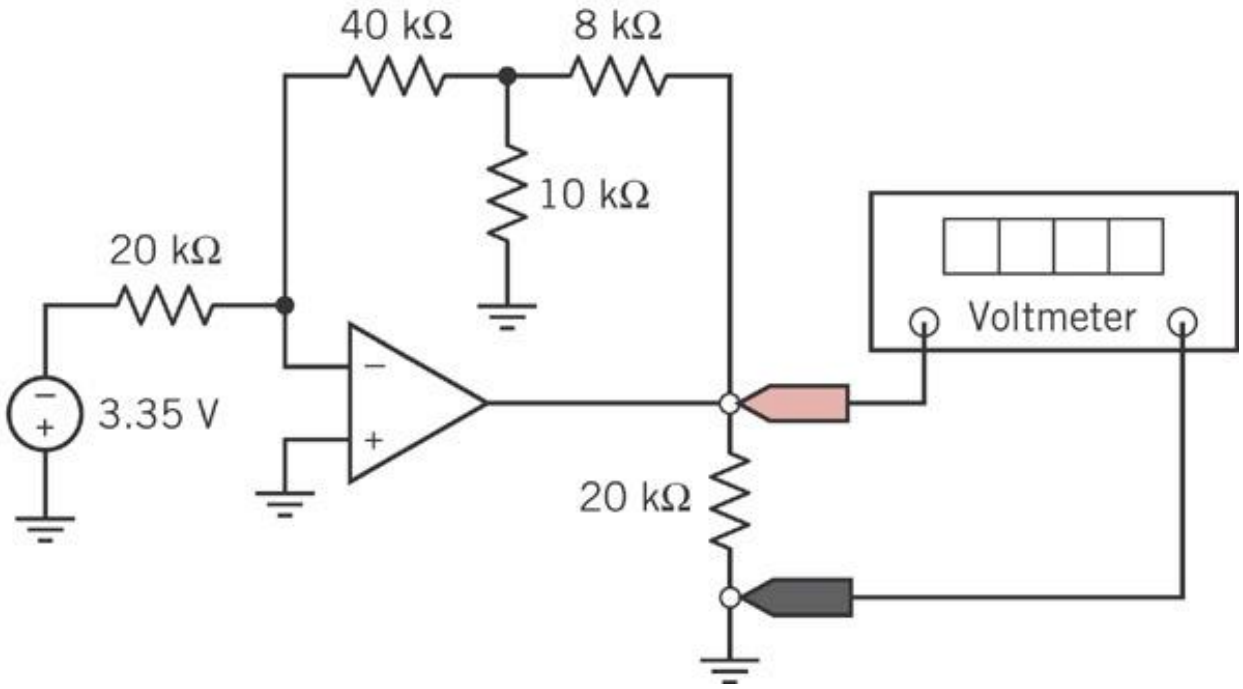
Using v_m =v4 and v_1=-4.55V gives the value of the voltmeter to be

$$v_m = -4.55 - 0.8 = -5.35\text{V}$$



Example 6.4-4 Analysis of an op amp circuit

- Consider the circuit shown in Figure 6.4-5. Find the value of the voltage measured by the voltmeter.



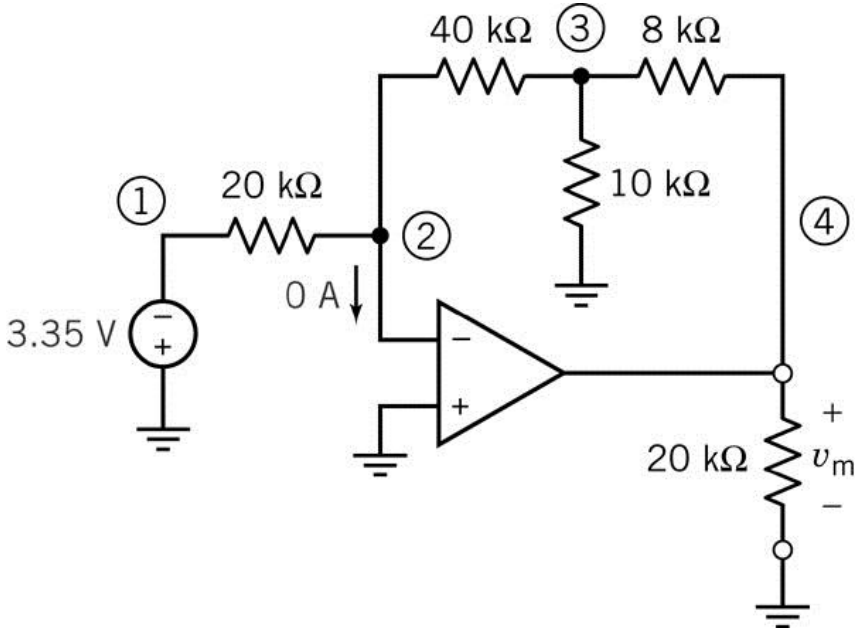
Solution

- The input to this circuit is the voltage of the voltage source. This input is related to the node voltages at the nodes of the voltage source by

$$0 - v_1 = 3.35 \quad \Rightarrow \quad v_1 = -3.35\text{V}$$

The output of this circuit is the voltage measured by the voltmeter. The output voltage is related to the node voltages by

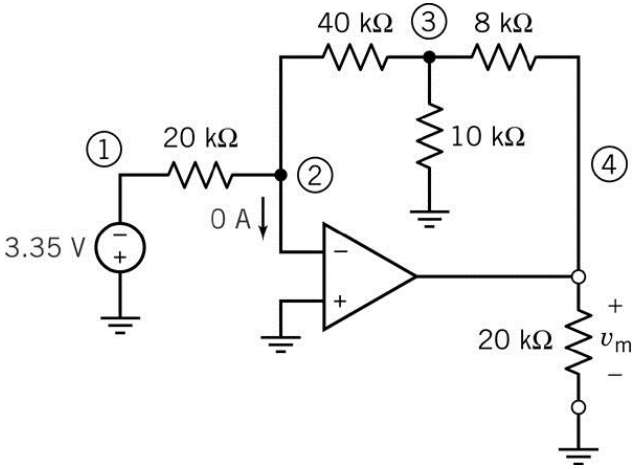
$$v_m = v_4 - 0 = v_4$$



Solution (cont'd)

- The noninverting input of the op amp is connected to the reference node. The node voltage at the inverting input of an ideal op amp is equal to the node voltage at the noninverting input. The inverting input of the op amp is connected to node 2. Consequently,

$$v_2 = 0\text{V}$$



Apply KCL to node 2 to get

$$\frac{v_1 - v_2}{20000} = 0 + \frac{v_2 - v_3}{40000} \quad \Rightarrow \quad v_3 = -2v_1 + 3v_2 = -2v_1$$

Apply KCL to node 3 to get

$$\frac{v_2 - v_3}{40000} = \frac{v_3}{10000} + \frac{v_3 - v_4}{8000} \quad \Rightarrow \quad 5v_4 = -v_2 + 10v_3 = 10v_3$$

Combining these equations gives

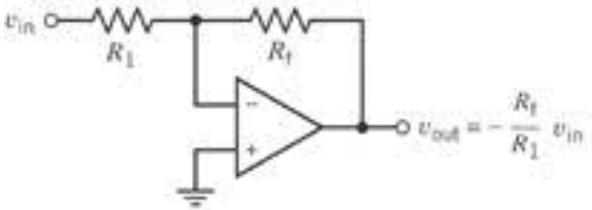
$$v_4 = 2v_3 = -4v_1$$

Using $v_m = v_4$ and v_1=-3.35V gives the value of the voltage measured by the voltmeter to be

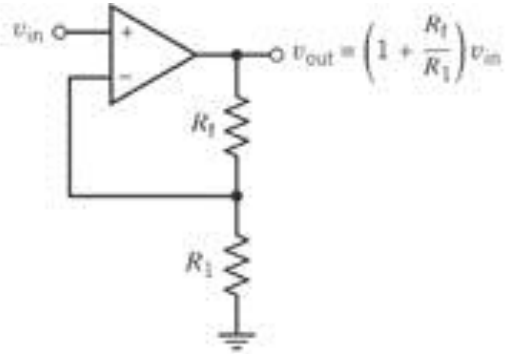
$$v_m = v - 4(-3.35) = 13.4\text{V}$$

Design using operational amplifiers

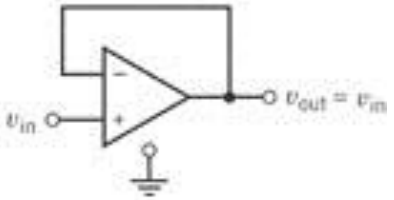
Fig. 6.5.1 A brief catalog of operational amplifier circuits.



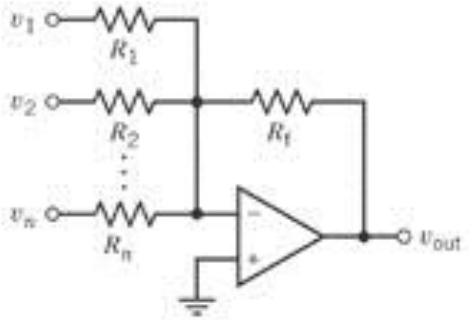
(a) Inverting amplifier



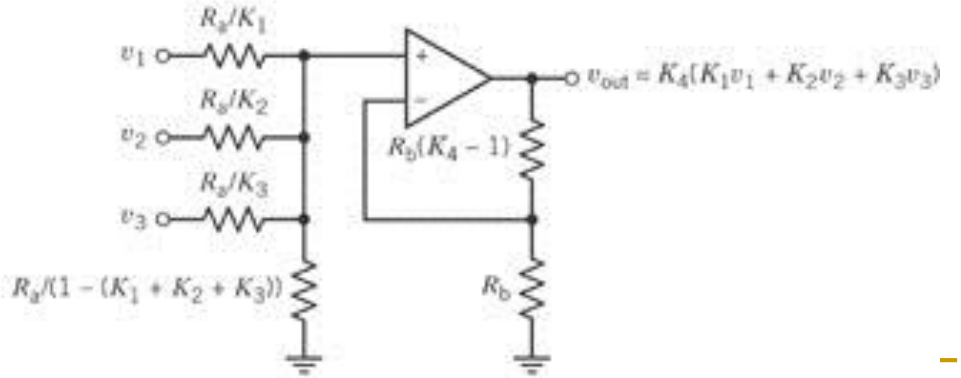
(b) Noninverting amplifier



(c) Voltage follower (buffer amplifier)



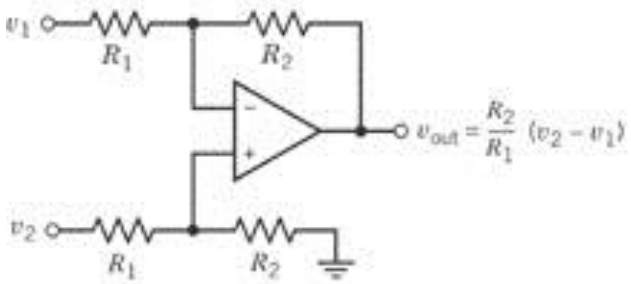
(d) Summing amplifier



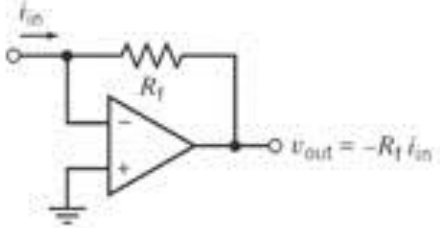
(e) Noninverting summing amplifier

Design using operational amplifiers

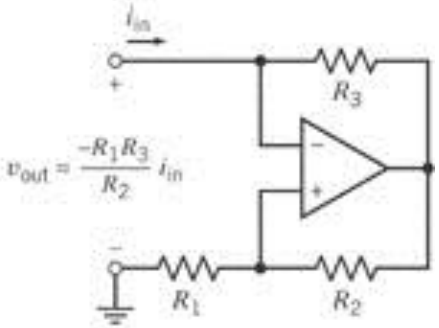
Figure 6.5–1 A brief catalog of operational amplifier circuits.



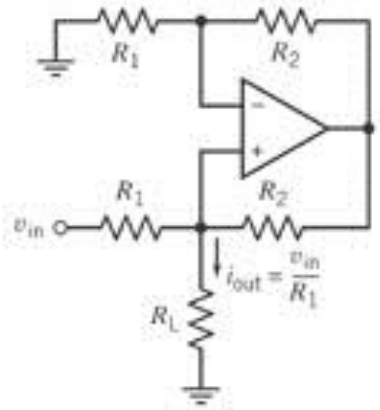
(f) Difference amplifier



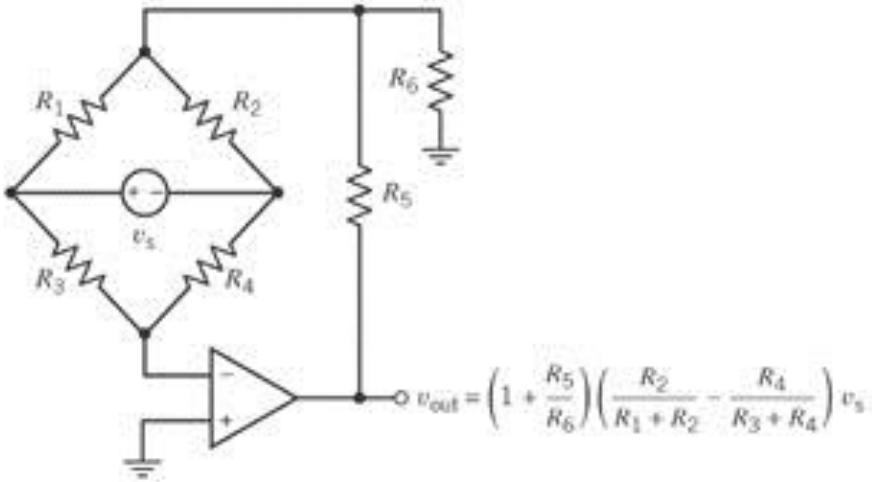
(g) Current-to-voltage converter



(h) Negative resistance convertor

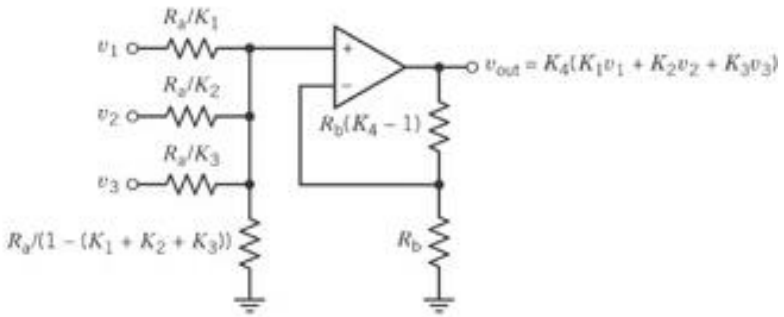


(i) Voltage-controlled current source (VCCS)

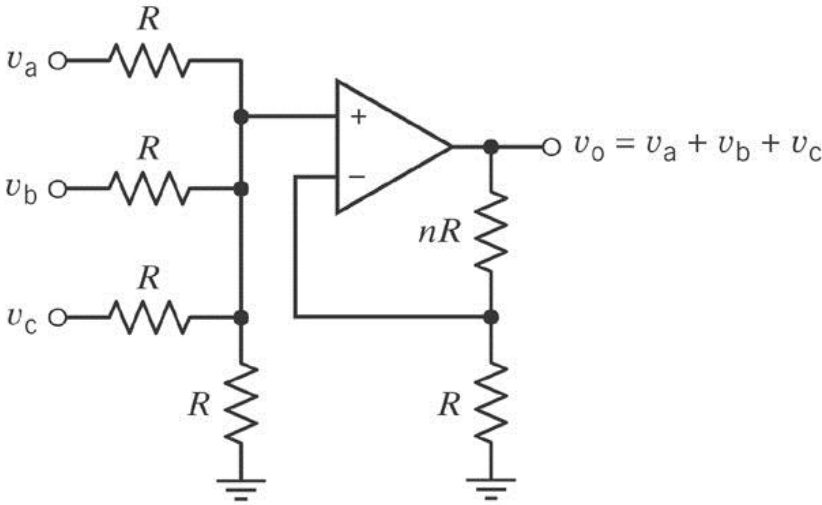


(j) Bridge amplifier

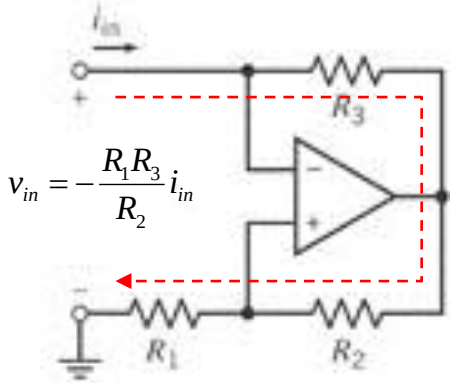
Design using operational amplifiers



(e) Noninverting summing amplifier

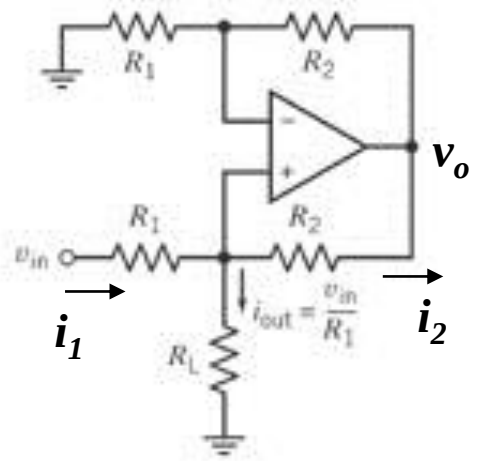


Design using operational amplifiers



$$v_{in} = -\frac{R_1 R_3}{R_2} i_{in}$$

(h) Negative resistance convertor



(i) Voltage-controlled current source (VCCS)

$$v_{in} - R_3 i_{in} - (R_1 + R_2) \cdot \frac{v_s}{R_1} = 0$$

$$v_{in}\left(1 - \frac{R_1 + R_2}{R_1}\right) = R_3 i_{in}$$

$$v_{in}\left(-\frac{R_2}{R_1}\right) = R_3 i_{in}$$

$$\therefore v_{in} = -\frac{R_1 R_3}{R_2} i_{in}$$

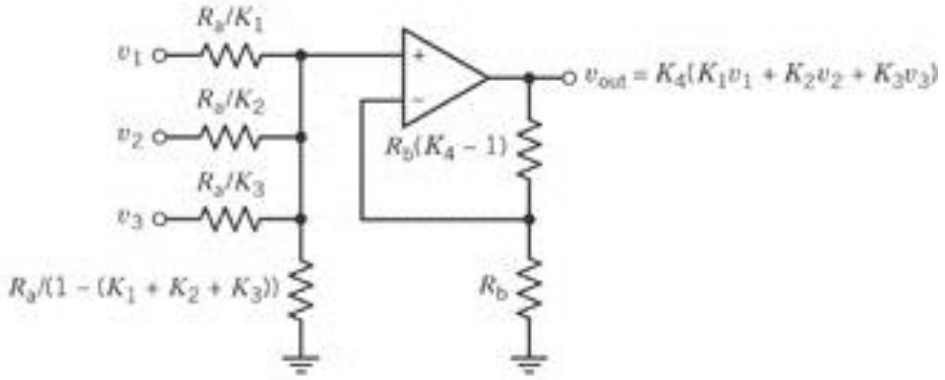
$$v^- = v^+ = \frac{v_o R_1}{R_1 + R_2}$$

$$i_2 = \frac{v^+ - v_o}{R_2} = \frac{-v_o}{R_1 + R_2}$$

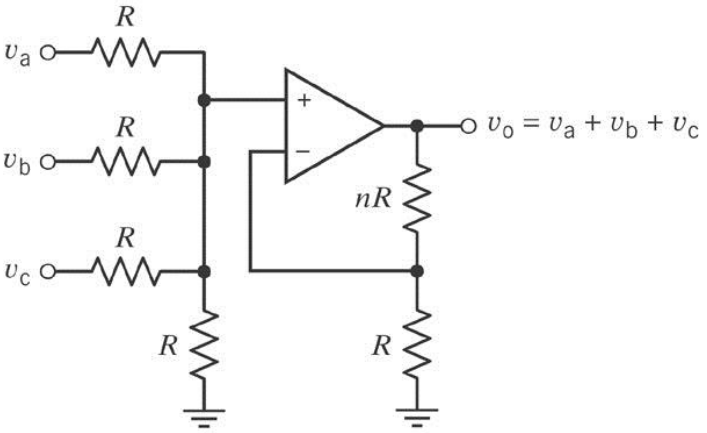
$$i_1 = \frac{v_{in} - v^+}{R_1} = \frac{v_{in}}{R_1} - \frac{v_o}{R_1 + R_2}$$

$$\therefore i_{out} = i_1 - i_2 = \left(\frac{v_{in}}{R_1} - \frac{v_o}{R_1 + R_2}\right) - \left(\frac{-v_o}{R_1 + R_2}\right) = \frac{v_{in}}{R_1}$$

Non inverting summing amplifiers



(c) Noninverting summing amplifier



(+)node에서 KCL:

$$\frac{(v_1 - v^+)K_1}{R_a} + \frac{(v_2 - v^+)K_2}{R_a} + \frac{(v_3 - v^+)K_3}{R_a} = \frac{v^+(1-(K_1+K_2+K_3)}{R_a}$$

$$\Rightarrow \quad v^+ = v_1K_1 + v_2K_2 + v_3K_3$$

$$v^- = v_{out} \cdot \frac{R_b}{R_bK_4} = \frac{v_{out}}{K_4}$$

$$\Rightarrow \quad v^+ = v^- \text{로부터}$$

$$\therefore v_{out} = K_4(v_1K_1 + v_2K_2 + v_3K_3)$$

(+)node에서 KCL:

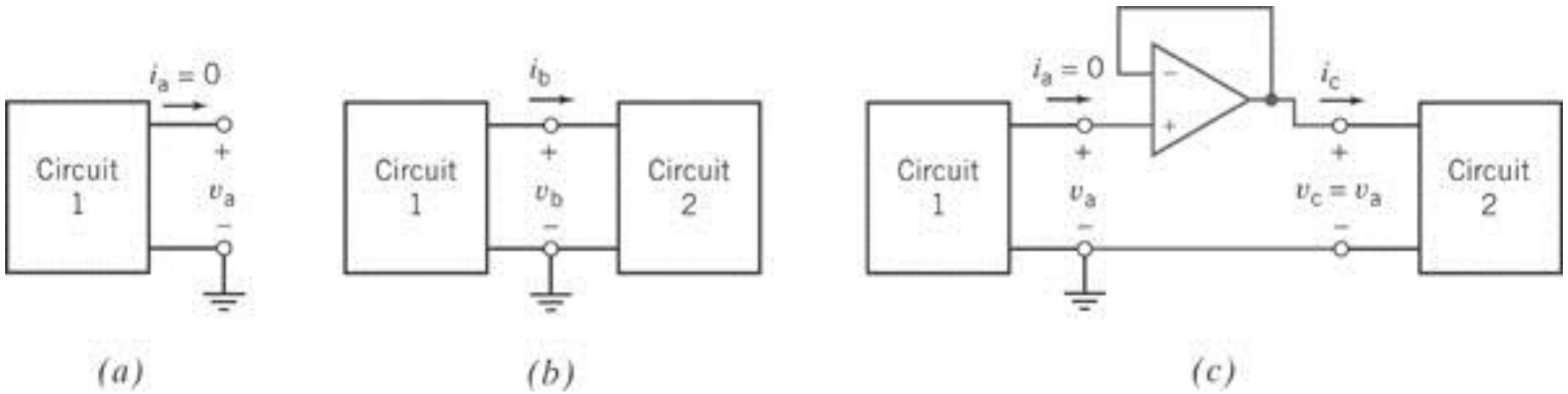
$$\frac{(v_a - v^+) + (v_b - v^+) + (v_c - v^+)}{R} = \frac{v^+}{R}$$

$$\Rightarrow \quad (n+1)v^+ = \sum_{n=1}^{N} v_i$$

$$\therefore v_o = \frac{1}{(n+1)} v^- = \sum_{n=1}^{N} v_i$$

Example 6.5-1 Preventing loading using a voltage follower

- This example illustrates the use of a voltage follower to prevent loading. The voltage follower is shown in Figure 6.5-1c. Loading can occur when two circuits are connected. Consider Figure 6.5-2. In Figure 6.5-2a the output of circuit 1 is the voltage v_a. In figure 6.5-2b, circuit 2 is connected to circuit 1. The output of circuit 1 is used as the input to circuit 2. Unfortunately, connecting circuit 2 to circuit 1 can change the output of circuit 1. This is called *loading*. Referring again to figure 6.5-2, circuit 2 is said to load circuit 1 if $v_b \neq v_a$. The current i_b is called the load current. Circuit 1 is required to provide this current in figure 6.5-2b but not in figure 6.5-2a. This is the cause of the loading .The load current can be eliminated using a voltage follower as shown in figure 6.5-2c. The voltage follower copies voltage v_a from the output of circuit 1 to the input of circuit 2 without disturbing circuit 1.



Solution

- As a specific example, consider Figure 6.5-3. The voltage divider shown in Figure 6.5-3a can be analyzed by writing a node equation at node 1.

$$\frac{v_a - v_{in}}{20000} + \frac{v_a}{60000} = 0$$

Solving for v_a, we have

$$v_a = \frac{3}{4} v_{in}$$

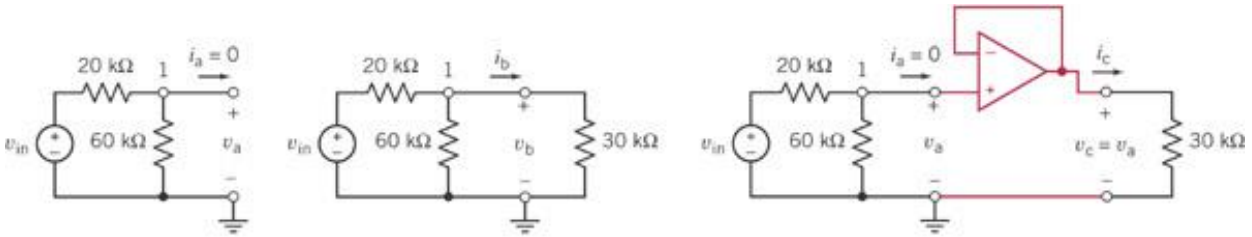
In Figure 6.5-3b, a resistor is connected across the output of the voltage divider. This circuit can be analyzed by writing a node equation at node 1:

$$\frac{v_b - v_{in}}{20000} + \frac{v_b}{60000} + \frac{v_b}{30000} = 0$$

Solving for v_b, we have

$$v_b = \frac{1}{2} v_{in}$$

Since $v_b \neq v_a$, connecting the resistor directly to the voltage divider loads the voltage divider. This loading is caused by the current required by the 30kΩ resistor. Without the voltage follower, the voltage divider must provide this current.



Solution (cont'd)

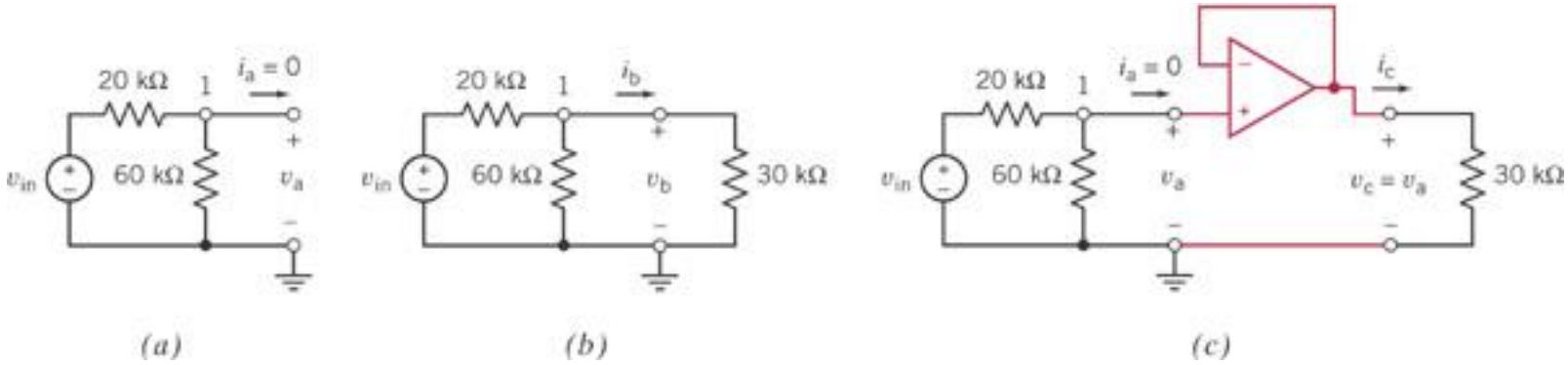
- In Figure 6.5-3c, a voltage follower is used to connect the 30kΩ resistor to the output of the voltage divider. Once again, the circuit can be analyzed by writing a node equation at node 1.

$$\frac{v_c - v_{in}}{20000} + \frac{v_c}{60000} = 0$$

Solving for v_c, we have

$$v_c = \frac{3}{4} v_{in}$$

Since vc=va, loading is avoided when the voltage follower is used to connect the resistor to the voltage divider. The voltage follower, not the voltage divider, provides the current required by the 30kΩ resistor.



Example 6.5-2 Amplifier Design

- A common application of operational amplifiers is to scale a voltage, that is, to multiply a voltage by a constant, K, so that

$$v_0 = Kv_{in}$$

This situation is illustrated in figure 6.5-4a. The input voltage, v_{in}, is provided by an ideal voltage source. The output voltage, v_o, is the element voltage of a 100kΩ resistor. This resistor, sometimes called a load resistor, represents the circuit that will use the voltage v_o as its input.

Circuits that perform this operation are usually called amplifiers. The constant K is called the gain of the amplifier.

The required value of the constant K will determine which of the circuits is selected from figure 6.5-1. There are four cases to consider:

$$K < 0, \quad K > 1, \quad K = 1, \quad \text{and} \quad 0 < K < 1$$

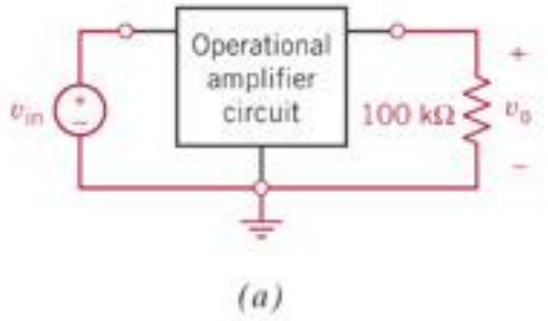


Fig. 6.5-4(a)

Solution

- Since resistor values are positive, the gain of the inverting amplifier, shown in Figure 6.5-1a, is negative. Accordingly, when K<0 is required, an inverting amplifier is used. For example, suppose we require K=-5. Form Figure 6.5-1a

$$-5 = -\frac{R_f}{R_1}$$

so

$$R_f = 5R_1$$

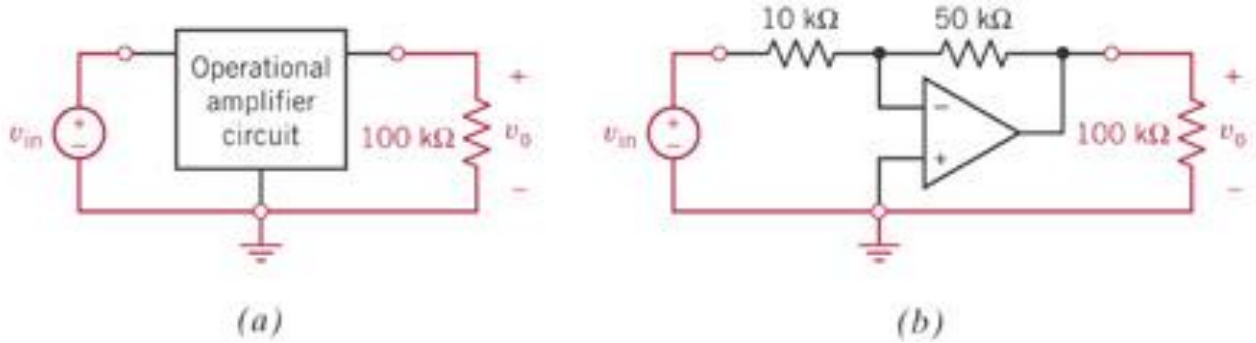
As a rule of thumb, is a good idea to choose resistors in operational amplifier circuits that have values between 5kΩ and 500kΩ when possible. Choosing

$$R_1 = 10k\Omega$$

gives

$$R_f = 50k\Omega$$

The resulting circuit is shown in Figure 6.5-4b



Solution (cont'd)

- Next, suppose we require K=5. The noninverting amplifier, shown in Figure 6.5-1b, is used to obtain gains greater than 1. From Figure 6.5-1b

$$5 = 1 + \frac{R_f}{R_1}$$

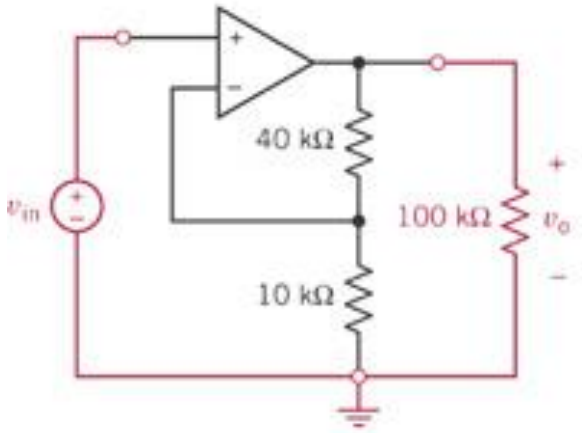
so

$$R_f = 4R_1$$

Choosing R_1=10kΩ gives R_f =40kΩ. The resulting circuit is shown in Figure 6.5-4c.

$$R_1 = 10k\Omega$$

$$R_f = 40k\Omega$$



(c)

Solution (cont'd)

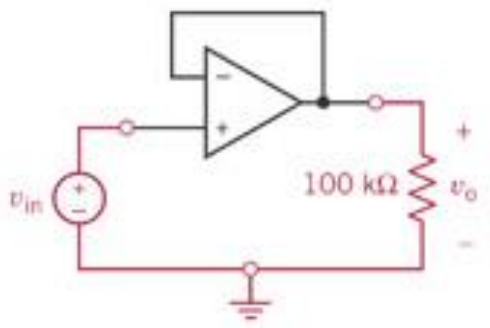
- Consider using the noninverting amplifier of Figure 6.5-1b to obtain a gain K=1. Figure 6.5-1b

$$1 = 1 + \frac{R_f}{R_1}$$

so

$$\frac{R_f}{R_1} = 0$$

This can be accomplished by replacing R_f by a short circuit (R_f=0) or by replacing R_1 by an open circuit (R_1=∞) or both. Doing both converts a noninverting amplifier into a voltage follower. The gain of the voltage follower is 1. In Figure 6.5-4d a voltage follower is used for the case K=1.



(d)

Solution (cont'd)

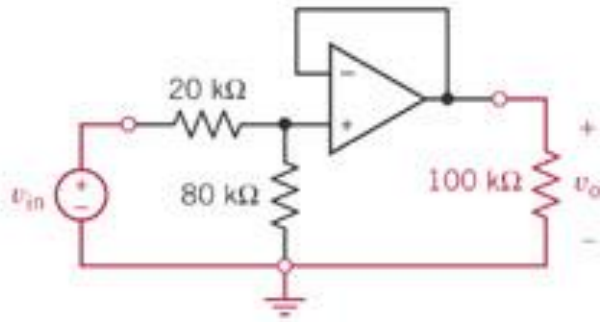
- There is no amplifier in Figure 6.5-1 that has a gain between 0 and 1. Such a circuit can be obtained using a voltage divider together with a voltage follower. Suppose we require K=0.8. First, design a voltage divider to gave an attenuation equal to K:

$$0.8 = \frac{R_2}{R_1 + R_2}$$

so

$$R_2 = 4 \cdot R_1$$

Choose R_1=20kΩ gives R_2=80kΩ. Adding a voltage follower fives the circuit shown in Figure 6.5-4e



(e)

Example 6.5-3 Designing a noninverting summing amplifier

- Design a circuit having one output, vo, and three inputs, v_1, v_2, and v_3. The output must be related to the inputs by

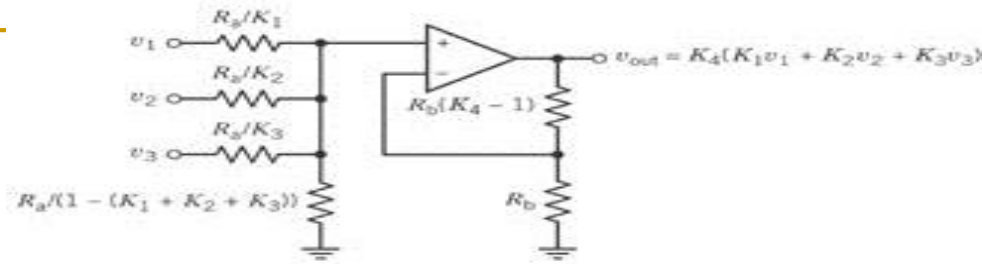
$$v_o = 2v_1 + 3v_2 + 4v_3$$

In addition, the inputs are restricted to having values between -1V and 1V, that is,

$$|v_i| \le 1\text{V} \quad i = 1,2,3$$

Consider using an operational amplifier having i_{sat} =2mA and v_{sat} =15V, and design the circuit.

Solution



- Designing the noninverting summer amounts to choosing values for these six parameters. (K_1, K_2, K_3, K_4, R_a, R_b) Notice that $K_1+K_2+K_3<1$ is required to ensure that all of the resistors have positive values. Pick $K_4=10$. Then

$$v_o = 2v_1 + 3v_2 + 4v_3 = 10(0.2v_1 + 0.3v_2 + 0.4v_3)$$

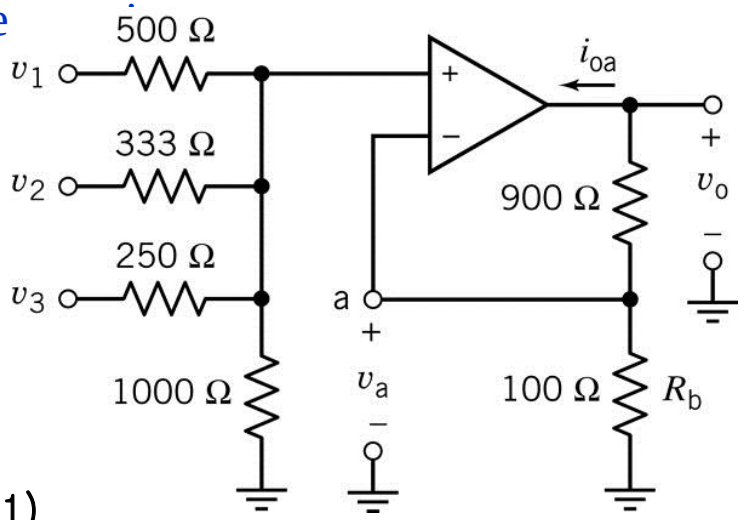
That is, $K_4=10$, $K_1=0.2$, $K_2=0.3$ and $K_3=0.4$. Figure 6.5-1e does not provide much guidance is picking values of R_a and R_b. Try $R_a=R_b=100\Omega$. Then

$$(K_4-1)R_b = (10-1)100 = 900\Omega$$

Figure 6.5-5 shows the resulting circuit. It is necessary to check this circuit to ensure that it satisfies the specifications. Writing node

$$\frac{v_a - v_1}{500} + \frac{v_a - v_2}{333} + \frac{v_a - v_3}{250} + \frac{v_a}{1000} = 0$$

$$-\frac{v_o - v_a}{900} + \frac{v_a}{100} = 0$$



and solving these equations yield

$$v_o = 2v_1 + 3v_2 + 4v_3, \quad v_a = \frac{v_o}{10}$$

The output current

$$i_{oa} = \frac{v_a - v_o}{900} = -\frac{v_o}{1000} \qquad (6.5\text{-}1)$$

Solution (cont'd)

- How large can the output voltage be? We know that

$$|v_o| = |2v_1 + 3v_2 + 4v_3|$$

so

$$|v_o| \le 2|v_1| + 3|v_2| + 4|v_3| \le 9\text{V}$$

The operational amplifier output voltage will always be less than v_{sat}. That's good. Now what about the output current? Notice that $|v_o| \le 9$V. From Eq. 6.5-1

$$|i_{oa}| = \left|\frac{-v_o}{1000\Omega}\right| \le \left|\frac{-9\text{V}}{1000\Omega}\right| = 9\text{mA}$$

The operational amplifier output current exceeds i_{sat} =2mA. This is not allowed. Increasing Rb will reduce i_o. Try R_b=1000Ω. Then

$$(K_4 - 1)R_b = (10 - 1)1000 = 9000\Omega$$

Solution (cont'd)

- This produces the circuit shown in Figure 6.5-6. Increasing Ra and Rb does not change the operational amplifier output voltage. As before

$$|v_o| \le 2|v_1| + 3|v_2| + 4|v_3| \le 9\text{V}$$

Increasing Ra and Rb does reduce the operational amplifier output current. Now

$$|i_{oa}| = \left|\frac{-v_o}{K_4 R_b}\right| \le \left|\frac{-9\text{V}}{10000\Omega}\right| = 0.9\text{mA}$$

so $|i_{oa}|<2$mA and $|v_o|<15$V, as required

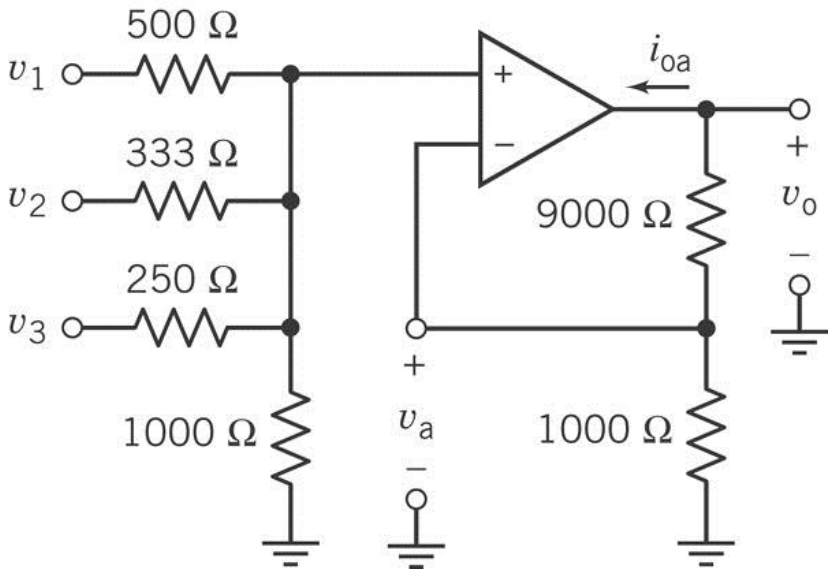


Figure 6.5-6

Operational amplifier circuits and linear algebraic equations

- This section describes a procedure for designing op-amp circuit to implement linear algebraic equations. Some of the node voltages of the op-amp circuit will represent the variables in the algebraic equation.
- For example, the equation

$$z = 4x - 5y + 2 \qquad (6.6\text{-}1)$$

will be represented by an op-amp circuit that has node voltages v_x, v_y, v_z that are related by the equation

$$v_z = 4v_x - 5v_y + 2$$

- The design procedure has two steps
  1. To represent the equation by a diagram called a block diagram.
  2. To implement each block of the block diagram as an op-amp circuit.

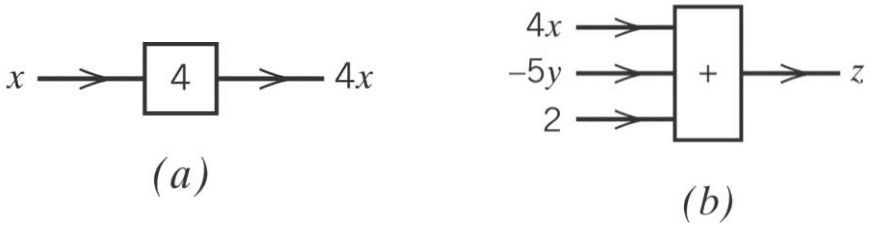
Operational amplifier circuits and linear algebraic equations

- Eq. 6.6-1 can be rewritten as

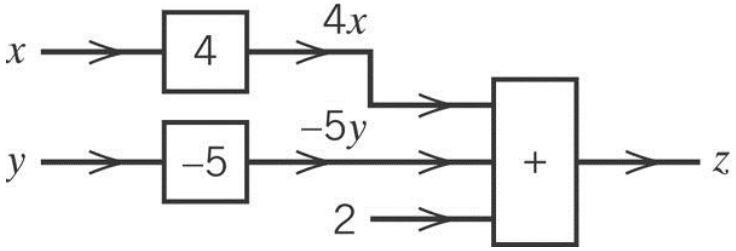
$$z = 4x + (-5)y + 2 \qquad (6.6\text{–}3)$$

that indicates that z can be obtained from z and y using only addition and multiplication, through one of the multiplier is now negative.

- Figure 6.6-1 shows symbolic representations of the operations of (a) multiplication by a constant and (b) addition.



- Figure 6.6-2 shows a block diagram representing the Eq. 6.6-3



Operational amplifier circuits and linear algebraic equations

- The block in Figure 6.6-3a requires multiplication by a positive constant, 4.
- Figure 6.6-3b shows the corresponding op-amp circuit, a noninverting amplifier having a gain equal to 4.
- This noninverting amplifier is designed by referring to Figure 6.5-1b and setting

$$R_1 = 20\ \text{k}\Omega \quad \text{and} \quad R_f = 3R_1 = 60\ \text{k}\Omega$$

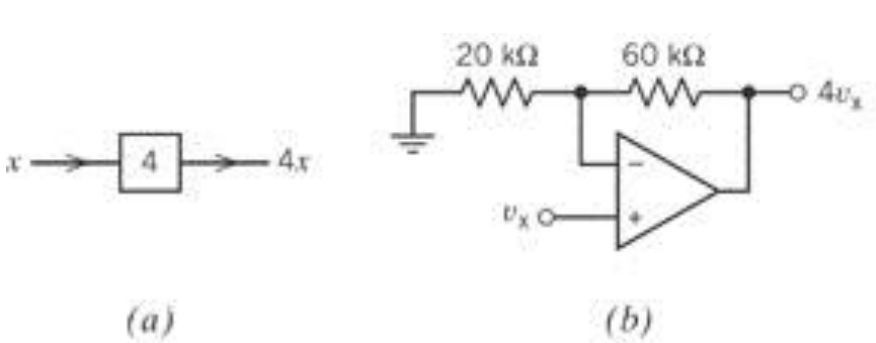


Figure 6.6-3a,b

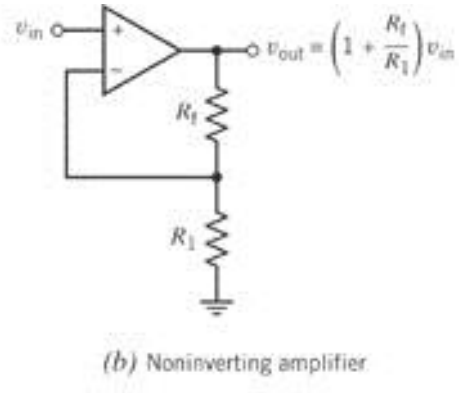


Figure 6.5-1b

Operational amplifier circuits and linear algebraic equations

- The block in Figure 6.6-3c requires multiplication by a negative constant, -5.
- Figure 6.6-3d shows the corresponding op-amp circuit, a inverting amplifier having a gain equal to -5.
- This noninverting amplifier is designed by referring to Figure 6.5-1a and setting

$$R_1 = 20\ \text{k}\Omega \quad \text{and} \quad R_f = 5R_1 = 100\ \text{k}\Omega$$

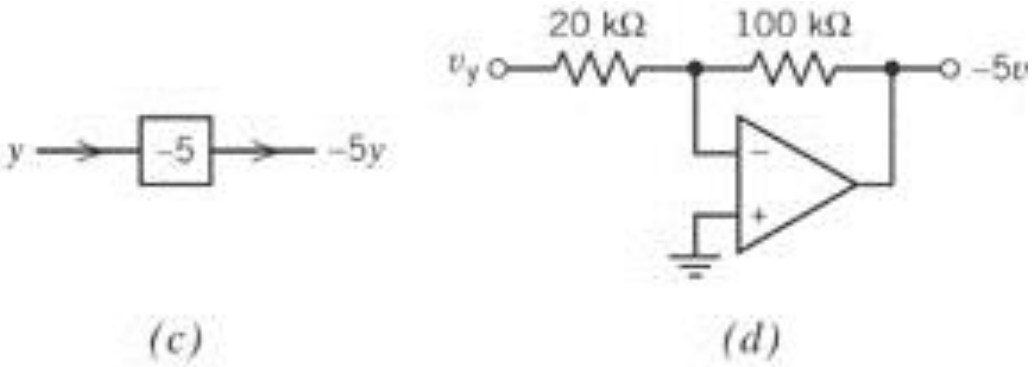


Figure 6.6-3c,d

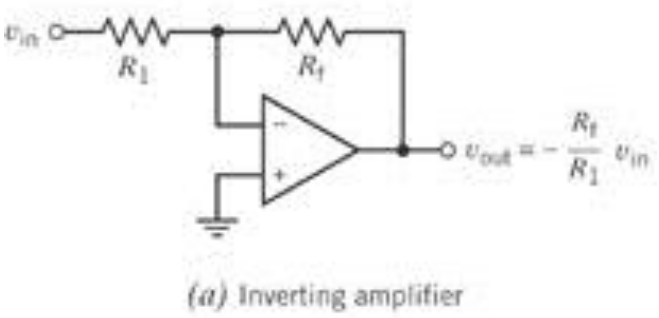


Figure 6.5-1a

Operational amplifier circuits and linear algebraic equations

- The block in Figure 6.6-3e requires adding the three terms.
- Figure 6.6-3f shows the corresponding op-amp circuit, a noninverting summer.
- This noninverting summer is designed by referring to Figure 6.6-4 and setting

$$R = 20\ \text{k}\Omega, \quad n = 3, \quad \text{and} \quad nR = 3(20,000) = 60\ \text{k}\Omega$$

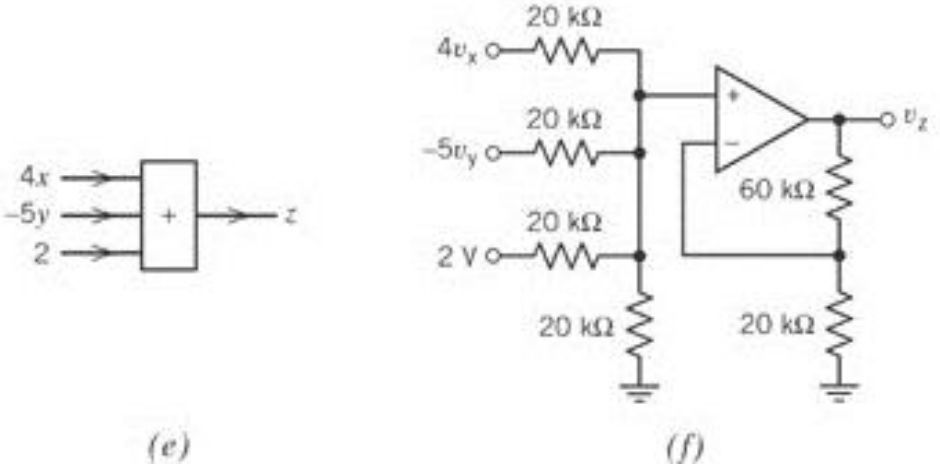


Figure 6.6−3e,f

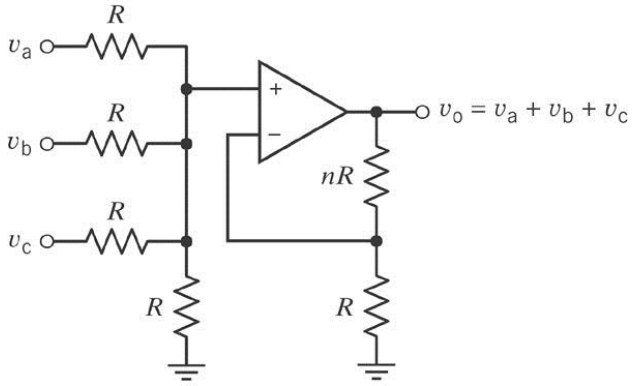


Figure 6.6−4

Operational amplifier circuits and linear algebraic equations

- Figure 6.6-5 shows the circuit obtained by replacing each block in Figure 6.6-2 by the corresponding op-amp circuit from Figure 6.6-3

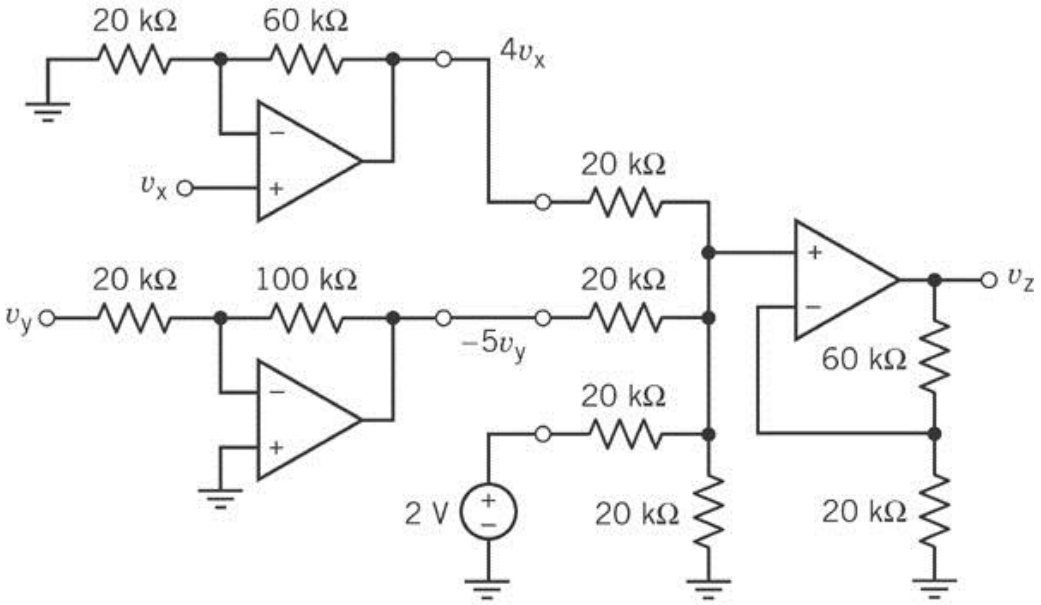


Figure 6.6–5

- The circuit does indeed implement Eq. 6.6-3, but it's possible to improve this circuit. (having 2V source is expensive.)

Operational amplifier circuits and linear algebraic equations

- The constant input to the summer has been implements using -2V voltage source. Voltage sources are relatively expensive devices, considerably more expensive than resistors or op amps.
- We can reduce the cost by using the op amp power supply ($\pm$15V)

Apply the voltage division rule in Figure 6.6-6 requires that

$$\frac{R_b}{R_a + R_b} = \frac{2}{15} = 0.133 \quad \Rightarrow \quad R_a = 6.5R_b$$

One solution is

$$R_a = 130\ \text{k}\Omega \quad \text{and} \quad R_b = 20\ \text{k}\Omega$$

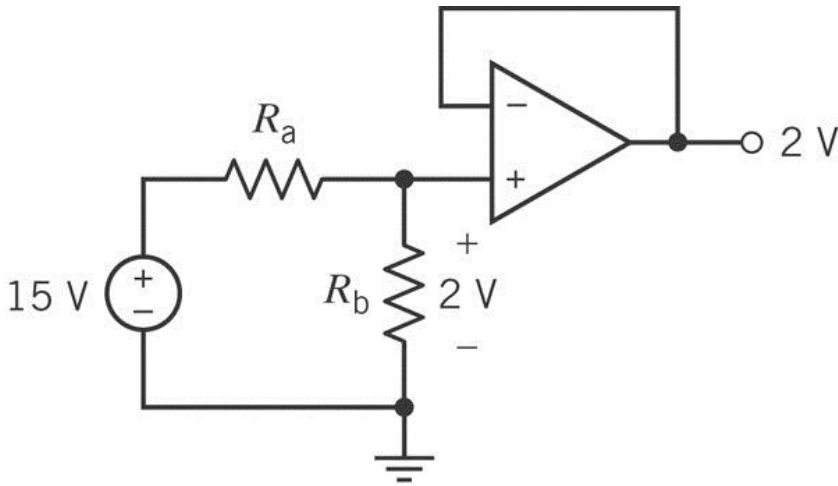


Figure 6.6-6

Operational amplifier circuits and linear algebraic equations

- Figure 6.7-7 shows the improved op-amp circuit.
- We can verify, perhaps by writing node equations, that $v_z = 4v_x - 5v_y + 2$

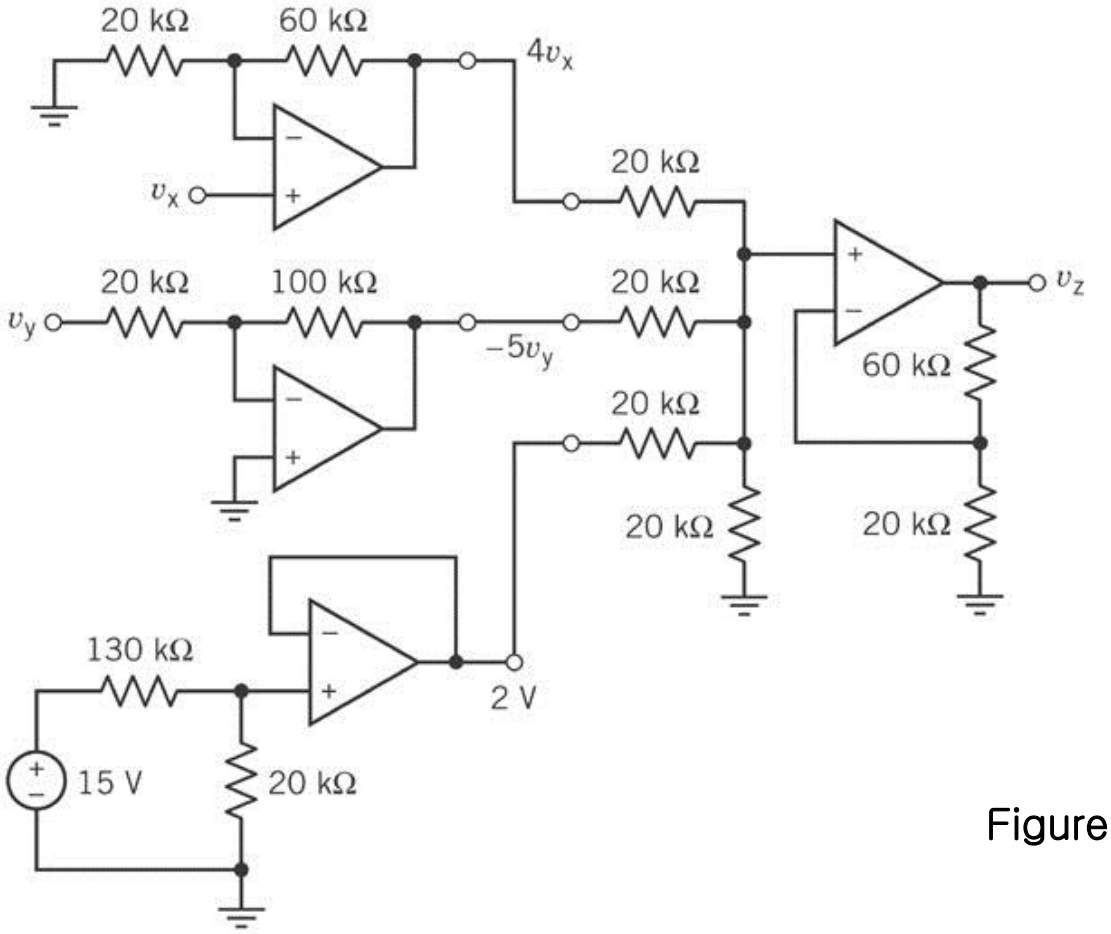


Figure 6.6−7

Operational amplifier circuits and linear algebraic equations

- The output voltage of an op-amp is restricted by $|v_0| \le v_{sat}$
  v_{sat} is approximately 15V when $\pm$15V voltage sources are used to bias the op-amp.
  $4v_c$, $-5v_y$, v_z are each output voltage of one of the op-amps.

$$|v_x| \le \frac{v_{sat}}{4} \approx \frac{15}{4} = 3.75 \text{ V}, \quad |v_y| \le \frac{v_{sat}}{5} \approx \frac{15}{5} = 3 \text{ V} \quad \text{and} \quad |v_z| \le v_{sat} \approx 15 = 15 \text{ V}$$

- The simple encoding of $v_x = x,\ v_y = y$ and $v_z = z$ gives

$$|x| \le 3.75, \quad |y| \le 3 \quad \text{and} \quad |z| \le 15$$

- Should these conditions be too restrictive, consider defining the relationship between the signals and the variables. For example, the encoding of $v_x = \frac{x}{10},\ v_y = \frac{y}{10}$ and $v_z = \frac{z}{10}$ gives

$$|x| \le 37.5, \quad |y| \le 30 \quad \text{and} \quad |z| \le 150$$

Practical Operational Amplifiers

Characteristics of practical operational amplifiers

- Consider the op-amp shown in Figure 6.7-1a. If this operational amplifier is ideal, then

$$i_1 = 0,\ \ i_2 = 0 \ \text{ and } \ v_1 - v_2 = 0$$

- In contrast Figure 6.7-1d accounts for several non-ideal parameters of practical op-amp, namely:
  - Nonzero bias currents
  - Nonzero input offset voltage
  - Finite input resistance
  - Nonzero output resistance
  - Finite voltage gain

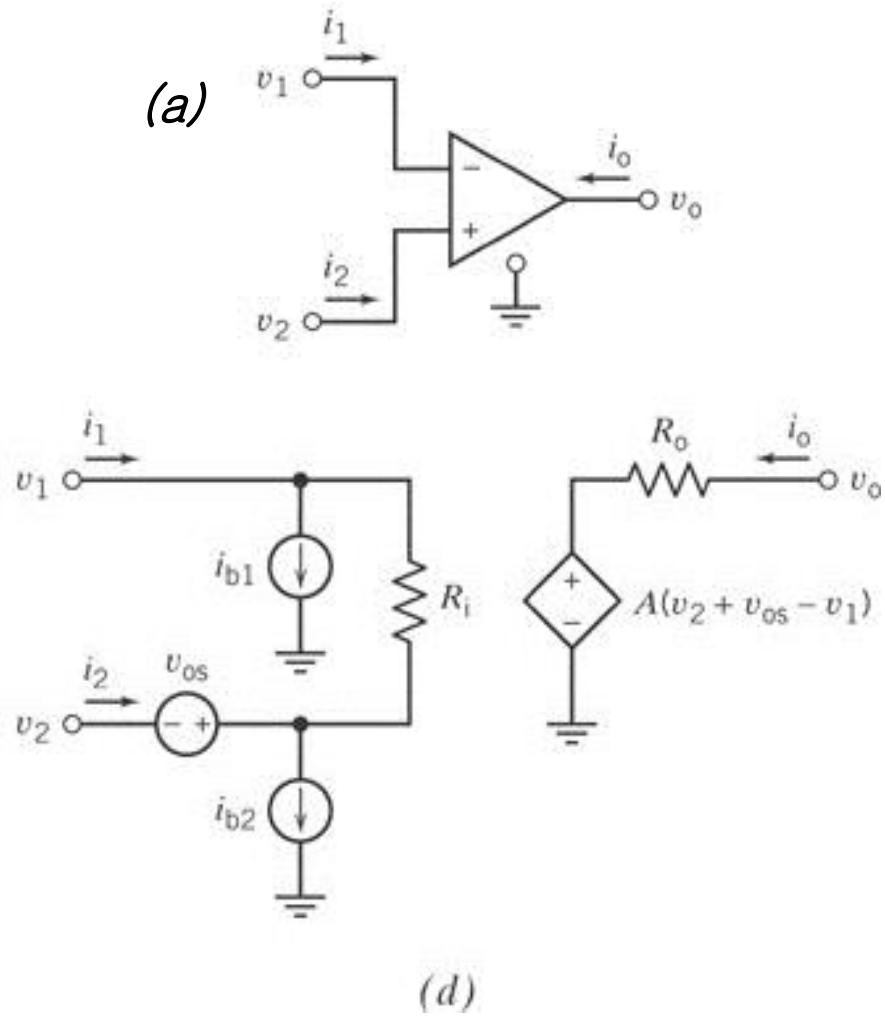


Figure 6.7-1

Characteristics of practical operational amplifiers

- The more accurate model of Figure 6.8-1d is much more complicated and much more difficult to use than the ideal op-amp.
- Figure 6.7-1b and 6.7-1c provide a compromise.

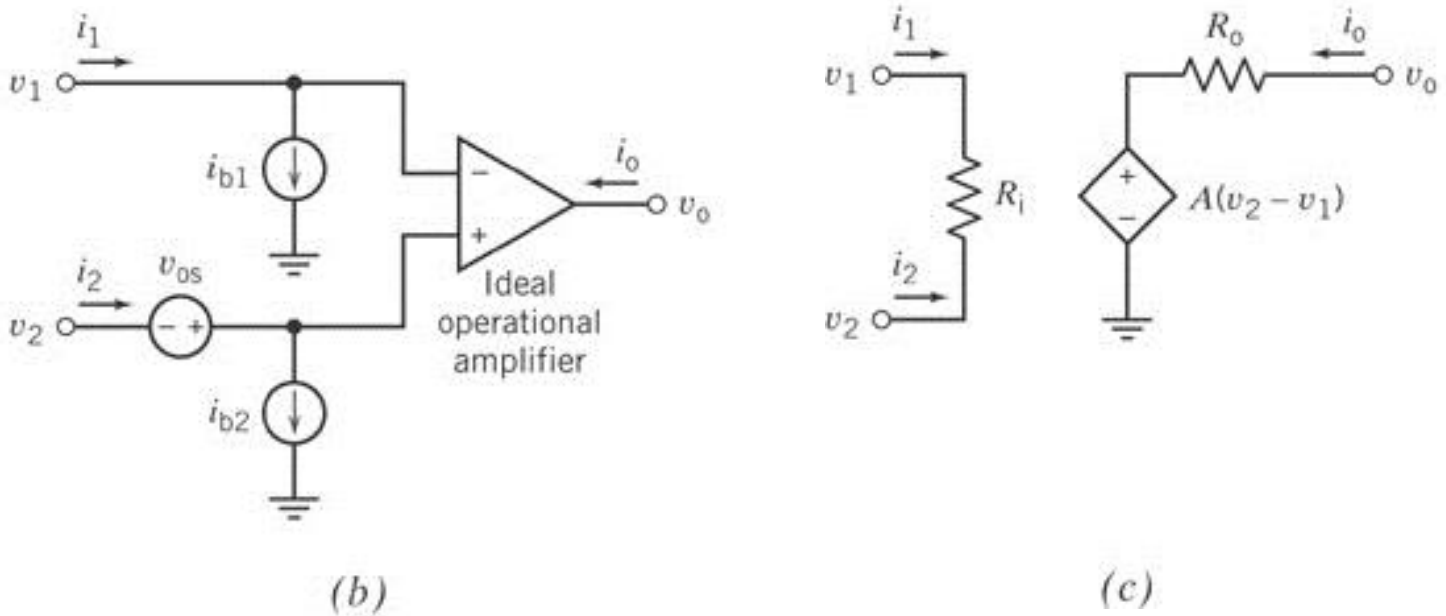


Figure 6.7−1

Characteristics of practical operational amplifiers

- The op-amp model shown in Figure 6.7-1b accounts for
  - Nonzero bias currents
  - Nonzero input offset voltage

- The offset model is represented by these equations.

$$i_1 = i_{b1},\ i_2 = i_{b2} \ \text{ and } \ v_1 - v_2 = v_{os}$$

The difference between the bias current is called the input offset current of the amp:

$$i_{os} = i_{b1} - i_{b2}$$

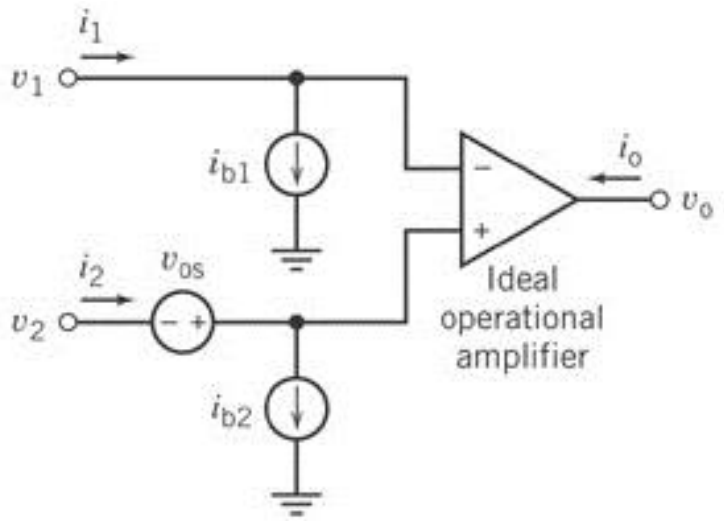


Figure 6.7-1 (b)

- If bias currents (i_{b1} and i_{b2}) and input offset voltage (v_{os}) are all zero, the offset model reverts to the ideal operational amplifier.

Characteristics of practical operational amplifiers

- Manufacturer specify a maximum value for the bias currents, the input offset current, and the output offset voltage.

- For example, the specifications of the uA741 guarantee that

$$|i_{b1}| \le 500 \text{ nA} \quad \text{and} \quad |i_{b2}| \le 500 \text{ nA}$$
$$|i_{b1} - i_{b2}| \le 200 \text{ nA}$$
$$|v_{os}| \le 5 \text{ mV}$$

Characteristics of practical operational amplifiers

- The op-amp model shown in Figure 6.7-1c accounts for
  - Finite input resistance
  - Nonzero output resistance
  - Finite voltage gain

- The finite gain model consist of two resistors and a VCVS.

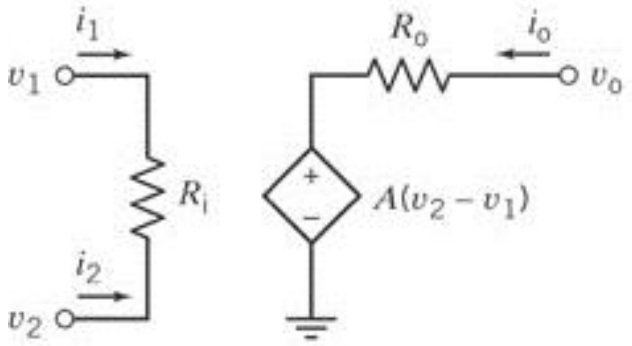


Figure 6.7-1 (c)

$$v_0 = A(v_2 - v_1) + R_0 i_0$$

so $$v_2 - v_1 = \frac{v_0 - R_0 i_0}{A}$$

Characteristics of practical operational amplifiers

- The finite gain model reverts to the ideal op-amp when the gain, A, becomes infinite.Since

$$|v_o| \le v_{sat} \quad \text{and} \quad |i_o| \le i_{sat}$$

Then $$v_2 - v_1 = \frac{v_0 - R_0 i_0}{A} \le \frac{v_{sat} + R_0 i_{sat}}{A}$$

Therefore, $$\lim_{A\to\infty}(v_2 - v_1) = 0$$

Next, since $$i_1 = -\frac{v_2 - v_1}{R_i} \quad \text{and} \quad i_2 = \frac{v_2 - v_1}{R_i}$$

We conclude that $$\lim_{A\to\infty} i_1 = 0 \quad \text{and} \quad \lim_{A\to\infty} i_2 = 0$$

- The gain for practical op-amps ranges from 10^5 to 10^7

Characteristics of practical operational amplifiers

- Table 6.7-1 show the bias currents, offset current, and input offset voltage typical of several types of op-amp.

Table 6.7-1 Selected Parameters of Typical Operational Amplifiers

Parameter	Units	uA741	LF351	TL051C	OPA101AM	OP-07E
Saturation voltage, v_{sat}	V	13	13.5	13.2	13	13
Saturation current, i_{sat}	mA	2	15	6	30	6
Slew rate, SR	V/us	0.5	13	23.7	6.5	0.17
Bias current, i_b	nA	80	0.05	0.03	0.012	1.2
Offset current, i_{os}	nA	20	0.025	0.025	0.003	0.5
Input offset voltage, v_{os}	mV	1	5	0.59	0.1	0.03
Input resistance, R_i	MΩ	2	10^6	10^6	10^6	50
Output resistance, R_o	Ω	75	1000	250	500	60
Differential gain, A	V/mV	200	100	105	178	5000
Common mode rejection ratio, CMRR	V/mV	31.6	100	44	178	1413
Gain bandwidth product, B	MHz	1	4	3.1	20	0.6

Characteristics of practical operational amplifiers

- Table 6.7-1 lists two other parameters of practical op-amp that have not yet been mentioned. They are the *common mode rejection ratio* (CMRR) and the gain band width product.
- Consider first the common mode rejection ratio.
  In the finite gain model, the voltage of the VCVS is

$$A(v_2 - v_1)$$

  In practice, the voltage is more accurately expressed as

$$A(v_2 - v_1) + A_{cm}\left(\frac{v_1 + v_2}{2}\right)$$

  where $v_2 - v_1$ is called the differential input voltage

  $\frac{v_1 + v_2}{2}$ is called the common mode input voltage

  and A_{cm} is called the common mode gain

Characteristics of practical operational amplifiers

- The gain A is sometimes called the differential gain to distinguish it form A_{cm}.
- The common mode rejection ratio is defined to be the ratio of A and A_{cm}.

$$\text{CMRR} = \frac{A}{A_{cm}}$$

- The dependent source voltage can be expressed using A and CMRR as

$$A(v_2 - v_1) + A_{cm}\left(\frac{v_1 + v_2}{2}\right) = A(v_2 - v_1) + \frac{A}{\text{CMRR}}\left(\frac{v_1 + v_2}{2}\right)$$

$$= A\left[\left(1 + \frac{1}{2\text{CMRR}}\right)v_2 - \left(1 - \frac{1}{2\text{CMRR}}\right)v_1\right]$$

CMRR can be added to the finite gain model. However, in most cases, negligible error is caused by ignoring the CMRR.

Characteristics of practical operational amplifiers

- Next, we consider the gain bandwidth product.
  Suppose

$$v_1 = 0 \quad \text{and} \quad v_2 = M \sin \omega t$$

  so that

$$v_2 - v_1 = M \sin \omega t$$

  The voltage of the dependent source in the finite gain model will be

$$A(v_2 - v_1) = A \cdot M \sin \omega t$$

  Practical op-amp do not work this way. The gain of a practical op-amp is a function of frequency, say A(ω). For many practical op-amps, A(ω) can be adequately represented as

$$A(\omega) = \frac{B}{j\omega}$$

  The parameter B is used to describe the dependence of the op-amp gain on frequency. The parameter B is called the gain bandwidth product of the op-amp.

Example 6.7-1 Offset voltage and bias currents

- The inverting amplifier shown in Figure 6.7-2a contains a uA741 operational amplifier. This inverting amplifier designed in Example 6.5-2 has a gain of -5, that is

$$v_0 = -5 \cdot v_{in}$$

The design of the inverting amplifier is based on the ideal model of an operational amplifier and so did not account for the bias currents and input offset voltage of the uA741 operational amplifier. In this example, the offsets model of an operational amplifier will be used to analyze the circuit. This analysis tell us what effect the bias currents and input offset voltage have on the performance of this circuit.

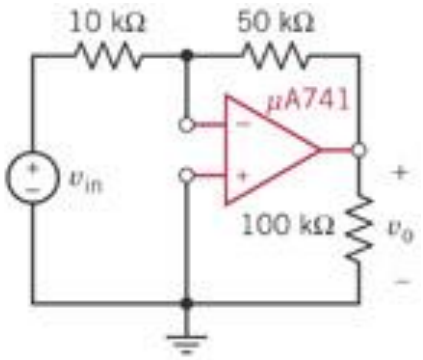
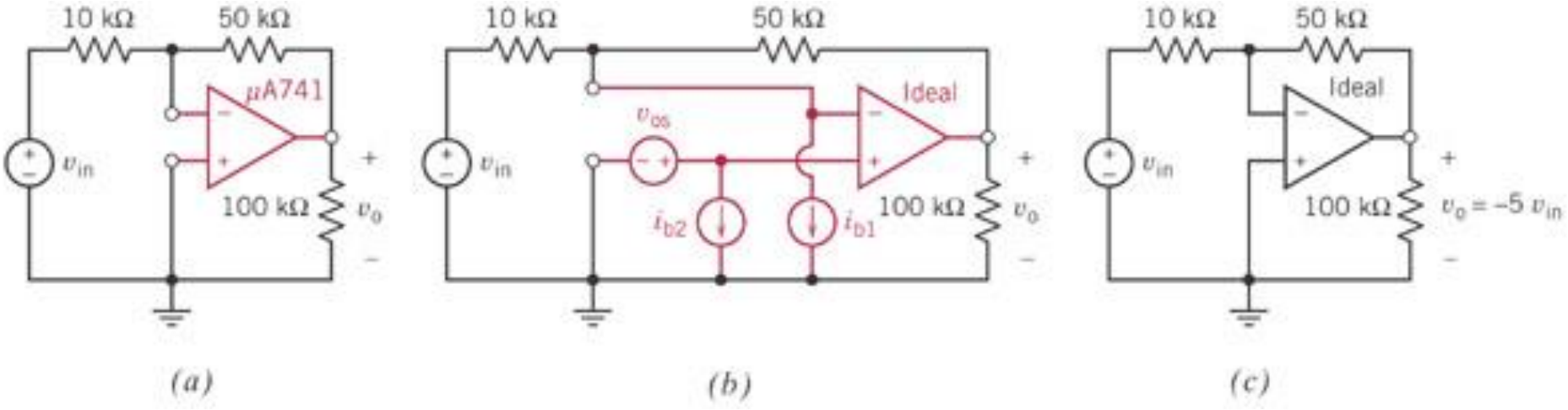


Figure 6.7−2 (a)

Solution

- In figure 6.7-2b the op amp has been replaced by the offset model of an op amp. Superposition can be used to good advantage in analyzing this circuit.
- Figure 6.7-2c shows the circuit used to calculate the response to v_{in} alone. Analysis of the inverting amplifier in Figure 6.7-2c gives

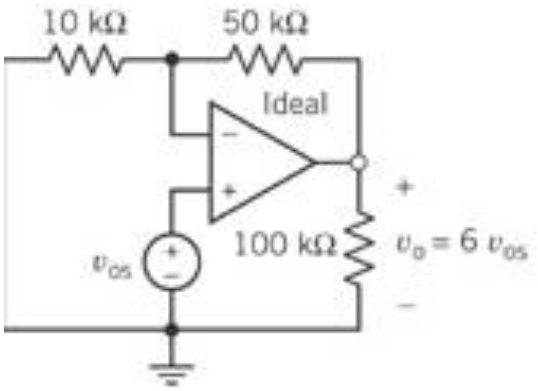
$$v_o = -5 \cdot v_{in}$$



Solution (cont'd)

- Next consider Figure 6.7-2d. This circuit is used to calculate the response to v_{os} alone. It is the noninverting amplifier
  Analysis of the noninverting amplifier gives

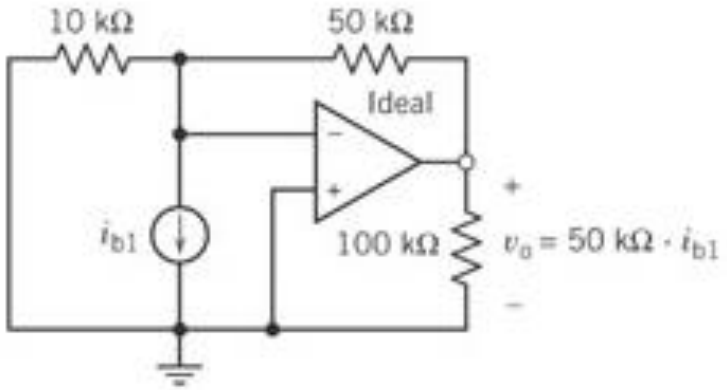
$$v_o = \left(1 + \frac{50\text{k}\Omega}{10\text{k}\Omega}\right) \cdot v_{os} = 6 \cdot v_{os}$$



(d)

- Next consider Figure 6.7-2e. The circuit is used to calculate the response to i_{b1} alone. Using Ohm's law to obtain

$$v_o = 50\text{k}\Omega \cdot i_{b1}$$

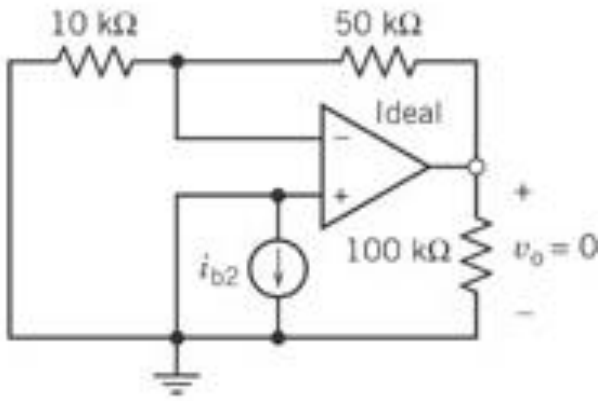


(e)

Solution (cont'd)

- Next consider Figure 6.7-2f. This circuit is used to calculate the response to i_{b2} alone.

$$v_o = 0$$



(f)

- The output caused by all four inputs working together is the sum of the outputs caused by each input working alone.
  Therefore

$$v_o = -5 \cdot v_{in} + 6 \cdot v_{os} + (50\text{k}\Omega) i_{b1}$$

Solution (cont'd)

- When the input of the inverting amp is zero, the output also should be zero. However, v_o is nonzero when we have finite vos or i_{b1}. Let

$$\text{output offset voltage} = 6 \cdot v_{os} + (50\text{k}\Omega) i_{b1}$$

Then $$v_o = -5 \cdot v_{in} + \text{output offset voltage}$$

- How large is the output offset voltage of this inverting amplifier?
The input offset voltage of a uA741 op amp will be at most 5 mV, and the bias current will be at most 500 nA, so

$$\text{output offset voltage} \leq 6 \cdot 5\text{mV} + (50\text{k}\Omega)500\text{nA} = 55\text{mV}$$

We note that we can ignore the effect if the offset voltage when

$$v_o = -5 \cdot v_{in}$$

is much greater than the maximum offset voltage. That is when |5 Vo |> 500 mV

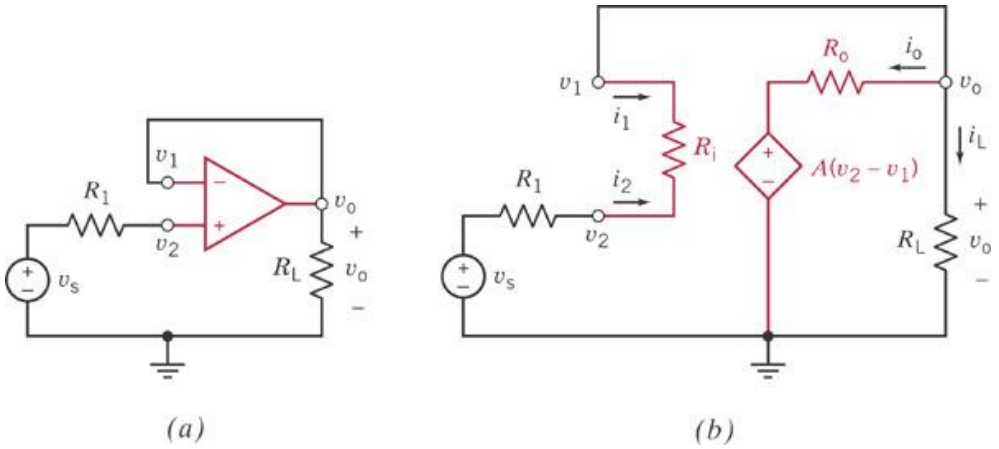
The output offset error can be reduced by using a better op amp, that is, one that guarantees smaller bias currents and input offset voltage.

Example 6.7-2 Finite Gain

- In Figure 6.7-3 a voltage follower is used as buffer amplifier. Analysis based on the ideal operational amplifier shows that the gain of the buffer amplifier is

$$\frac{v_0}{v_S} = 1$$

What effects will the input resistance, output resistance, and finite voltage gain of a practical operational amplifier have on the performance of this circuit?



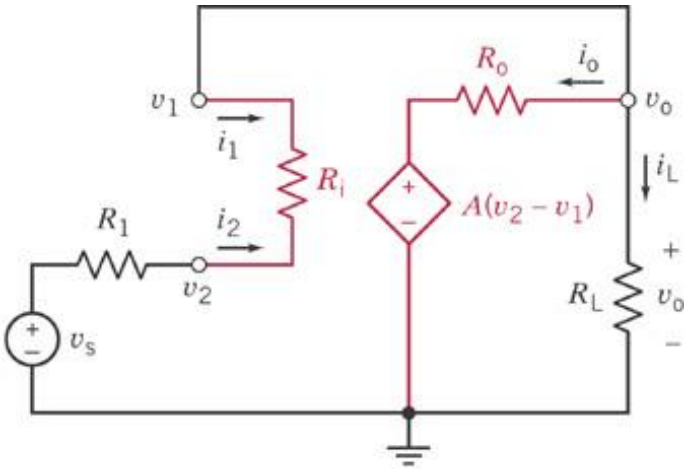
Solution

- Suppose R_1=1kΩ, R_L=10kΩ, R_i =100kΩ, R_o=100Ω and A=10^5V/V
  Suppose v_o=10V

$$i_L = \frac{v_o}{R_L} = \frac{10\text{V}}{10^4\,\Omega} = 10^{-3}\,\text{A}$$

Apply KCL at the top node of R_L to get

$$i_1 + i_o + i_L = 0$$



(b)

It will turn out that i_1 will be much smaller than both i_o and i_L.
It is useful to make the approximation that i_1=0.
Then

$$i_o = -i_L$$

Solution (cont'd)

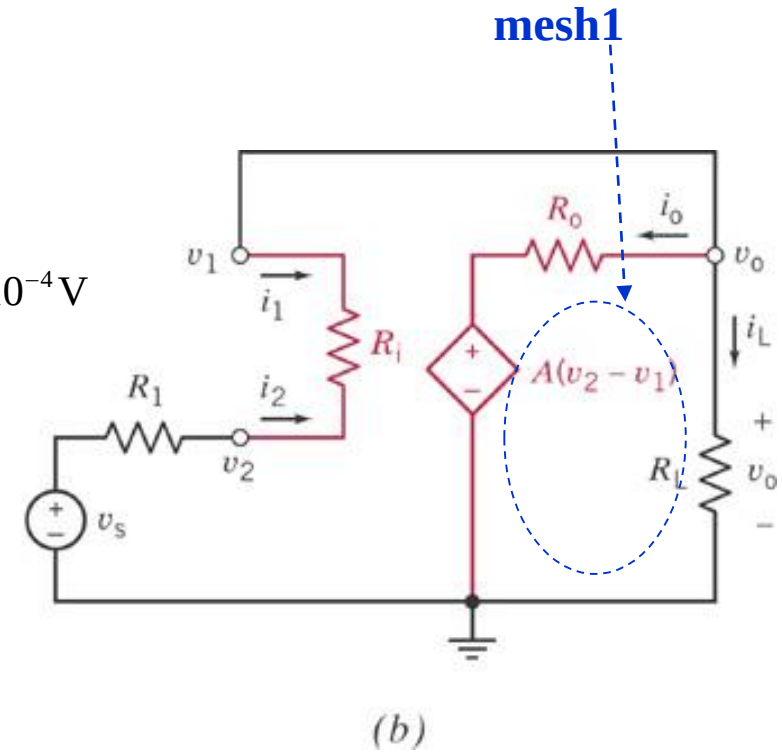
- Next, apply KVL to the mesh 1 to get

$$-A(v_2 - v_1) - i_o R_o + i_L R_L = 0$$

$$\Rightarrow \quad v_2 - v_1 = \frac{i_L(R_o + R_L)}{A} = \frac{10^{-3}(100 + 10000)}{10^5} = 1.01 \times 10^{-4}\,\text{V}$$

Now i1 can be calculated using Ohm's law

$$i_1 = \frac{v_1 - v_2}{R_i} = \frac{-1.01 \times 10^{-4}\,\text{V}}{100\text{k}\Omega} = -1.01 \times 10^{-9}\,\text{A}$$



This justifies our earlier assumption that i1 is negligible compared with io and iL.

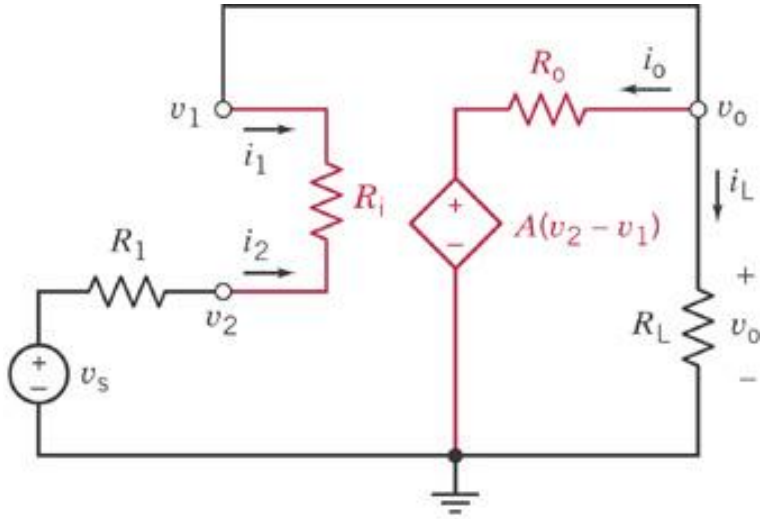
Solution (cont'd)

- Apply KVL to outside loop gives

$$-v_S - i_1 R_1 - i_1 R_i + v_0 = 0$$

Now let us do some algebra to determine Vs

$$\begin{aligned} v_S &= v_0 - i_1(R_1 + R_i) = v_0 + i_2(R_1 + R_i) \\ &= v_0 + \frac{v_2 - v_1}{R_i} \times (R_1 + R_i) \\ &= v_0 + \frac{i_L(R_0 + R_L)}{A} \times \frac{R_1 + R_i}{R_i} \\ &= v_0 + \frac{v_0}{R_L} \times \frac{R_0 + R_L}{A} \times \frac{R_1 + R_i}{R_i} \end{aligned}$$



(b)

Solution (cont'd)

- The gain of this circuit is

$$\frac{v_0}{v_S} = \frac{1}{1 + \frac{1}{A} \times \frac{R_0 + R_L}{R_L} \times \frac{R_1 + R_i}{R_i}}$$

This equation shows that the gain will be approximately 1 when A is very large, $R_0 \ll R_L$, $R_1 \ll R_i$.

In this example, for the specified A, Ro, Ri, we have

$$\frac{v_0}{v_S} = \frac{1}{1 + \frac{1}{10^5} \times \frac{100 + 10,000}{10,000} \times \frac{10^5 + 1000}{10^5}} = \frac{1}{1,00001} = 0.99999$$

Thus, the input resistance, output resistance, and voltage gain of the practical op amp gave only a small essentially negligible, combined effect on the performance of the buffer amplifier.