# 화합물 반도체 (I-2) Introduction & Material Properties

## 2007 / 가을 학기

## Wide Bandgap Materials for High Power RF Devices



## **Combined Figure of Merit - high frequency/high power**



Various Figure-of-Merits for Power Devices (Ref.: A. Q. Huang, IEEE T-ED, 2004)

BFOM =  $\varepsilon \mu E_C^3$ BHFFOM =  $\frac{1}{(R_{\text{on,sp}}C_{\text{in,sp}})}$ NHFFOM =  $\frac{1}{(R_{\text{on,sp}}C_{\text{oss,sp}})}$ - conductive loss- including switching loss- driving reactive load

Table 1. DARPA's	three-track attac	k		
Track/module type	Prime contractor	Funding (Phase II)	Required module output power	Companies also on team
1: X-band transmit/receive module	Raytheon	\$26.9 million (up to \$59.4 million)	60 W continuous wave	Cree
2: Q-band high-power amplifier module (more than 40 GHz)	Northrop Grumman Space Technologies	\$16.5 million (up to \$53.4 million)	20 W continuous wave	Monolithics, Erricore, Boeing, Sirenza Micro Devices
3: Wideband high-power amplifier module (2-20 GHz)	TriQuint Semiconductor	\$15.8 million (up to \$31.7 million)	100 W continuous wave	BAE Systems, Lockheed-Martin II-VI, Nitronex, Emcore
Taken from DARPA's broad agency	announcement			

- launched from 2005
- supported by DARPA

(from Compound Semiconductor(CS) magazine, May 2005) http://compoundsemiconductor.net/articles/magazine

Table 2. DARPA's 18 and 30 month "go/no-go" targets	
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Target	Track 1	Track 2	Track 3
18 months	8–12 GHz transistor with a 1.25 mm gate periphery operating at 40 V with 39 dBm continuous-wave output power, 12 dB gain, a PAE of 60%, a water yield of 50% and 10 <sup>5</sup> hours' projected performance	Q-band transistor with a 0.5 mm gate periphery operating at 25 V with 39 dBm continuous-wave output power, 8 dB gain, a PAE of 35%, a wafer yield of 50% 10 <sup>5</sup> hours' projected performance	As for Track 1
30 months	8–12 GHz power-amplifier MMIC operating at 48 V with 15 W continuous-wave output power, 16 dB gain, a PAE of 55% and a wafer yield of 50%	Q-band MMIC operating at 28 V with 4 W continuous-wave output power, 7.5 dB gain, a PAE of 37% and a wafer yield of 50%	2–20 GHz power-amplifier MMIC operating across a decade of bandwidth at 48 V with 15 W continuous-wave output power, 16 dB gain, a PAE of 30%, and a wafer yield of 50% (at least 12 three-inch wafers)

Taken from DARPA's broad agency announcement - actual program goals have been modified slightly.

### (from Compound Semiconductor(CS) magazine, May 2005) <u>http://compoundsemiconductor.net/articles/magazine</u>

## Lattice Structure of Basic Semiconductors (1)

**2 FCC (Face Centered Cubic) cells – separation (a/4, a/4, a/4)** 

- Diamond Structure; Si 1Si FCC cell + 1Si FCC cell
- Zincblende Structure; GaAs 1 Ga FCC cell + 1As FCC cell



Diamond Structure ex) Si, Ge, C ... Zincblende Structure ex) GaAs, GaP ....3-5

## Lattice Structure of Basic Semiconductors (II)



Wurtzite Structure ex) CdS, ZnS ...2-6 Rock-salt Structure ex) PbS, PbTe ...4-6

## Various III-V Semiconductors



\* 같은 lattice constant를 갖는 반도체 - GaAs/AlAs or InAs/GaSb/AlSb : GaAs substrate InP/In<sub>0.53</sub>GaAs/In<sub>0.48</sub>AlAs : InP substrate

## **Double Heterostructure LED & Laser Diode**



Nobel Lectures (Reviews of Modern Physics, Volume 73, July 2001)

- H. Kroemer, "Quasielectric fields and band offsets: teaching electrons new tricks"
- Z. I. Alferov, "The double heterostructure concept and its applications in physics, electronics, and technology"

## III-V Compound의 crystal 구조

\* Crystal structure \* Energy Band-gap diagram  $\psi(\mathbf{r}) = e^{i\mathbf{k}\cdot\mathbf{r}}u_{n\mathbf{k}}(\mathbf{r})$ a: lattice constant T = 300 K3 **Real Space** 0.40 eV Chergy (s-sv) (electron volts) X<sub>6</sub> Δ3 <Zinc-Blende 구조> e<sub>c</sub> T<sub>6</sub> (-1/4,1/4,1/4) 1.90 eV 1.71 eV 1.42 eV Γ<sub>8</sub> Ev kz (V1) 0.34 eV Heavy holes k Space Light holes (V2) X Split-off band (V3) **<Reciprocal** Lattice> (111) T(000) X(100) ٨ ۵ х.. Reduced wave vector a (Ref.) Sze, 1.2.2 \* Energy gap  $\propto$  (Lattice constant) <sup>-1</sup> \* conduction band -  $\Gamma_6$ , L<sub>6</sub>, X<sub>6</sub> valley

## GaAs의 Energy Band 구조



## **Atomic Physics of Semiconductors**



$$\frac{1}{m^*} = \frac{1}{\hbar^2} \frac{\partial^2 E}{\partial k^2}$$

## **Electron Effective Mass**



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#### **Electrons in Conduction Band**



## Compound Semiconductor의 전기적 특성



## Inter-valley Transfer in GaAs Conduction Band



## **AIGaAs Lattice-Matched to GaAs Substrate**



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## **InP-based Material System**



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## v-E Characteristics of InGaAs & Nitride Semiconductors



## SiC Crystal Structures





Closely-Packed Crystal Structures

◉ 積層方向

#### **Stacking Order of 3C-SiC**



### **Stacking Order of 6H-SiC**

<0001> ① • <1120>



## Properties of typical SiC polytypes and Si, GaAs, GaN

	SiC			Si	GaAs	GaN
Crystal Form	<b>3</b> C (ZB)	<b>6</b> H	<b>4</b> H	dia.	ZB	W
Band Structure	indirect				direct	
Bandgap [eV]	2.3	3.0	3.3	1.11	1.43	3.5
Electron Mobility [cm <sup>2</sup> /V s]	1000	450	900	1500	8500	900
Hole Mobility [cm <sup>2</sup> /V s]	50	50	100	600	400	30?
Breakdown Field [MV/cm]	2	3	3	0.3	0.4	3
Thermal Conductivity [W/cm K]	4.9	4.9	4.9	1.5	0.5	1.3
Electron Saturation Velocity [10 <sup>7</sup> cm/s]	2.7	2	2.7	1	2*	2.5
Dielectric Constant ε	9.7	9.7	9.7	11.8	12.8	9.5

## Various Substrate for GaN Power Amplifiers

	Sapphire	n-type	s.i.	GaN bulk	Si
		SiC	SiC		
Lattice mismatch (%)	13	3.1	3.1	0	17
Availability / Price (2", \$)	100	500	3000	not available	100
Thermal Conductivity (W/cmK)	0.3	4	4	1.3	1.48



## Wurtzite GaN, InN, and AIN



\* substrate for GaN/InN/AIN - Al<sub>2</sub>O<sub>3</sub> (lattice mismatched) SiC (lattice mismatched) GaN (lattice matched) : difficult to grow

## Transistor Nanotechnology



## Strained Si MOSFET - 45nm node



## Valence Band of SiGe in Compressive Strain



## **Conduction/Valence Band of Si in Tensile Strain**



## **Right Material for n-Channel (1)**



(From Jerry Woodall)



## Right Material for n-Channel (II)



(Source) D. K. Sadana, Sematech Workshop, 2005

# Higher mobility leads to higher speed at a given bias.

S. Laux, P. Solomon, M. Fischetti, 2003.

DD	Si 10nm	Si 20nm	InGaAs 20nm	InGaAs vs Si 10nm	InGaAs vs Si 20nm
(V)	(ps)	(ps)	(ps)	(%)	(%)
0.25	4.9	5.9	2.8	76	110
0.6	2.8	3.8	1.9	45	98

Performance benefits continue down to  $L_g$ = 20 nm.

Mobility continues to be important in scaled devices

## High-mobility dual-channel CMOS for (sub)-22 nm

#### (Target of DUALLOGIC) - 36month project of EU

# Monolithic co-integration of Ge pMOS with III-V nMOS on the same engineered substrate using a 65 nm/200 mm platform



Material	μ <sub>e</sub> (cm²/Vs)	μ <sub>h</sub> (cm²/Vs)
Diamond	2200	1800
Ge	3900	1900
InP	5400	200
GaAs	8500	400
InGaAs(53%)	12000	300
InAs	40000	500
GaSb InSb	3000 77000	1000 850
InP <b>GaAs</b> InGaAs(53%) InAs GaSb InSb	5400 <b>8500</b> 12000 40000 3000 77000	200 <b>400</b> 300 500 <u>1000</u> 850

#### Main project components

- Local GeOI substrates and evaluation
- III-V Selective epitaxy process and tool development
- Front end modules development and co-integration
- Device modeling and generic circuit design

(LETI, ST-Crolles, AIXTRON, IMEC, IBM-Zurich, NCSR, UoG, KUL, NXP, UoG)

### Sub-22 nm node



#### 화<mark>합물반도체</mark>

## **High Mobility Channel Materials**





- InAs has lowest intrinsic delays with largest band-to-band tunneling currents.
- GaAs provides slightly higher delays but at much reduced off state leakage

(Ref.) Y. Nishi, 2006