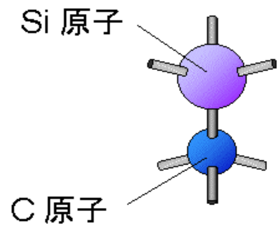
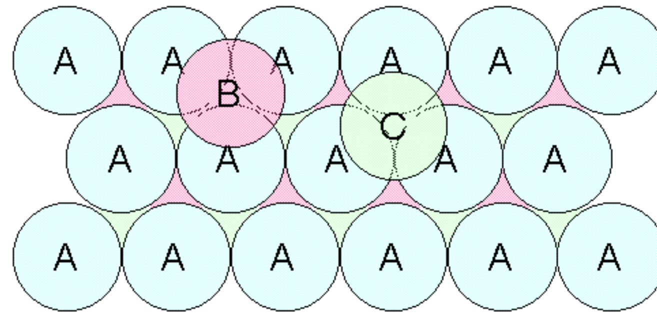
# 화합물 반도체 ( I-3 )
# Introduction & Material Properties

2007 / 가을 학기

# SiC Crystal Structures

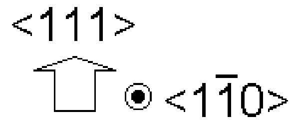


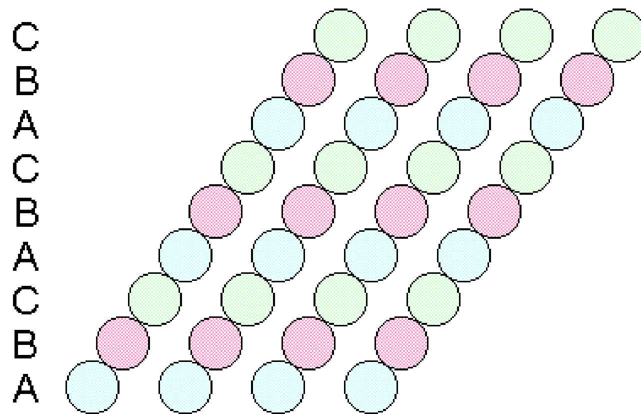



◉ 積層方向

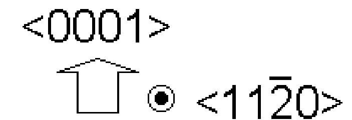
*Closely-Packed Crystal Structures*

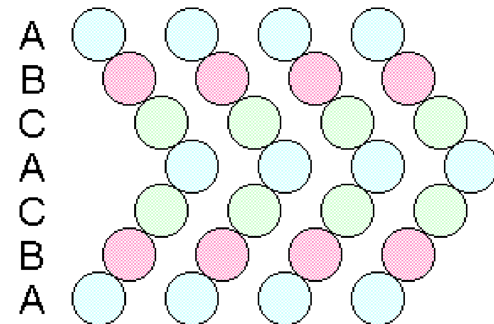
## Stacking Order of 3C-SiC




## Stacking Order of 6H-SiC



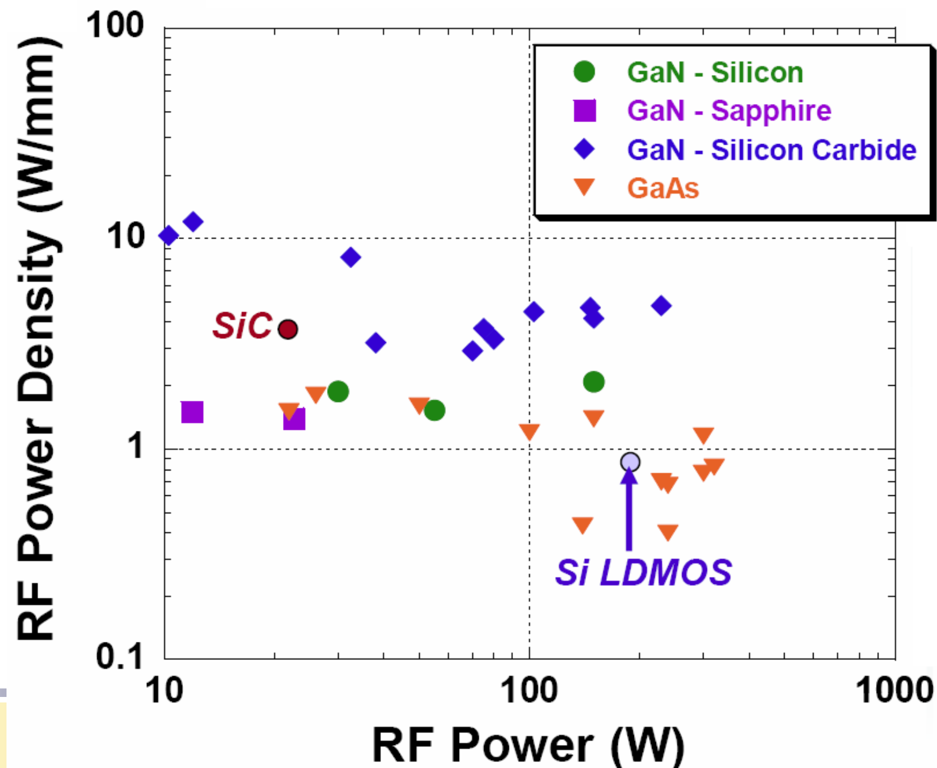



# Properties of typical SiC polytypes and Si, GaAs, GaN

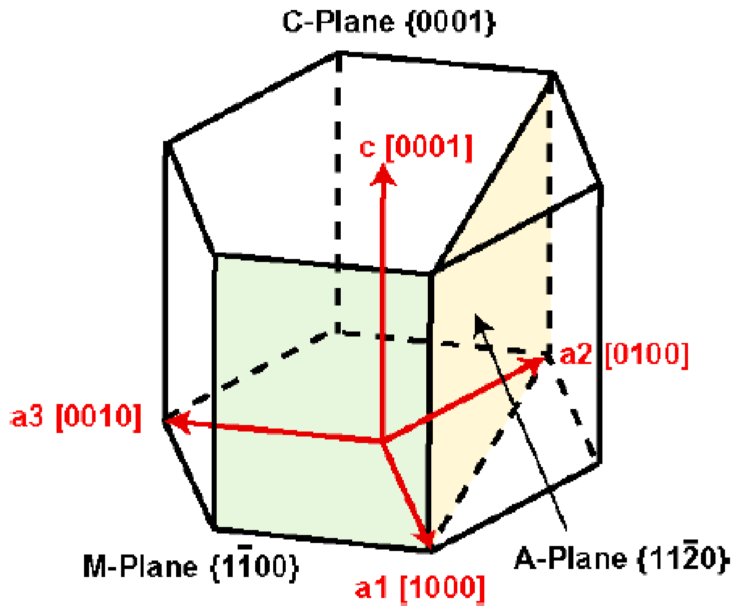
| | SiC | | | Si | GaAs | GaN |
|---|---|---|---|---|---|---|
| **Crystal Form** | **3C** (ZB) | **6H** | **4H** | **dia.** | **ZB** | **W** |
| **Band Structure** | indirect | | | | direct | |
| **Bandgap [eV]** | 2.3 | 3.0 | 3.3 | 1.11 | 1.43 | 3.5 |
| **Electron Mobility [cm$^2$/V s]** | 1000 | 450 | 900 | 1500 | 8500 | 900 |
| **Hole Mobility [cm$^2$/V s]** | 50 | 50 | 100 | 600 | 400 | 30? |
| **Breakdown Field [MV/cm]** | 2 | 3 | 3 | 0.3 | 0.4 | 3 |
| **Thermal Conductivity [W/cm K]** | 4.9 | 4.9 | 4.9 | 1.5 | 0.5 | 1.3 |
| **Electron Saturation Velocity [10$^7$cm/s]** | 2.7 | 2 | 2.7 | 1 | 2* | 2.5 |
| **Dielectric Constant ε** | 9.7 | 9.7 | 9.7 | 11.8 | 12.8 | 9.5 |

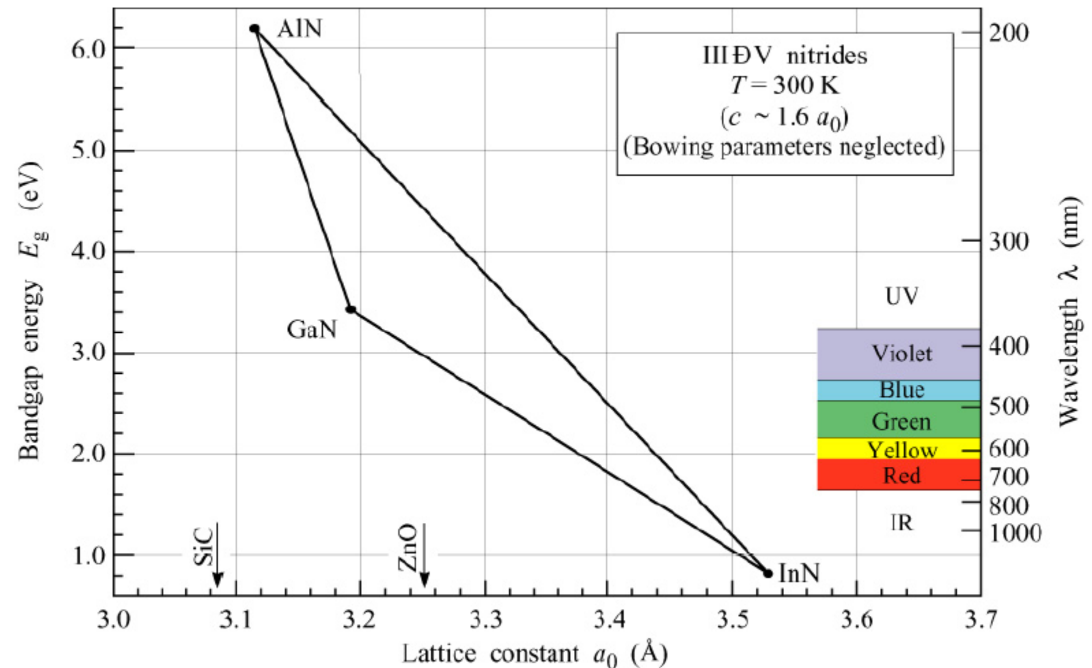
# *Various Substrate for GaN Power Amplifiers*

| | Sapphire | n-type SiC | s.i. SiC | GaN bulk | Si |
|---|---|---|---|---|---|
| Lattice mismatch (%) | 13 | 3.1 | 3.1 | 0 | 17 |
| Availability / Price (2“, $) | 100 | 500 | 3000 | not available | 100 |
| Thermal Conductivity (W/cmK) | 0.3 | 4 | 4 | 1.3 | 1.48 |



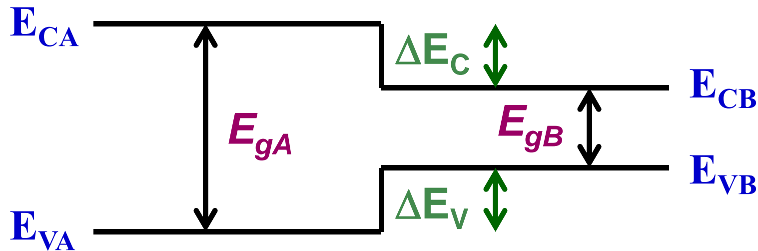
# Wurtzite GaN, InN, and AlN




*** substrate for GaN/InN/AlN - $Al_2O_3$ (lattice mismatched)**
**SiC (lattice mismatched)**
**GaN (lattice matched) : difficult to grow**

# •Band-edge Lineup of Heterojunctions (I)



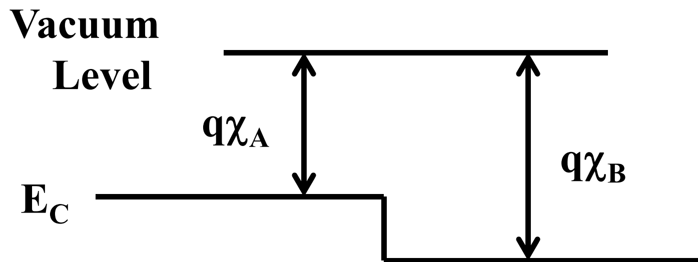

$Al_xGa_{1-x}As/GaAs$ < 실험적 측정 >

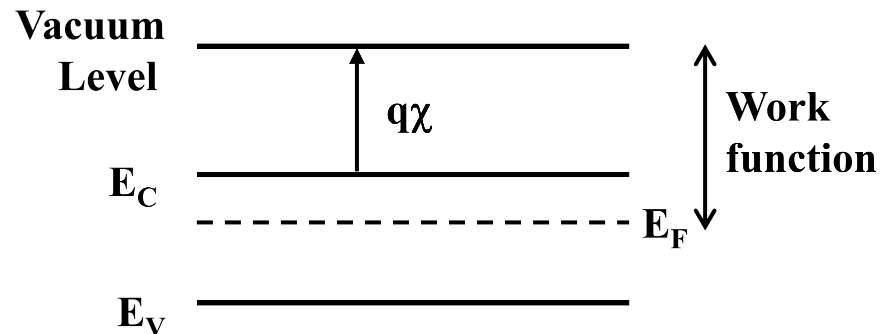
$\Delta E_c \sim 0.6\Delta E_g$

$\Delta E_v \sim 0.4\Delta E_g$

* <u>Electron-Affinity Rule</u> ( Classical theory ) → $\Delta E_c = q(\chi_B - \chi_A)$ 에 의하면

$\Delta E_c \sim 0.85\Delta E_g$

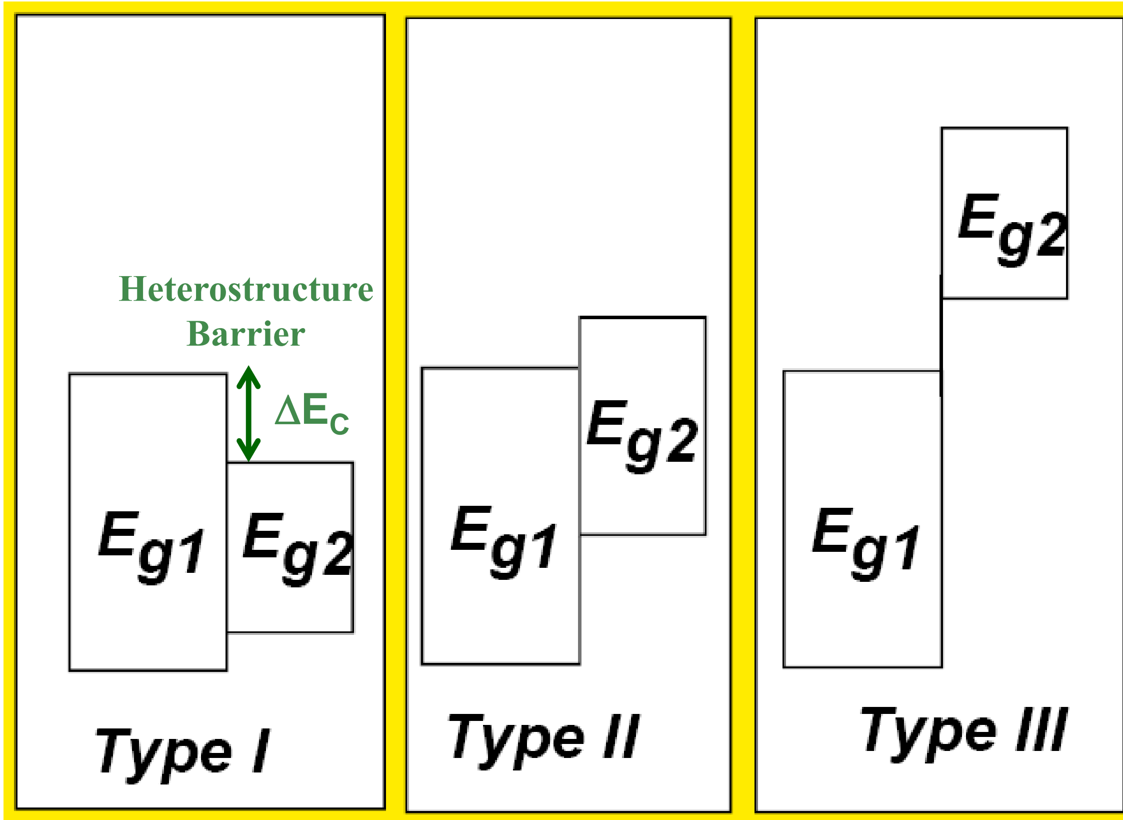


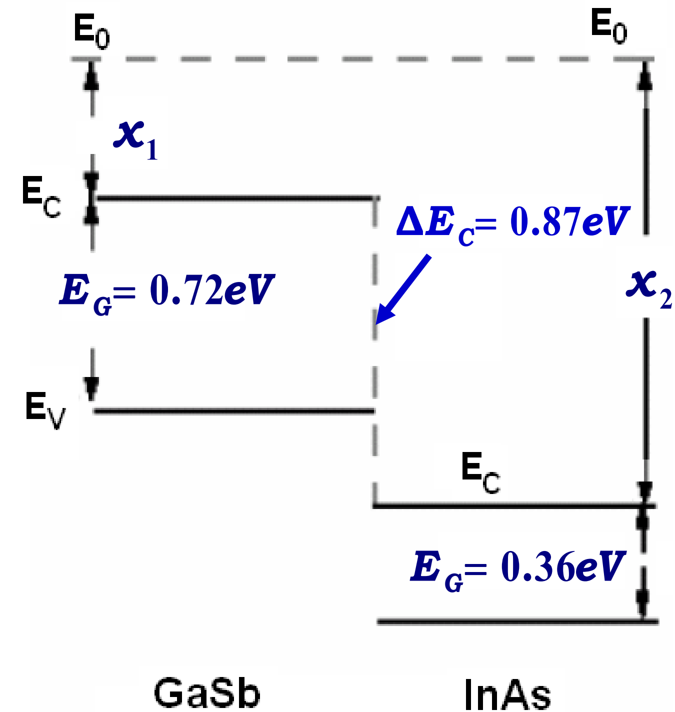

- 실제 값과 차이가 나는 원인 ; interface 효과에 의해 $\Delta E_C$ 변화
  - atom의 rearrangement
  - wave function들의 interaction.

* Ref, "Electronic Materials Science" ( Ch. 14. 4 )

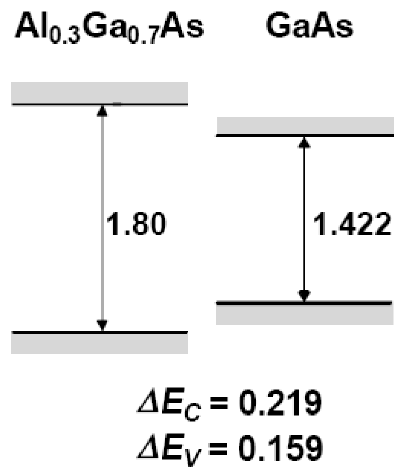
# •Band-edge Lineup of Heterojunctions (II)

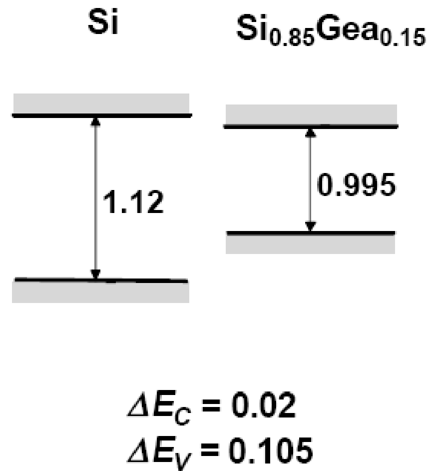


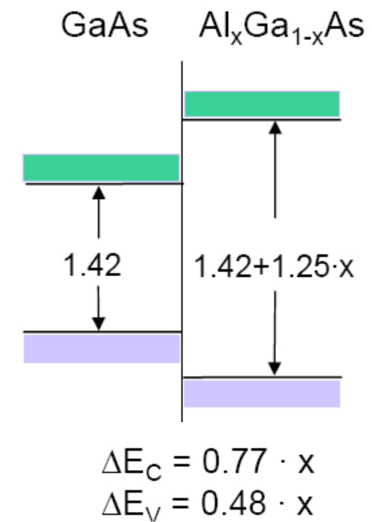

- AlGaAs/GaAs
- GaSb/AlSb
- GaAs/GaP
- InP/$In_{0.52}Al_{0.48}P$
- InGaAs/GaSbAs
- $Al_xIn_{1-x}As$/InP
- InAs/GaSb

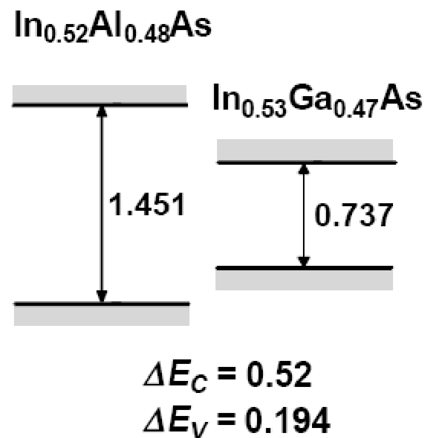


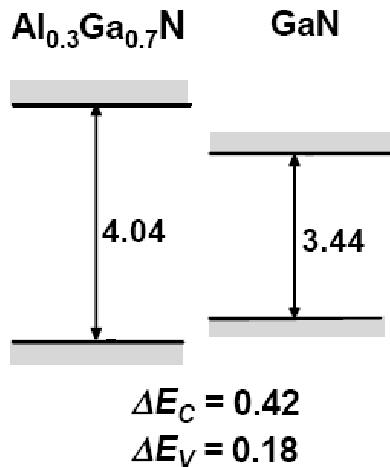
# •Band-edge Lineup of Heterojunctions (III)

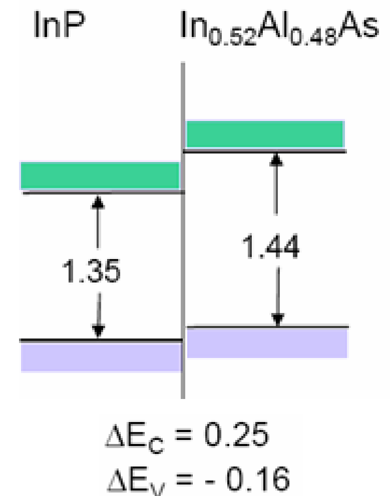


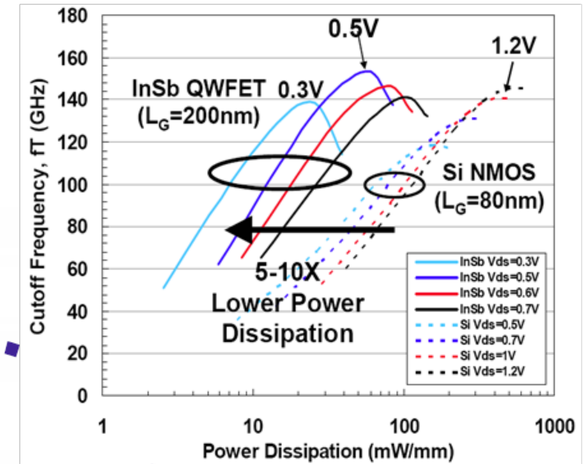



# Transistor Nanotechnology

(source) R. Chau, Intel




Requires a high-k/metal-gate to eliminate Schottky $I_{GATE}$

Technology Generation

90 nm 2003 | 65 nm 2005 | 45 nm 2007 | 32 nm 2009 | 2011+

Manufacturing → Development → Research

50 nm — SiGe S/D PMOS; Uniaxial strain; 1.2nm thin gate oxide

35 nm — SiGe S/D PMOS; Uniaxial Strain; 1.2nm thin gate oxide

30 nm — Metal Gate; High-k; Si Substrate

20 nm — 40nm; L$_G$=20nm; Tri-Gate

10 nm — Si

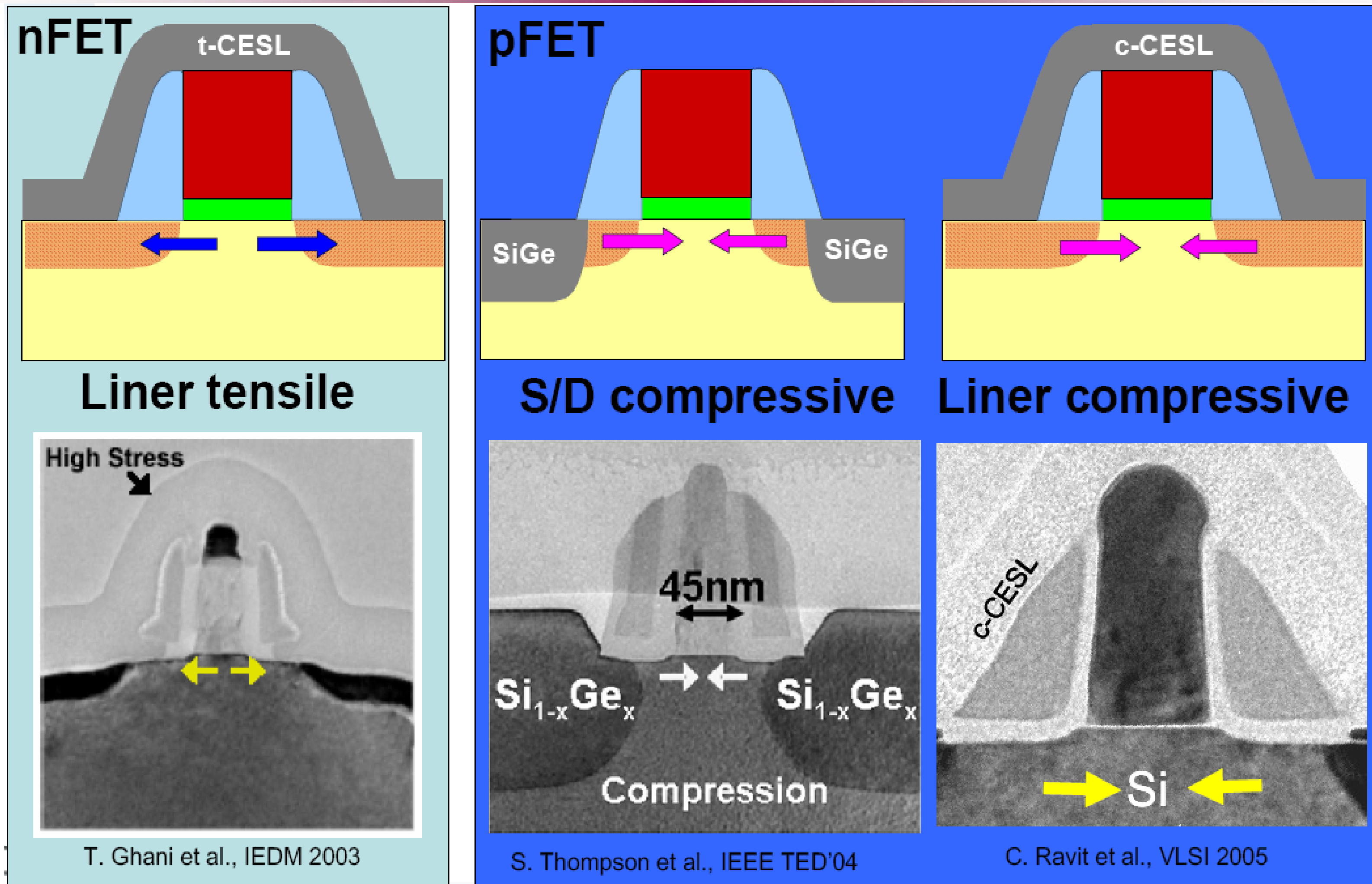
S D S G — III-V

5 nm — Semiconductor Nanowire

Carbon Nanotube

Emerging Nanoelectronic Devices

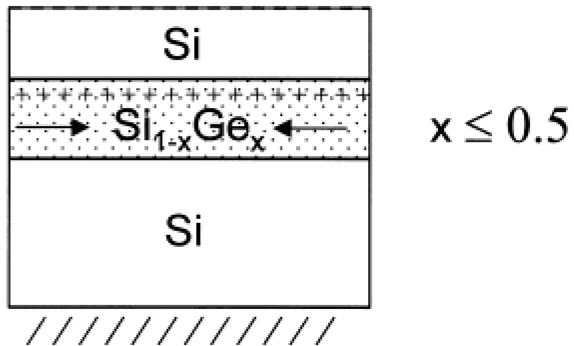
# Strained Si MOSFET - 45nm node




**(Ref.) T. Ernst, 2006**

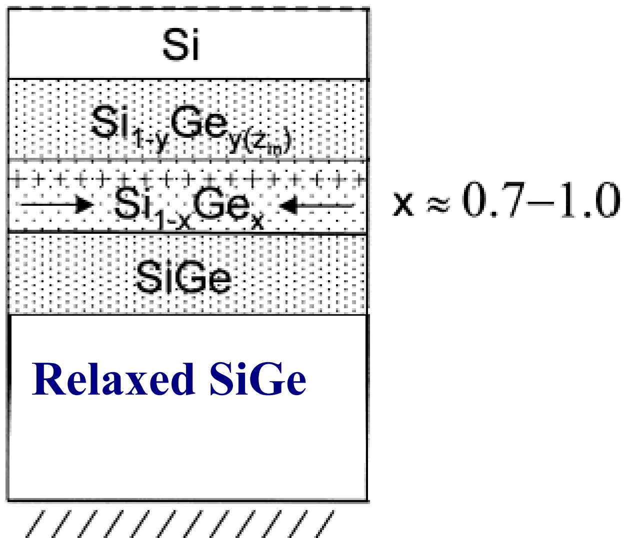
# Valence Band of SiGe in Compressive Strain

* **Pseudomorphic**



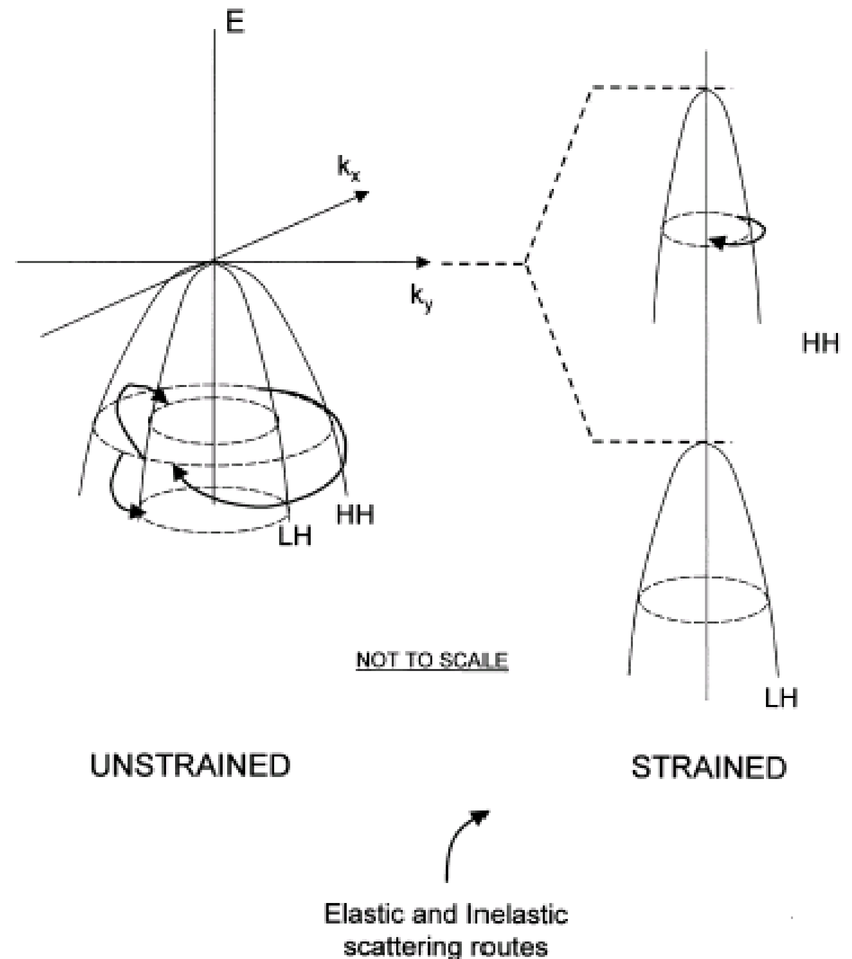

$x \leq 0.5$

* **Virtual Substrate - Metamorphic**

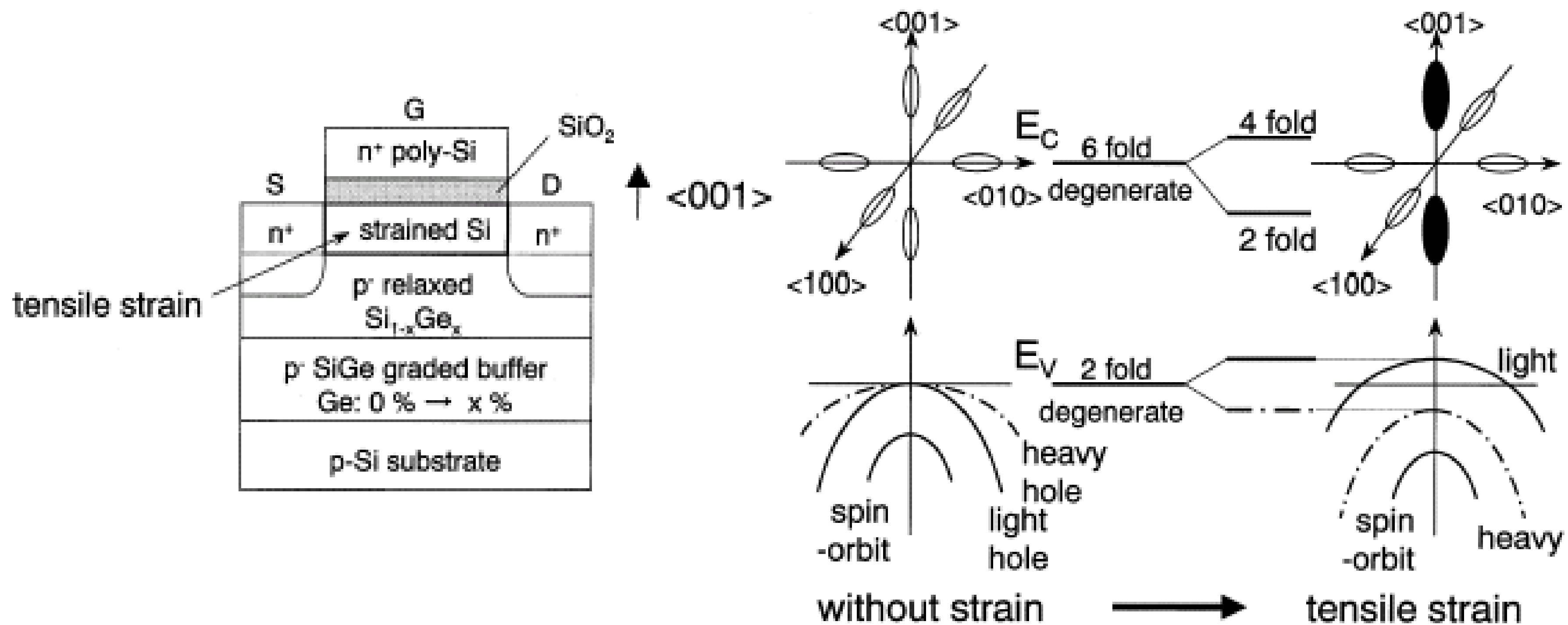



$x \approx 0.7–1.0$

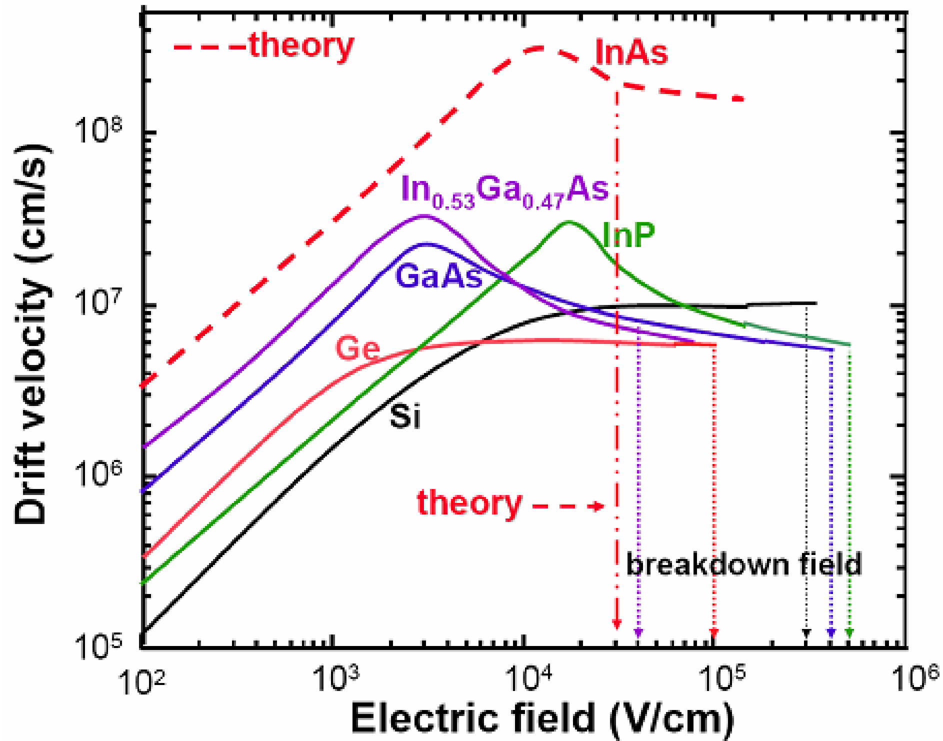
* **Valence Band of SiGe in Compressive Strain**



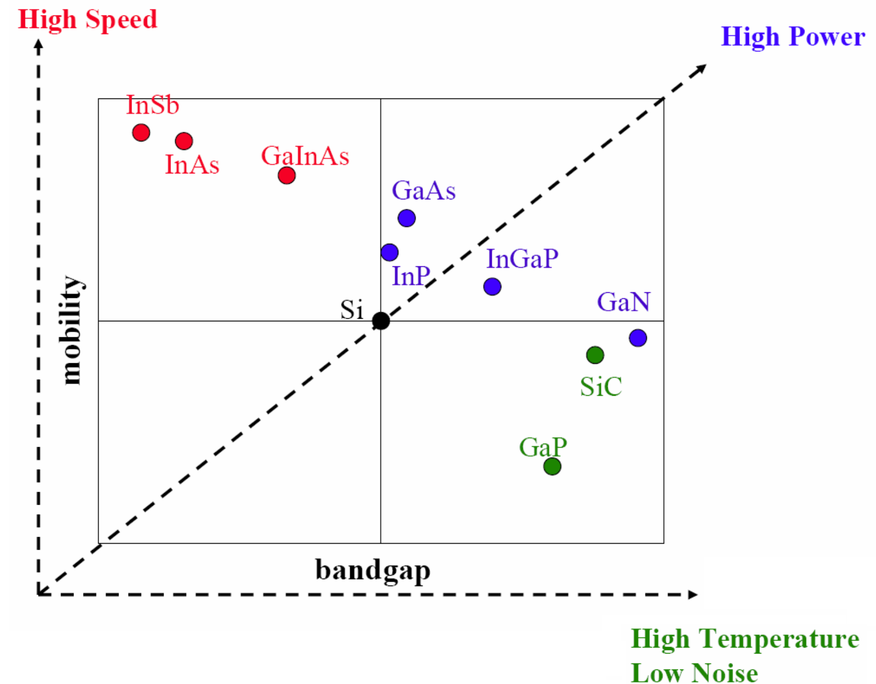
# Conduction/Valence Band of Si in Tensile Strain



# Right Material for n-Channel ( I )

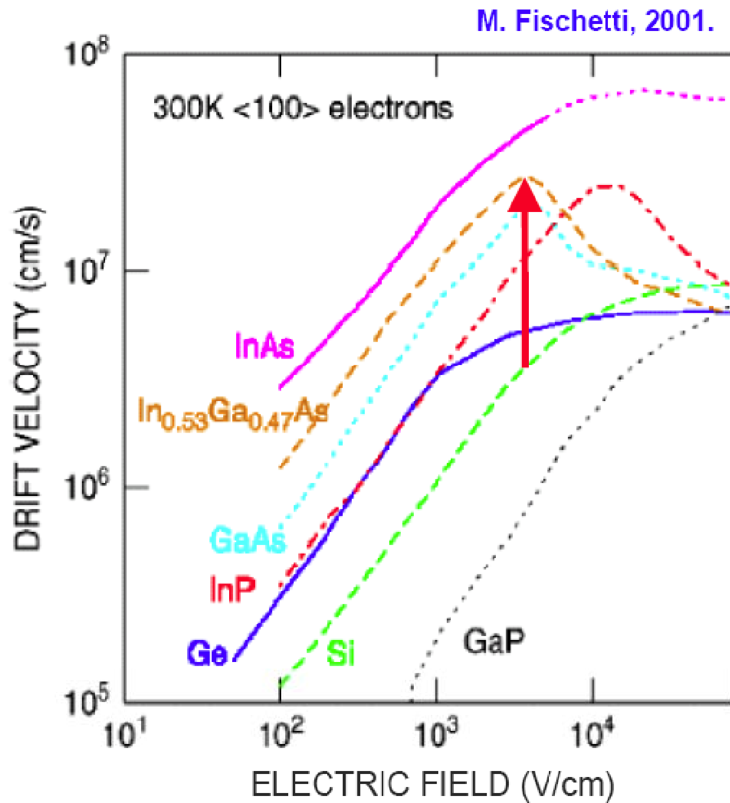



(From Jerry Woodall)




(Source) T. P. Ma, Sematech Workshop, 2005

# Right Material for n-Channel ( II )




(Source) D. K. Sadana, Sematech Workshop, 2005

**Higher mobility leads to higher speed at a given bias.**

S. Laux, P. Solomon, M. Fischetti, 2003.

| DD | Si 10nm | Si 20nm | InGaAs 20nm | InGaAs vs Si 10nm | InGaAs vs Si 20nm |
|---|---|---|---|---|---|
| (V) | (ps) | (ps) | (ps) | (%) | (%) |
| 0.25 | 4.9 | 5.9 | 2.8 | 76 | 110 |
| 0.6 | 2.8 | 3.8 | 1.9 | 45 | 98 |

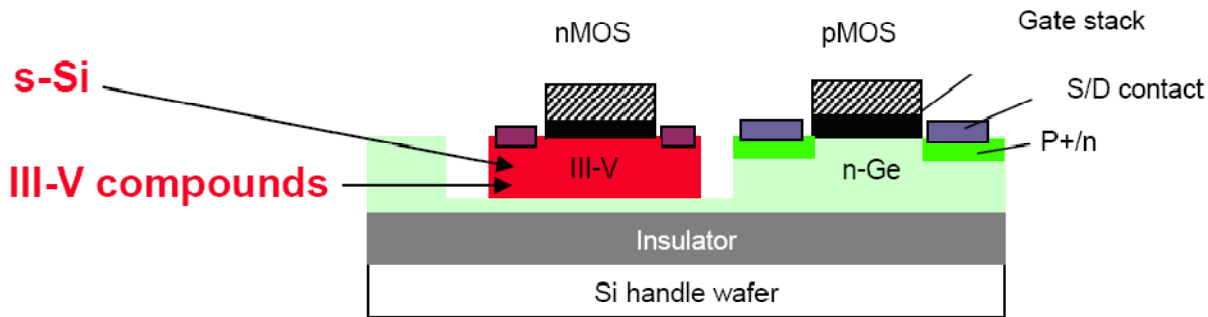
**Performance benefits continue down to $L_g$= 20 nm.**

**Mobility continues to be important in scaled devices**

# High-mobility dual-channel CMOS for (sub)-22 nm

(Target of DUALLOGIC) - 36month project of EU

**Monolithic co-integration of Ge pMOS with III-V nMOS on the same engineered substrate using a 65 nm/200 mm platform**



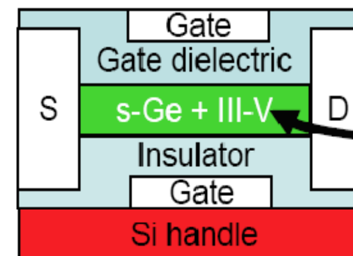

| Material | $\mu_e$ ($cm^2/Vs$) | $\mu_h$ ($cm^2/Vs$) |
|---|---|---|
| Diamond | 2200 | 1800 |
| Si | 1350 | 480 |
| Ge | 3900 | 1900 |
| InP | 5400 | 200 |
| GaAs | 8500 | 400 |
| InGaAs(53%) | 12000 | 300 |
| InAs | 40000 | 500 |
| GaSb | 3000 | 1000 |
| InSb | 77000 | 850 |

## Main project components

- Local GeOI substrates and evaluation
- III-V Selective epitaxy process and tool development
- Front end modules development and co-integration
- Device modeling and generic circuit design

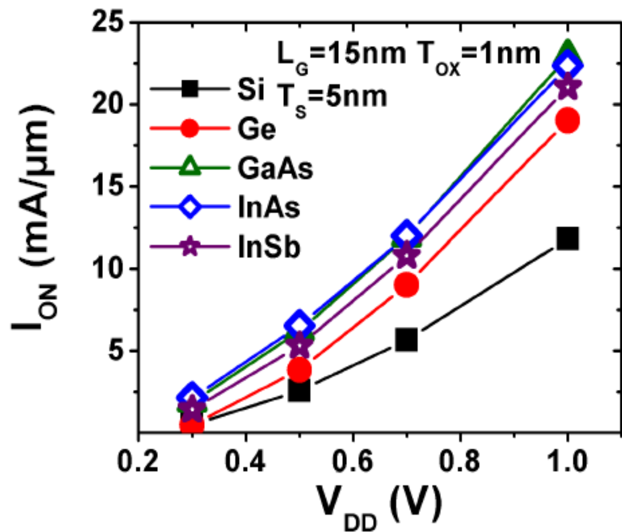
(LETI, ST-Crolles, AIXTRON, IMEC, IBM-Zurich, NCSR, UoG, KUL, NXP, UoG)

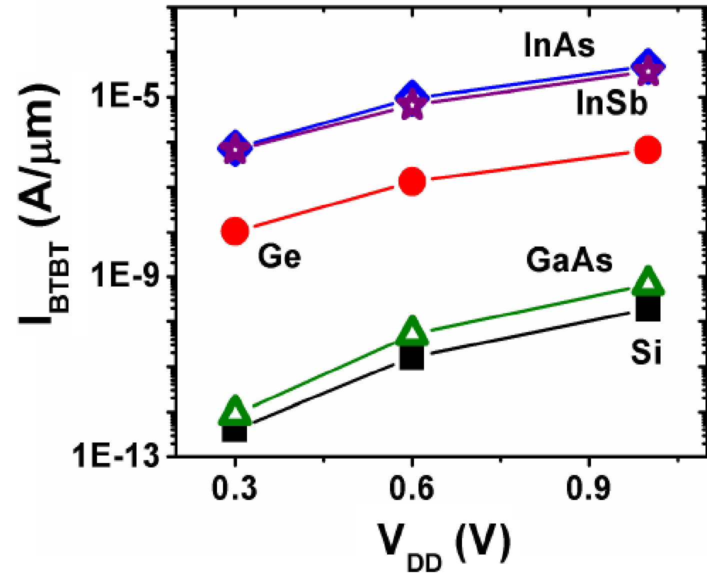
## Sub-22 nm node

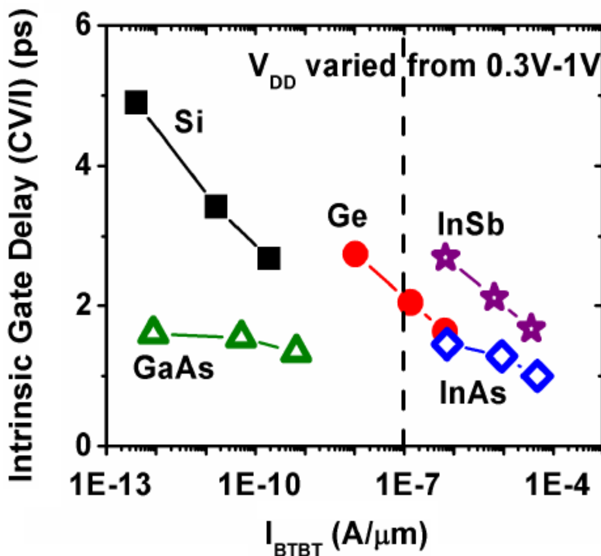



dual channel as the main new introduction ?

# *High Mobility Channel Materials*



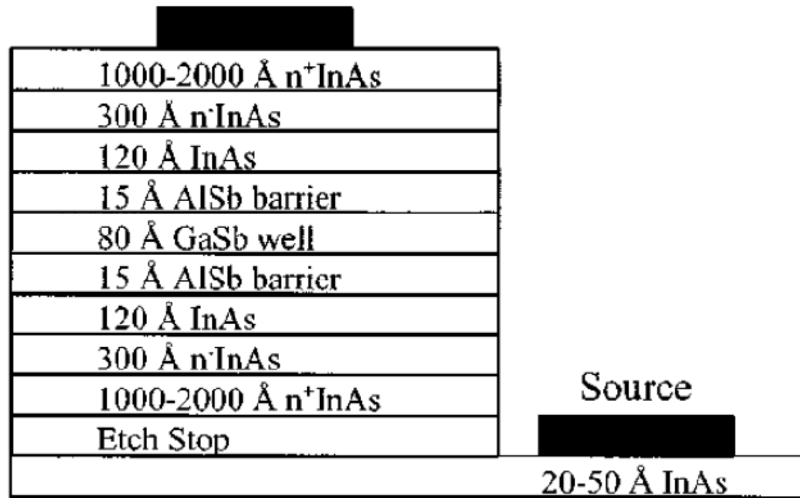



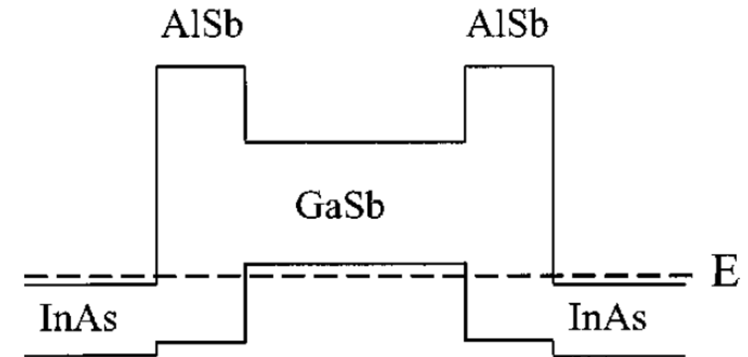



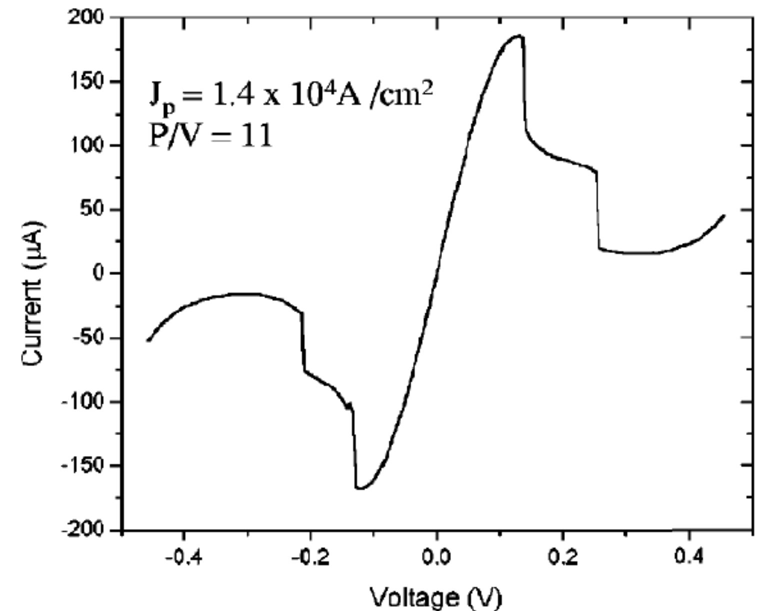

- **InAs has lowest intrinsic delays with largest band-to-band tunneling currents.**
- **GaAs provides slightly higher delays but at much reduced off state leakage**

**(Ref.) Y. Nishi, 2006**

# *Resonant Interband Tunneling Diode (RITD)*

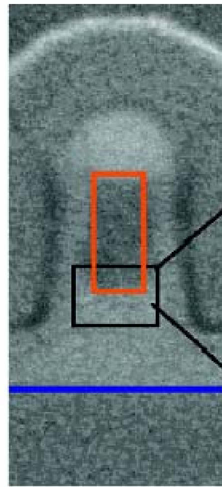


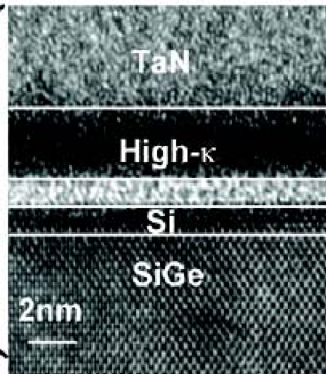




**(Ref.) B. R. Benett, et al.,**
**J. Vac. Sci. Technol. B 18, p. 1650, 2000**

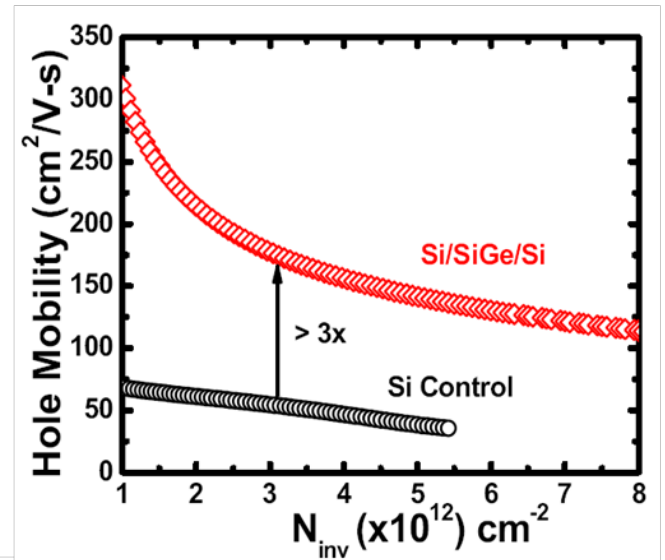
# p-Channel ; 70nm Ge PMOS - SEMATECH (2007)

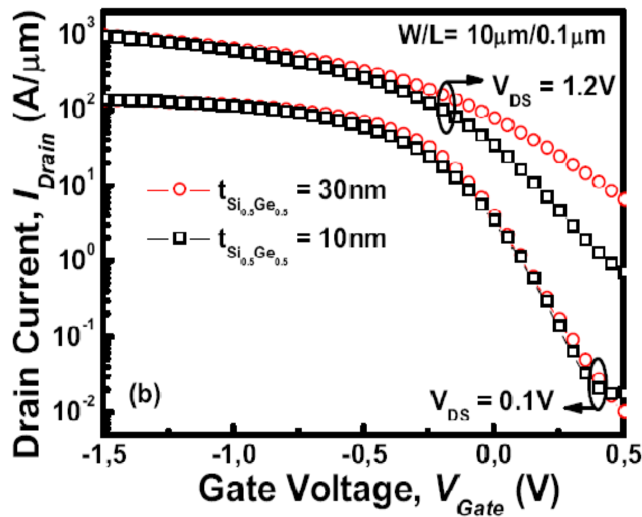


CVD growth for Si/SiGe/Si heterostructures

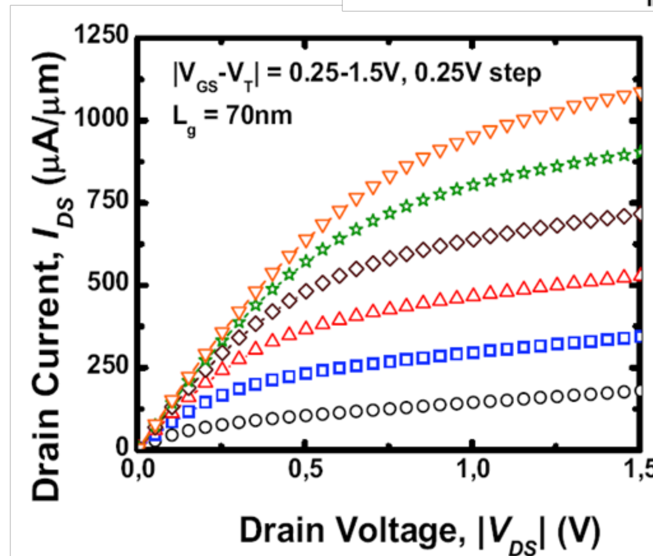



$HfSiO_x$
~1nm Si passivation



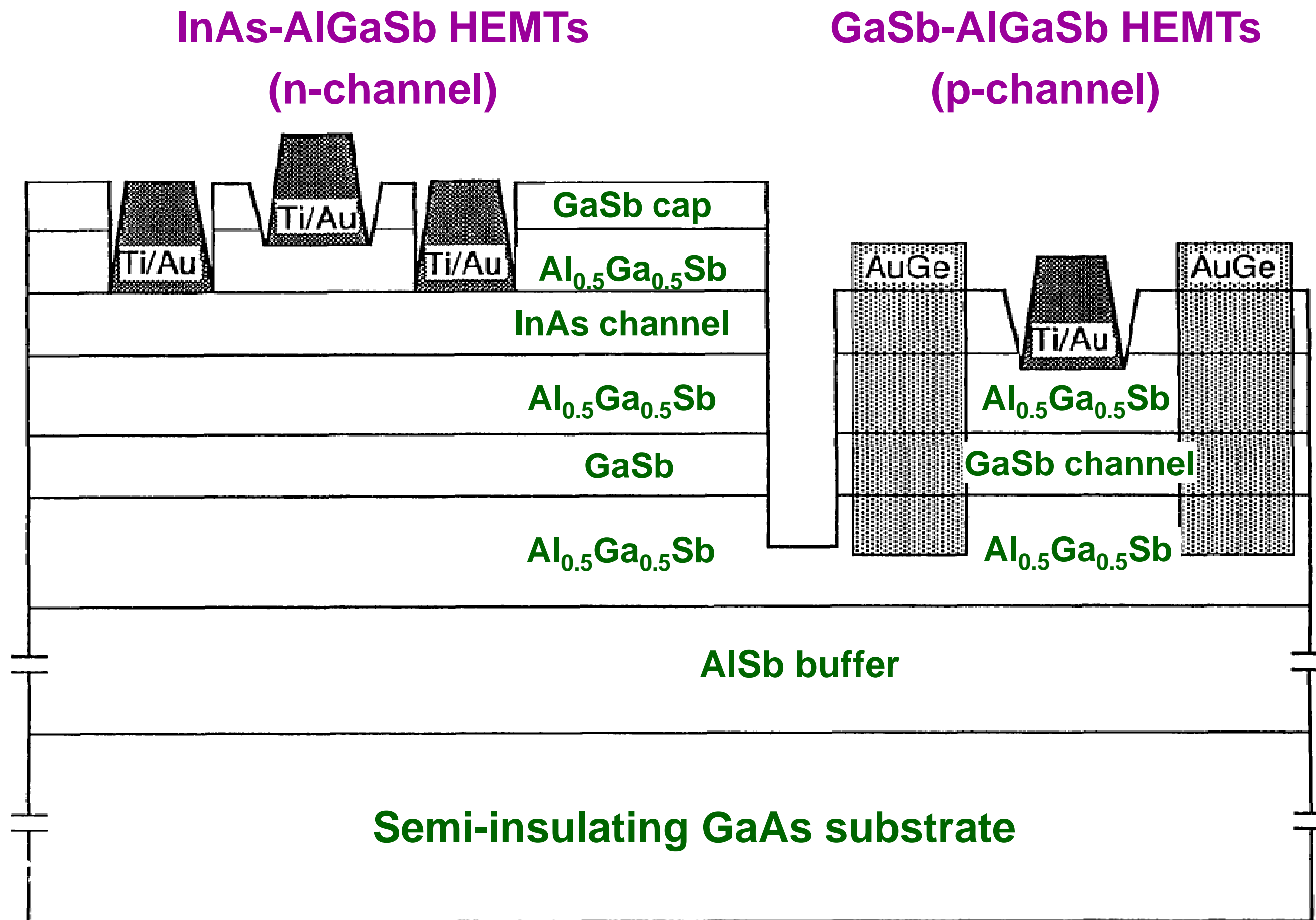




< 10nm $Si_{0.5}Ge_{0.5}$ for higher $I_{on}/I_{off}$ >




(Ref.)
D. Q. Kelly, 2007

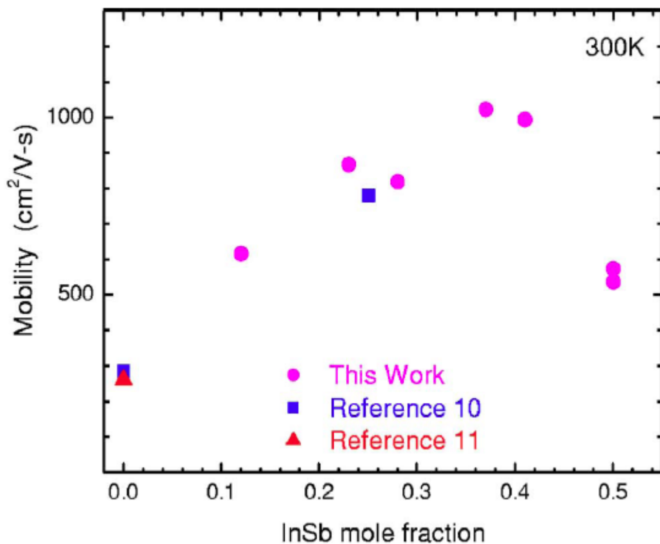
# CMOS-like III-V Logic based on Sb-compounds



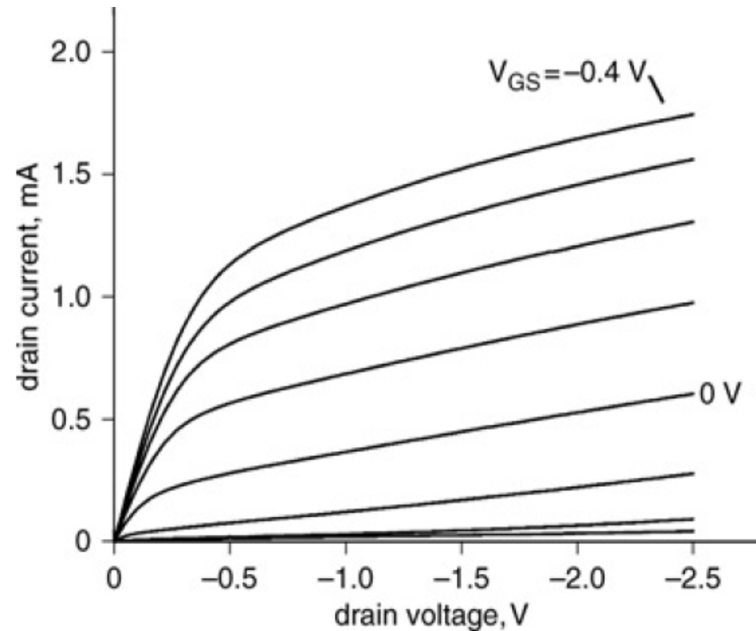

(proposed by Prof. Wang's group)

# *Strained Sb-based p-channel HFET*

InAs 20 Å
$In_{0.2}Al_{0.8}Sb$ 40 Å
$Al_{0.7}Ga_{0.3}Sb$ 100 Å
$In_{0.41}Ga_{0.59}Sb$ 75 Å
$Al_{0.7}Ga_{0.3}Sb$ 210 Å
p-$Al_{0.7}Ga_{0.3}Sb$ 50 Å (Be ~1 x $10^{18}$)
$Al_{0.7}Ga_{0.3}Sb$ 1.5 μm
SI GaAs




**$\mu$=1,020 cm²/Vs, $n_s$= 1.6x10¹² cm⁻²**
**(Hall mobilities up to 1,500 cm²/Vs)**




$L_G = 0.25$ μm, $L_{DS} = 1.0$ μm, $W_G = 28$ μm

**$g_{m,max}$=133mS/mm**
**$f_T$=15GHz, $f_{max}$=27GHz**

**(Ref.) NRL, 2007 (EL, APL)**