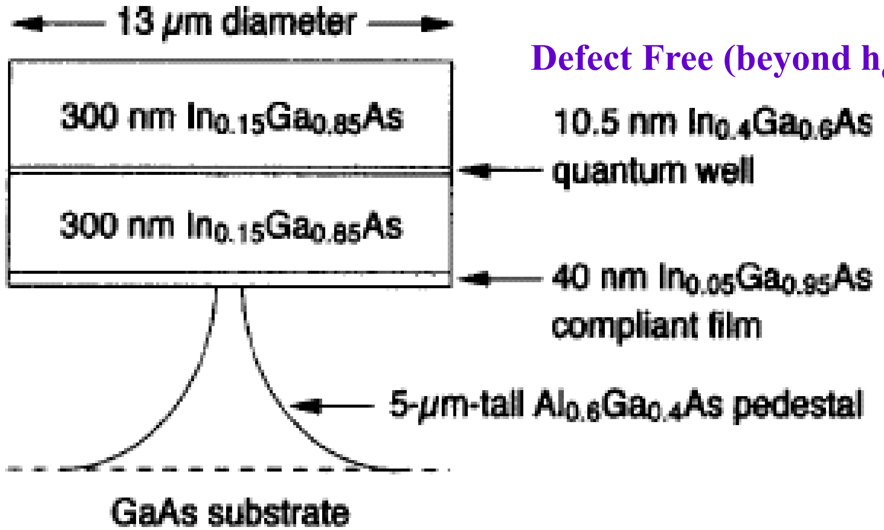
화합물 반도체 (II-3)
Heterostructure Growth

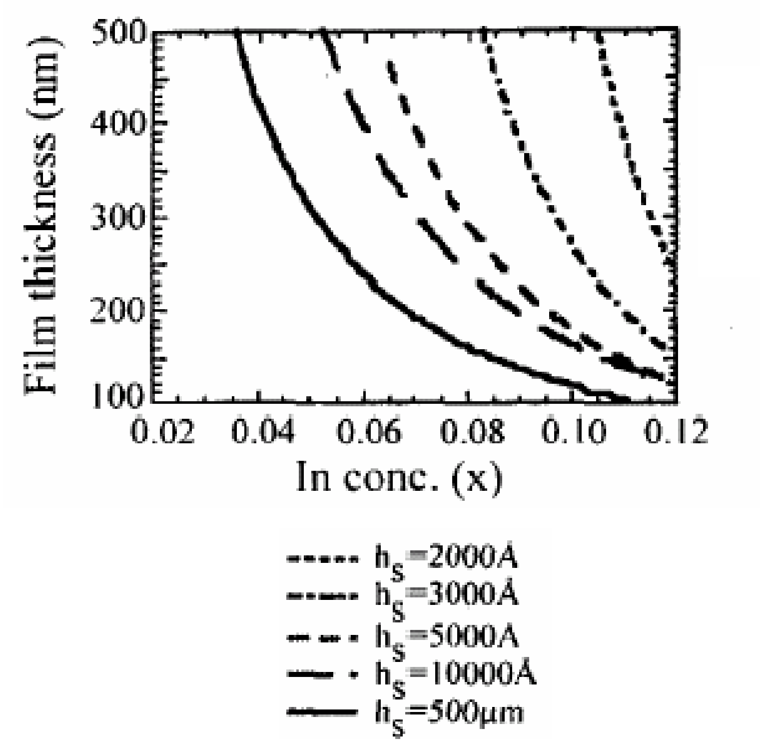
2007 / 가을 학기

Compliant Substrate : Thin Template decoupled from Mechanical Host

(Free-Standing Substrate)

Defect Free (beyond h_c)





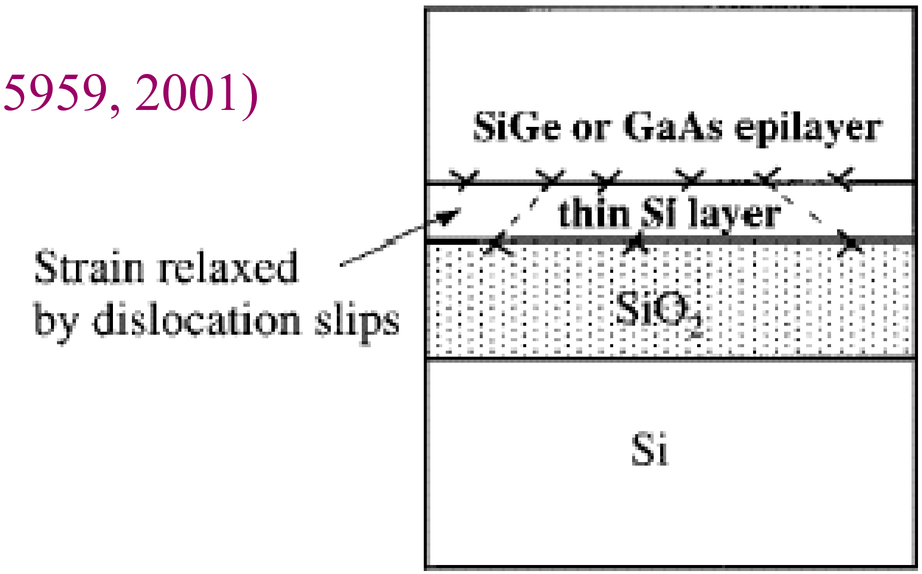
critical thickness of InGaAs on GaAs compliant substrate

- as a function of substrate thickness h_S

(Ref) Progress in Crystal Growth and Characterization, p. 1-55, 2000

SOI Compliant Substrate

(Ref. : J.A.P., p. 5959, 2001)



$Si_{0.6}Ge_{0.4}$

600°C, 1000 nm

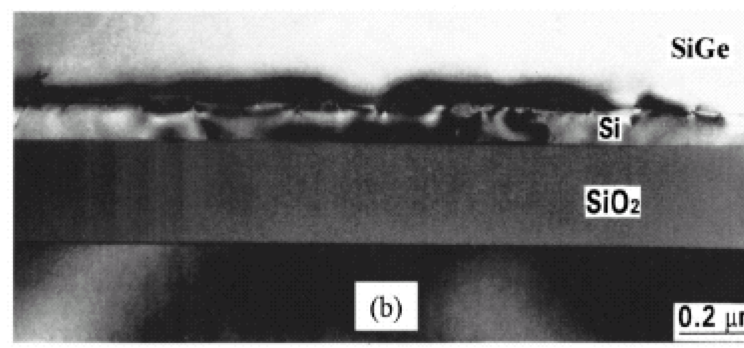
20 nm

200 nm

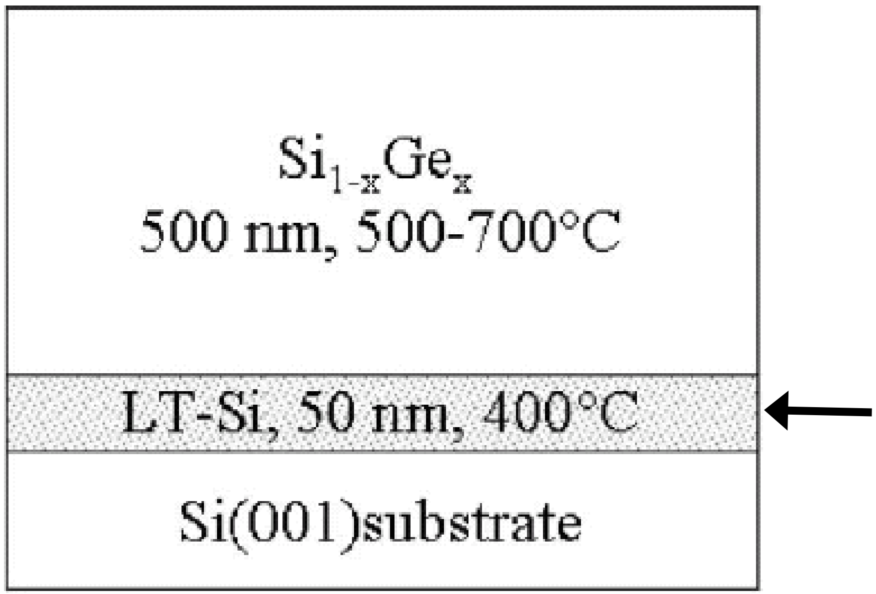
TABLE I. Theoretical dislocation density in SiGe (2% mismatch) grown on conventional Si substrates and SOI compliant substrates.

	Dislocation density in epilayers	
Epilayer thickness (nm)	grown on Si	grown on SOI
10	$5.4 \times 10^{10}/cm^2$	$5.4\times10^{8}/cm^2$
100	$1.6 \times 10^{7}/cm^2$	$1.6\times10^{5}/cm^2$
1000	$3.0 \times 10^{3}/cm^2$	$16/cm^2$

TEM Study of SiGe Thin Films



Low Temp. Si Compliant Substrate



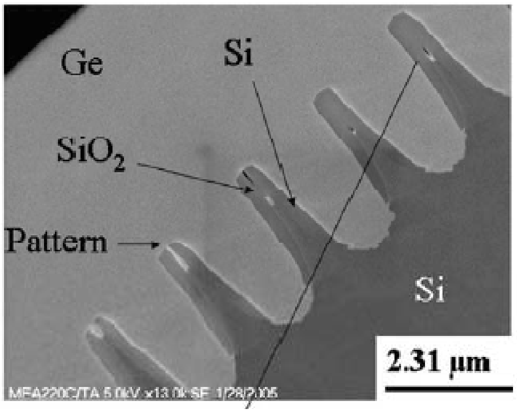
Large Vacancy Density $>10^{18}$ cm^{-3}
⇨ Reduced Elastic Constant

* Threading Dislocation Density : 10^6 cm^{-2} ⇨ 10^4 cm^{-2}
* Surface Roughness : 10 nm ⇨ 1 nm
* SiGe Buffer Thickness : 6~10 µm ⇨ 1 µm

(Ref) J. Crystal Growth, p. 761, 2001

Ge Growth on Structured Si Substrate

Ge growth on nanostructured Si



10 μm of Ge grown by CVD on Si off-cut 4° –5° in the <111>

Dislocation density

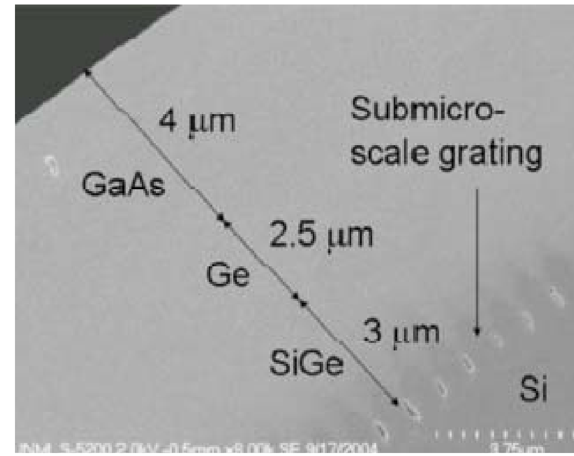
$6x10^{8}$ cm^{-2} (planar)

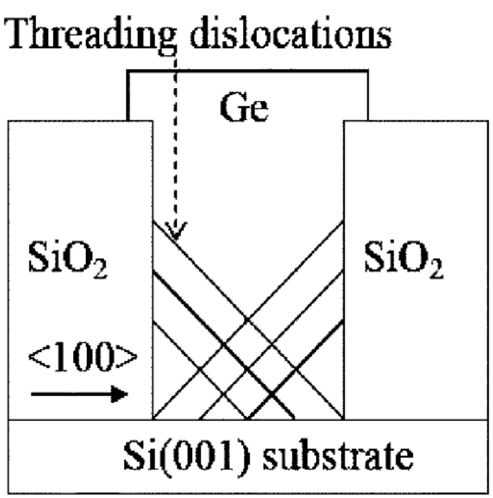
⇩

$5x10^{5}$ cm^{-2} (nanostructured)

(Ref.) G. Vanamu, APL, 2006

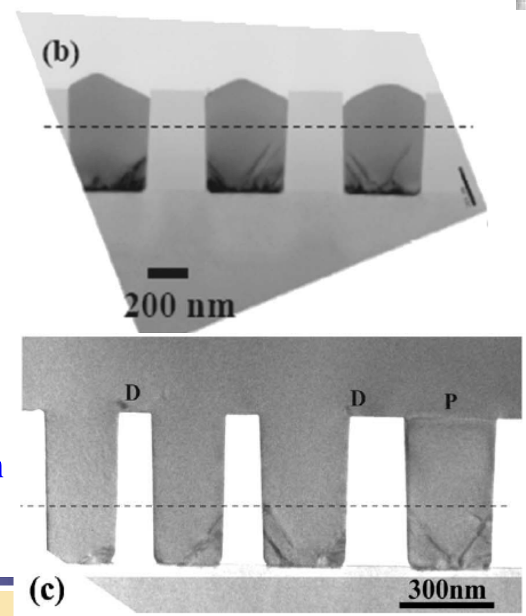
GaAs-Ge-Si growth





Ge growth on Si

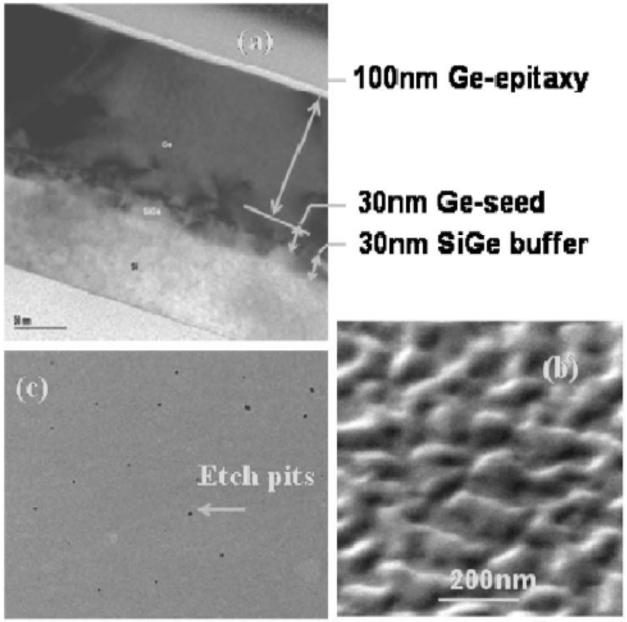
GaAs growth on Si



Regions of Ge up to 400 nm wide and free of near-surface defects have been demonstrated in SiO_2 trenches on Si using selective growth as thin as 450 nm.

(Ref.) Amberwave, APL, 2007

Ultrathin Low Temp. SiGe Buffer for Ge on Si



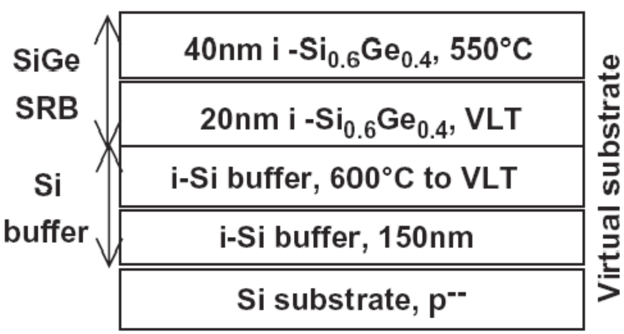
(550-600°C growth)

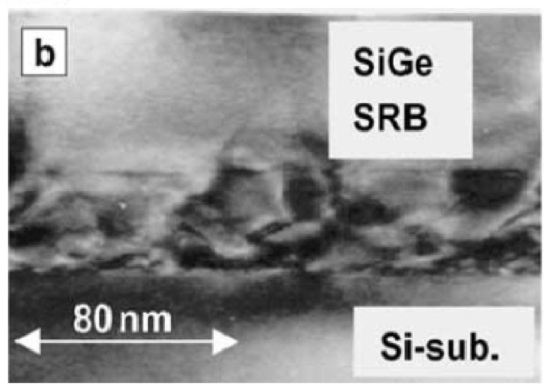
(Ref.) T. H. Loh, APL, 2007

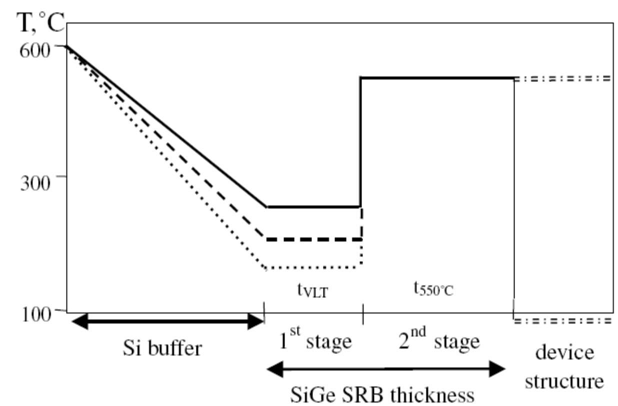
⇐ 350-400°C growth of SiGe buffer and Ge seed for the growth of high quality Ge epilayer on Si (100) by ultrahigh vacuum chemical vapor deposition

etch-pit density ~ 6×10^{6} cm^{-2}
rms surface roughnesses ~ 1.4nm

(Ref.) E. Kasper, Solid-State Electronics, 2004

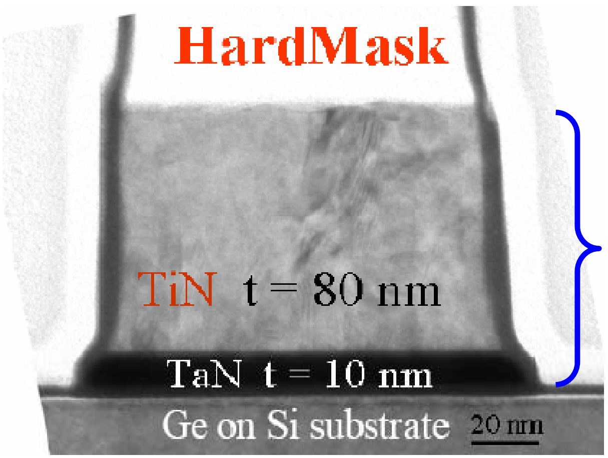






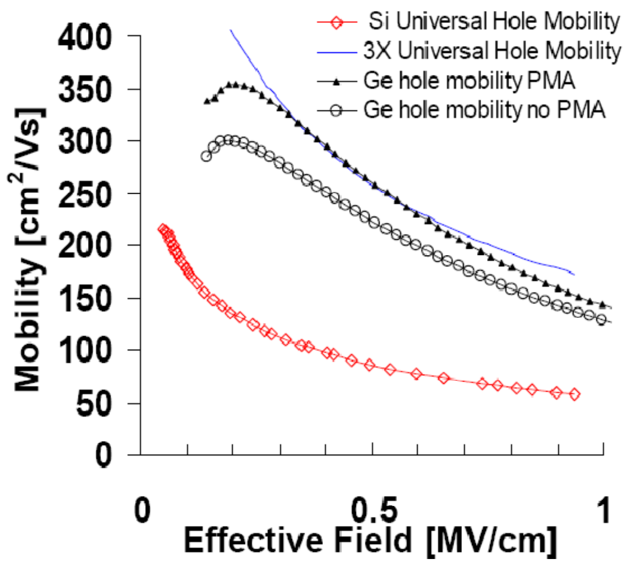
⇒ various devices demonstrated including 95nm n-MODFET

125nm Ge PMOS - IMEC (IEDM, 2006)

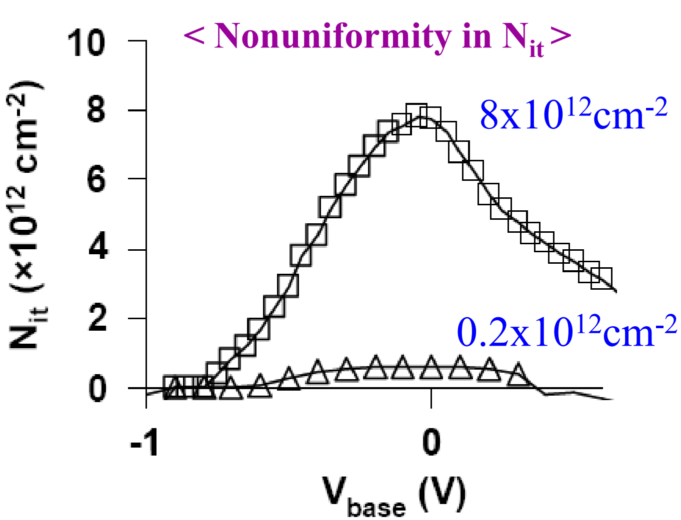


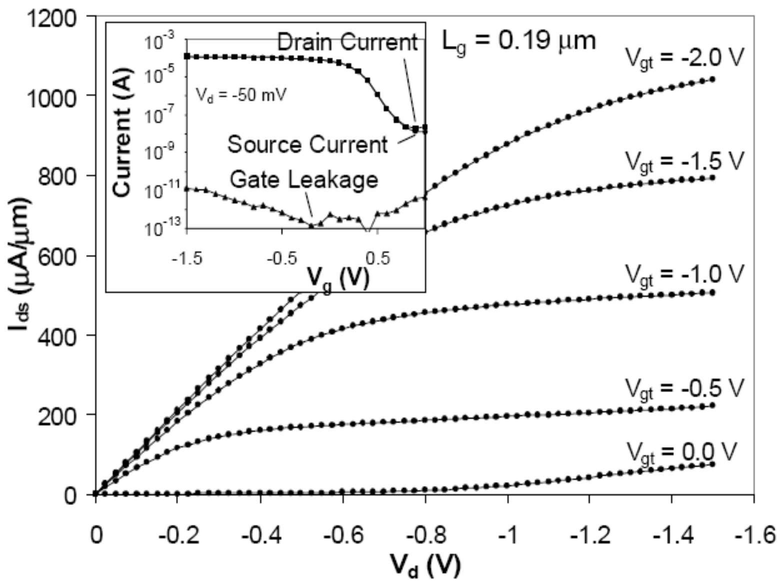
0.6nm epitaxial Si passivation
4 nm ALD HfO_2 dielectric
PVD TaN/TiN metal gate

process temperature ≤ 500°C



2 µm thick Ge layer grown on (100) Si
[dislocation density ; 10^7~10^8/cm^2]

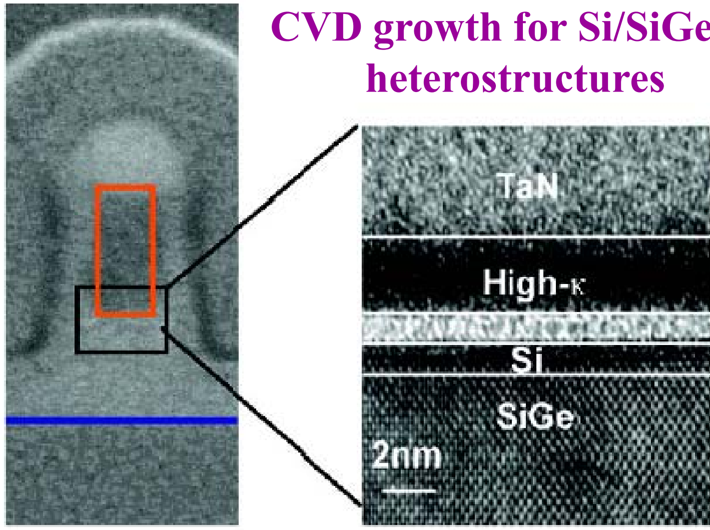




(Ref.) P. Zimmerman, IEDM, 2006

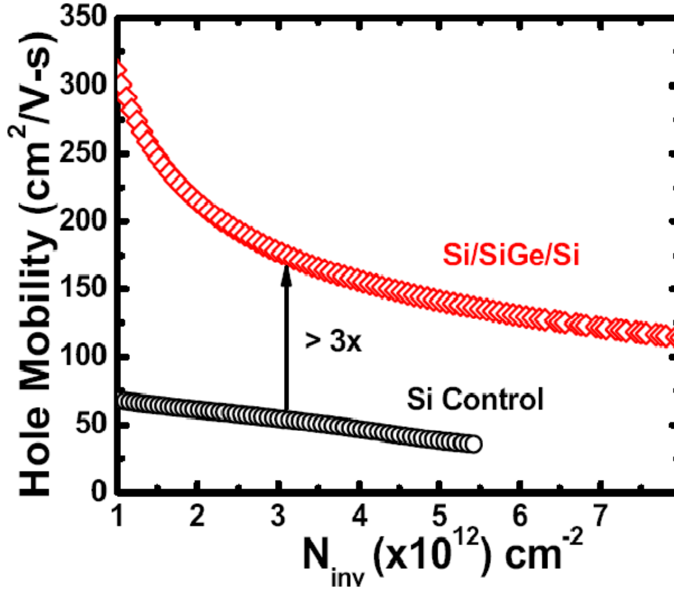
70nm Ge PMOS - SEMATECH (2007)

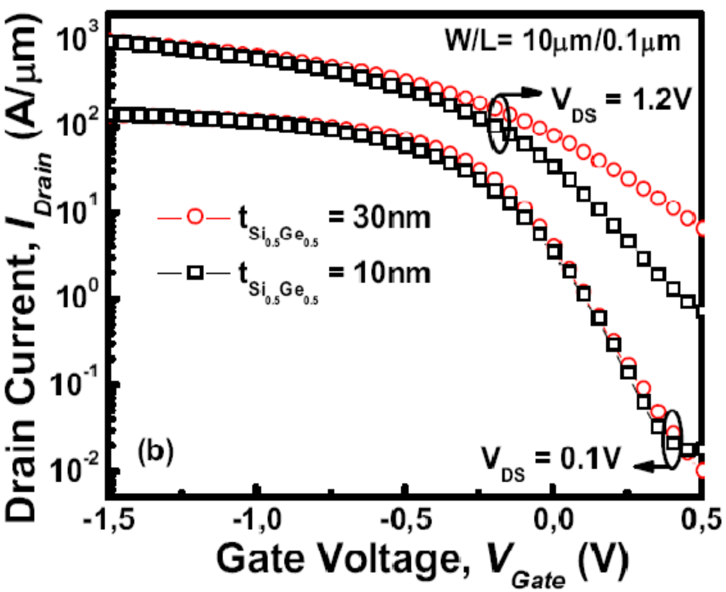
CVD growth for Si/SiGe/Si heterostructures



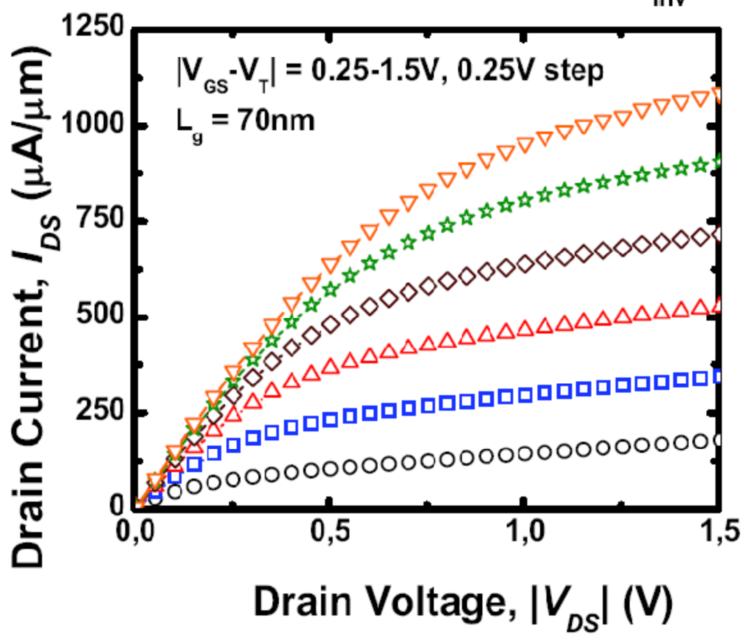
$HfSiO_x$

~1nm Si passivation





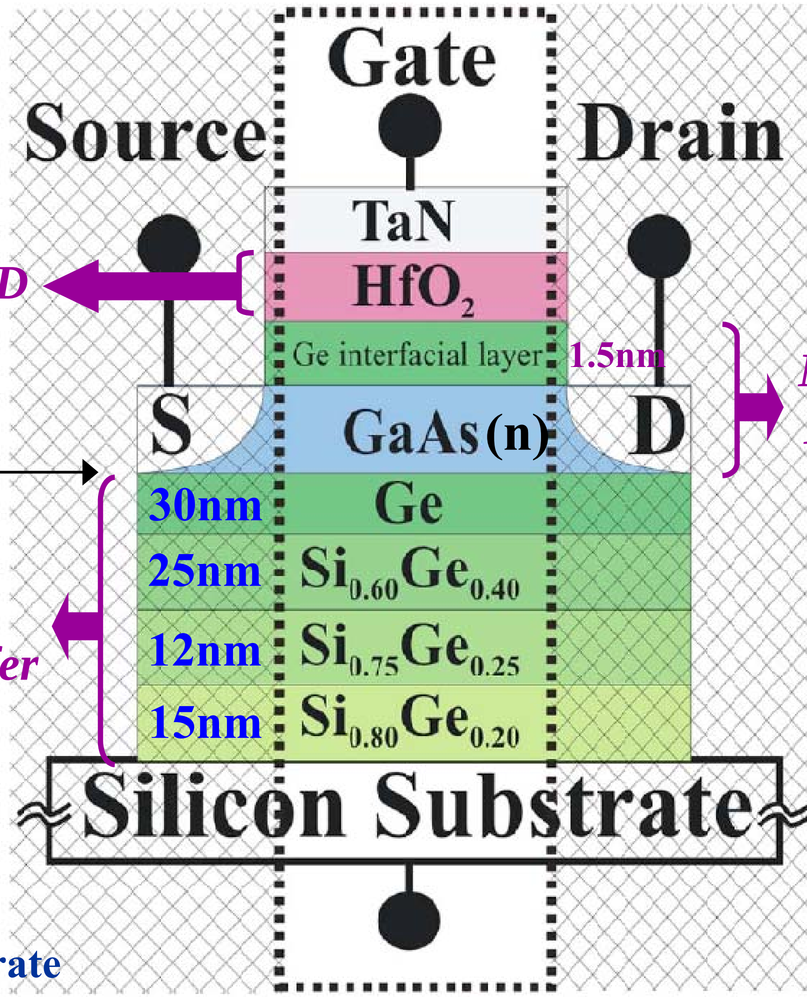
< 10nm $Si_{0.5}Ge_{0.5}$ for higher I_{on}/I_{off} >



(Ref.)

D. Q. Kelly, 2007

(Ref.) M. M. Oye, et al., J. Vac. Sci. Technol. B, p. 1098, May/Jun 2007



ALD

MBE
MEE

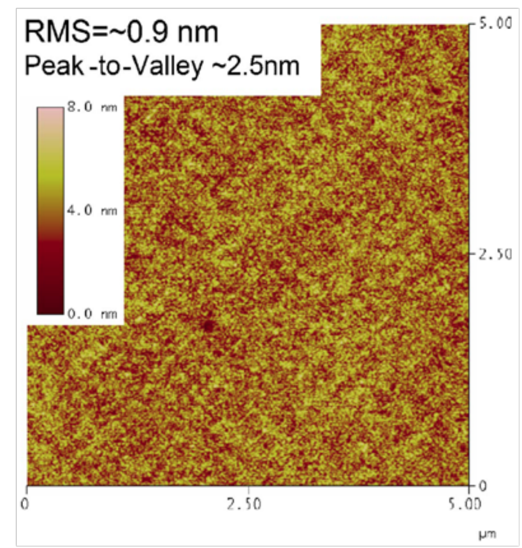
- 0.6nm surface roughness
- defects < $10^7 cm^{-2}$

UHVCVD for thin buffer

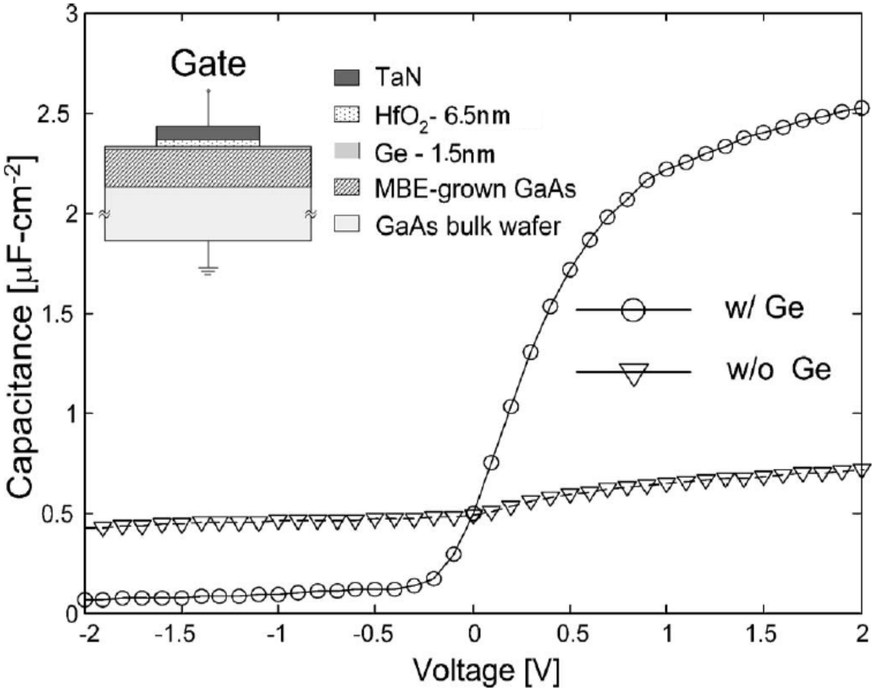
(100) Si substrate
6° degree off toward [110]

30-nm-thick GaAs layer grown on Si substrates

- low temperature (400°C) MEE-grown GaAs



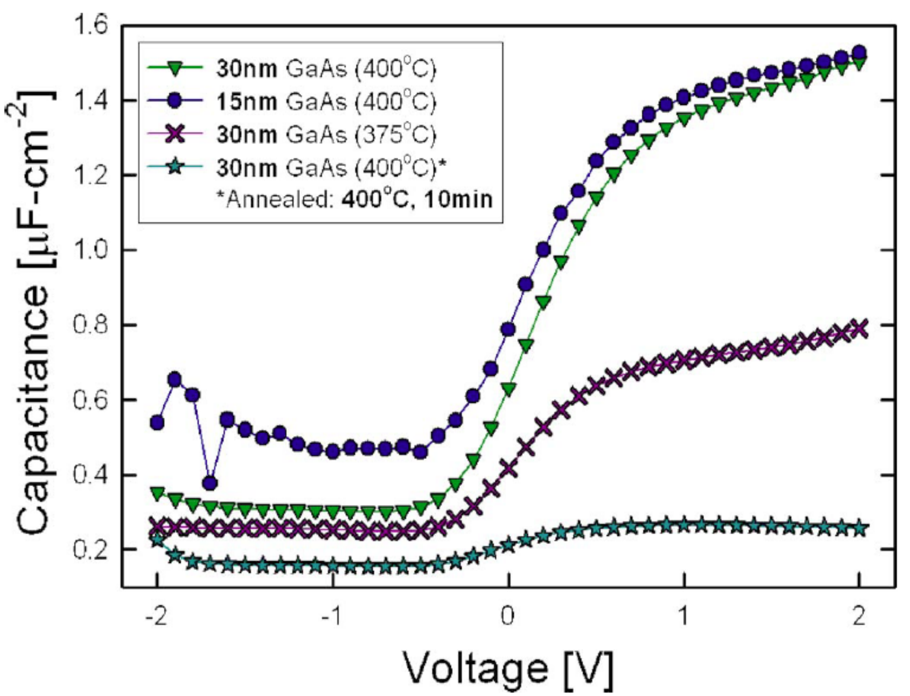
GaAs/Ge/Si Approach of U. Texas (II)



Ge interfacial layer의 효과

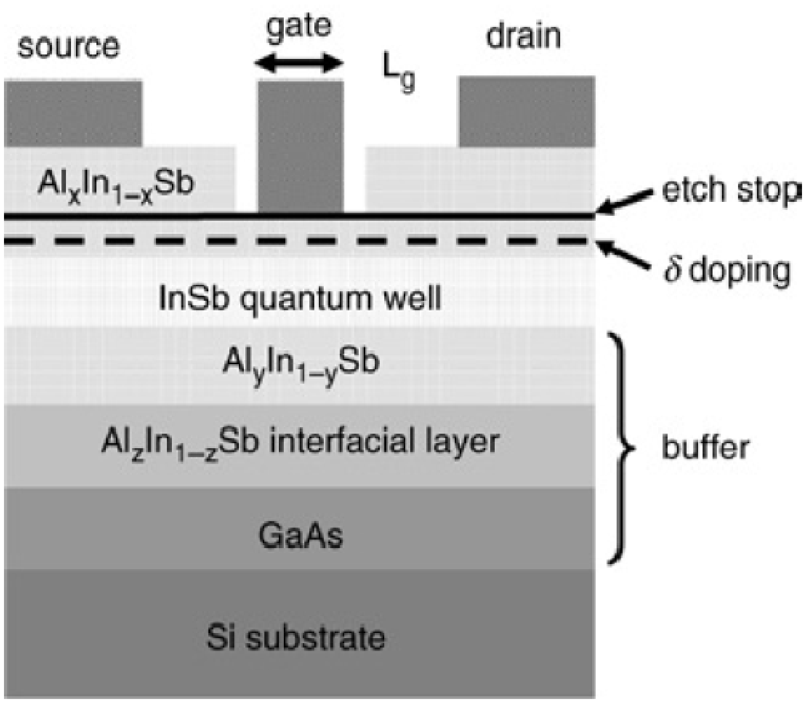
(Ref.) M. M. Oye, et al., J. Vac. Sci. Technol. B, p. 1098, May/Jun 2007

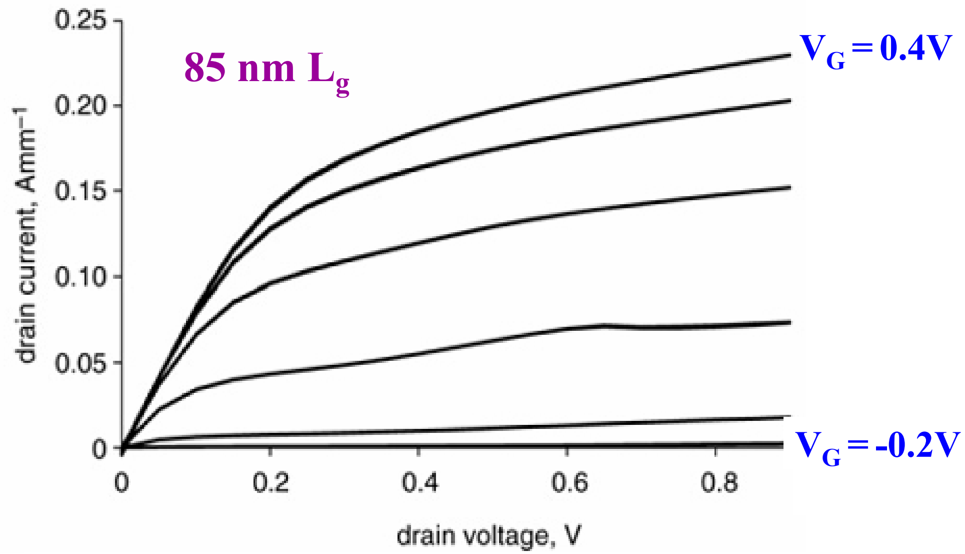
GaAs MEE 성장의 온도 및 후속 열처리의 영향

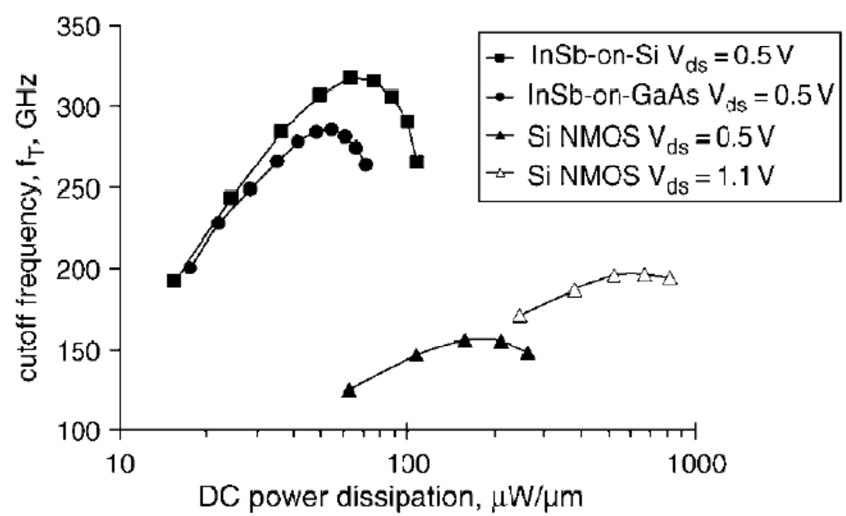


QinetiQ/Intel's InSb FET on Si

(Ref.) T. Ashley, EL 2007







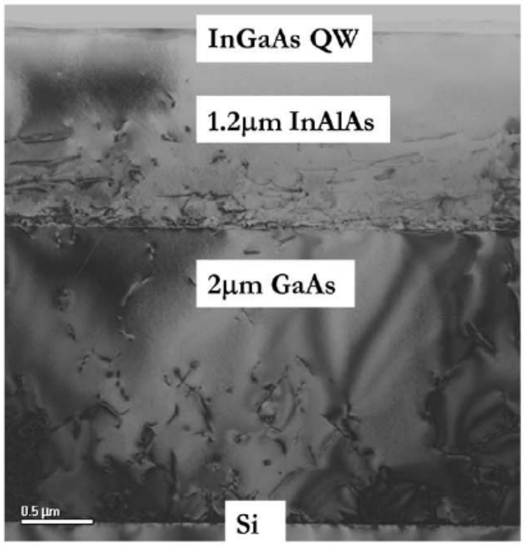
InSb QW transistor on 1.8 μm buffer on Si

- **intrinsic f_T=305GHz**
- **transconductance=710mS/mm at V_{ds}=0.5V**

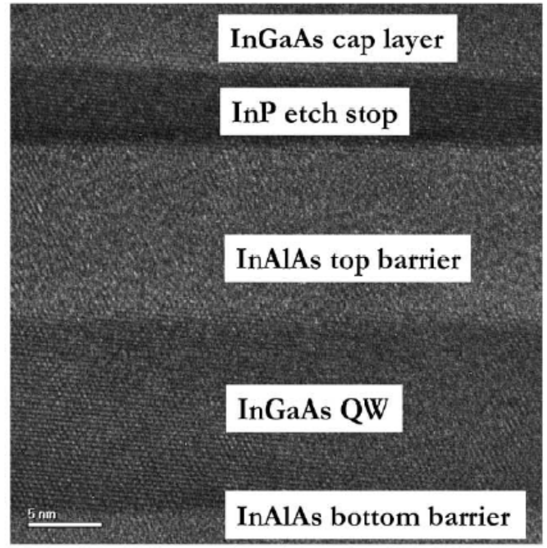
Intel/IQE's InGaAs QW-FET on Si

3.2µm metamorphic buffer

4° off-axis (100) p-type Si substrates

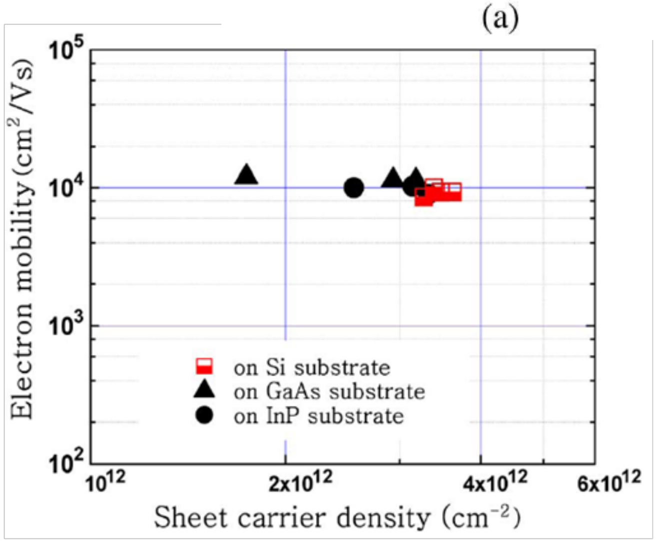


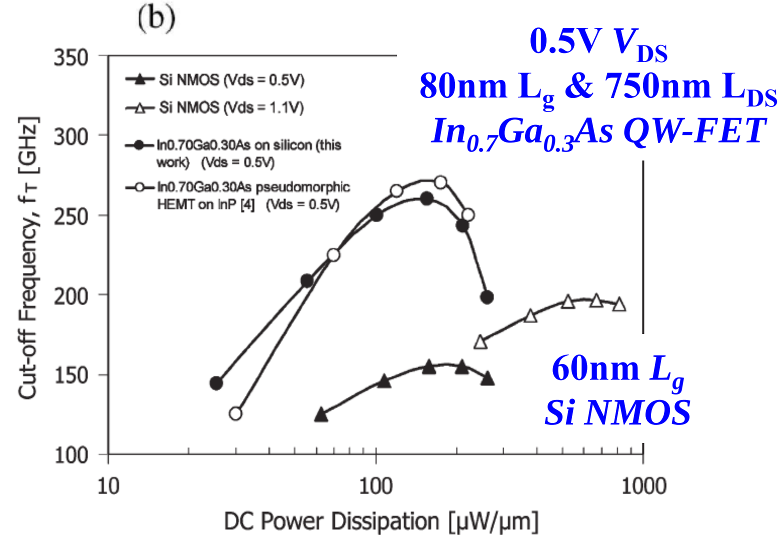
(a)



(b)

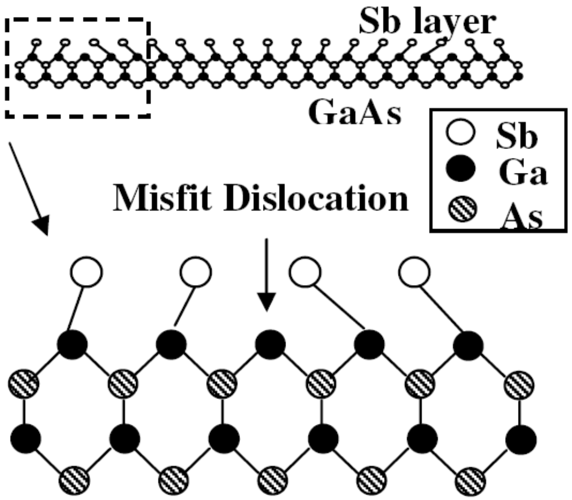
(Ref.) S. Datta, EDL 2007





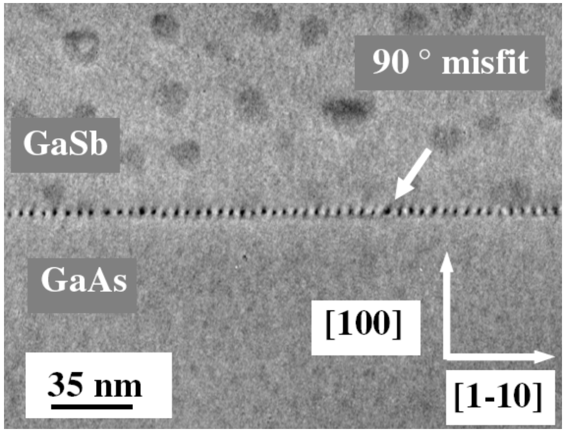
IMF Arrays for Lattice-Mismatched System

Schematic of periodic IMF



Dislocation Density
~ 6 x 10^5 cm^{-2}

Periodic IMF array (TEM)



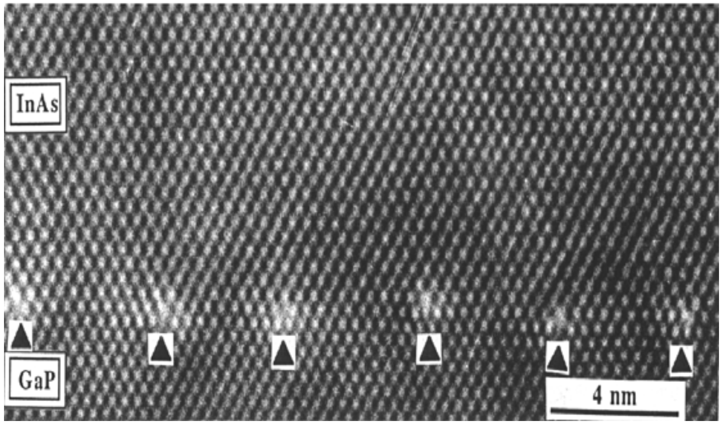
Interfacial Misfit Dislocations (IMF)

InAs on GaP

*** GaP is lattice matched with Si.**

(From Jerry Woodall)

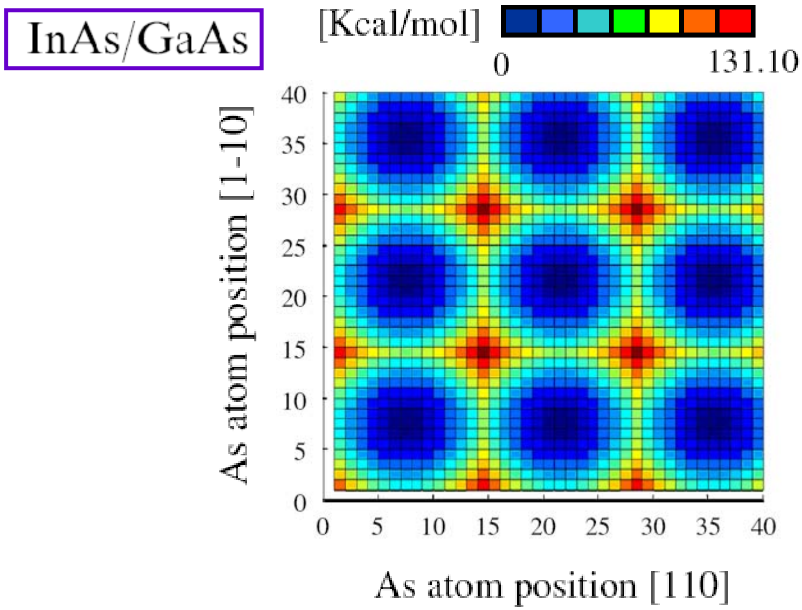
(Ref.) V. Gopal, J. Vac. Sci. Technol. B, p. 1767, Jul/Aug 1999

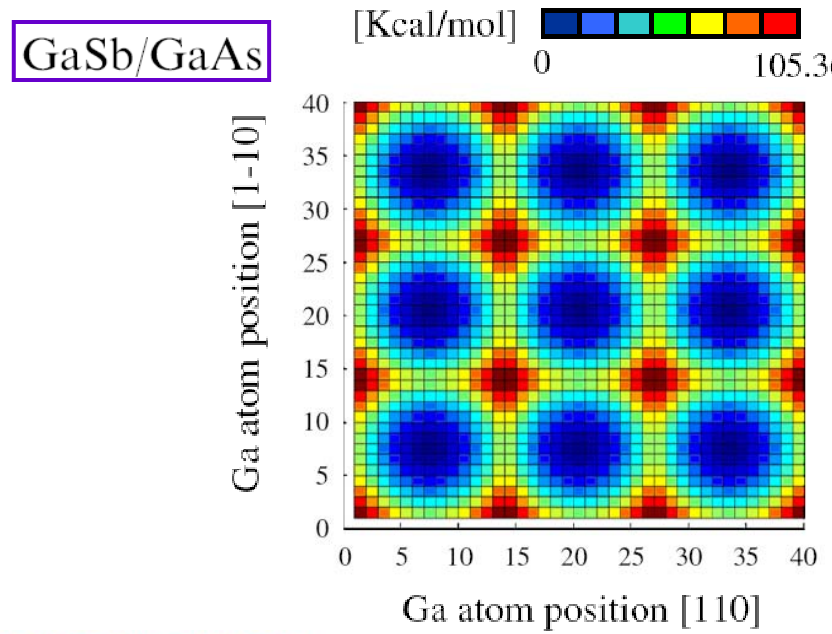


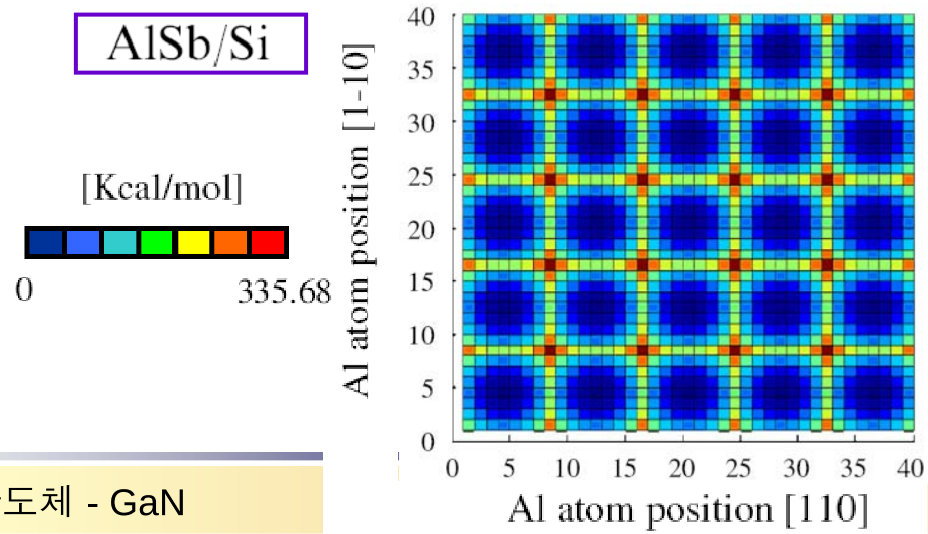
IMF ➪ ionized donor 10^{13} cm^{-2}

Dislocation Density ; 10^{10} cm^{-2}

Molecular-Mechanics Simulation of IMF Arrays

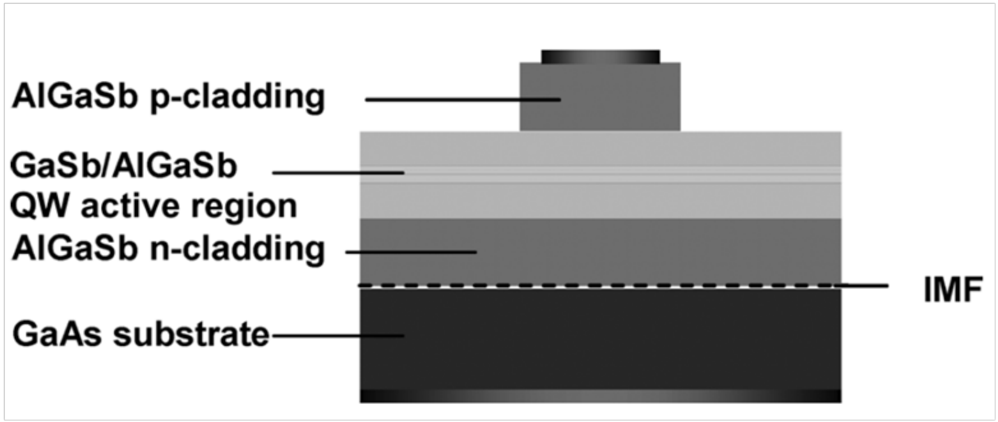




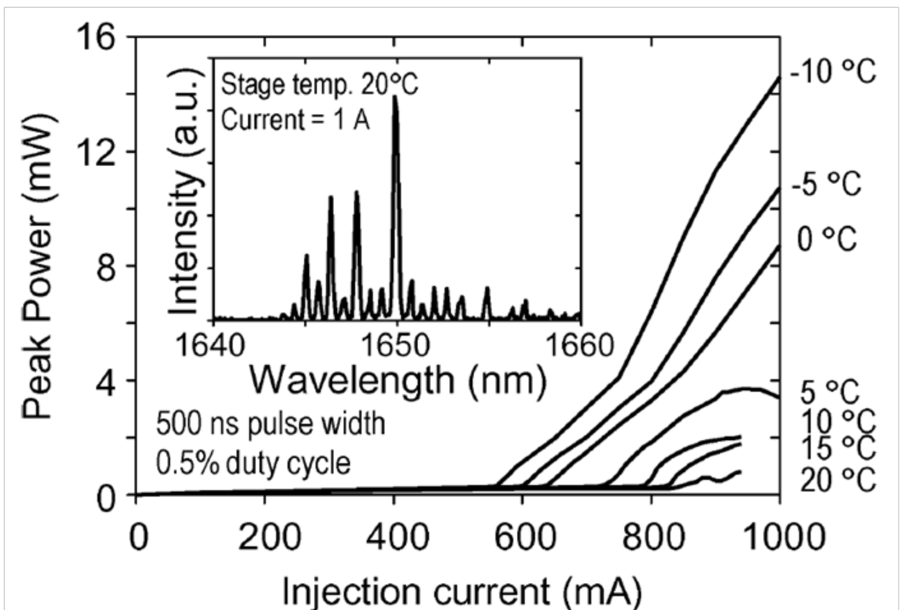


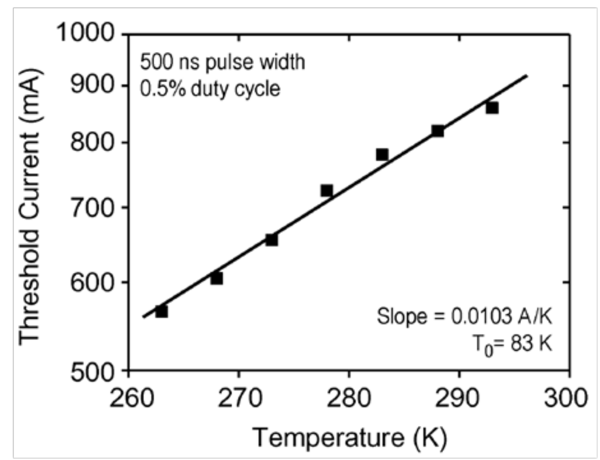
(Ref.) A. Jallipalli, J. Crystal Growth, p. 449, 2007

GaSb Laser on GaAs Substrate utilizing IMF Arrays



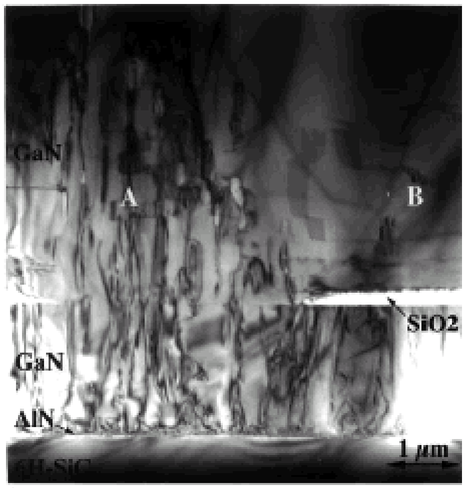
(Ref.) M. Mehta,
IEEE Photonics Tech.
Lett., p. 1628, 2007

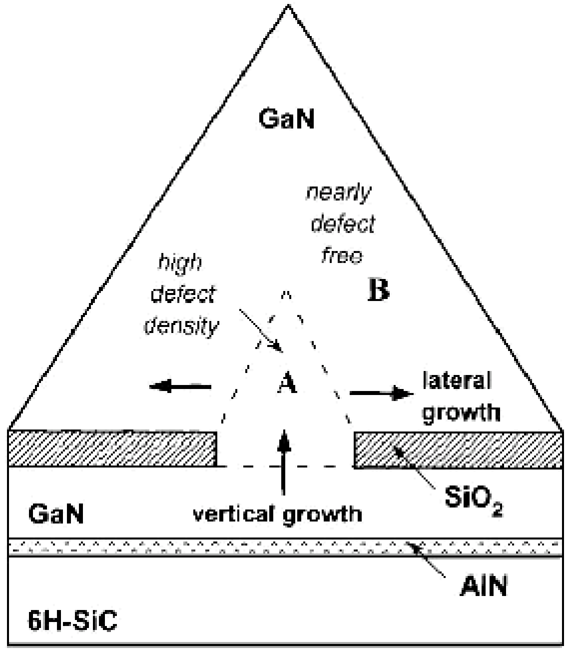


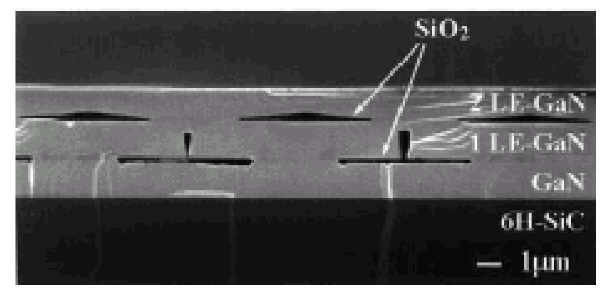


$T_0 = 83K$

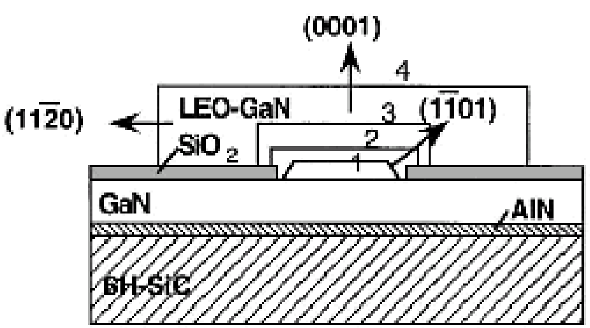
Lateral Epitaxial Overgrowth (LEO) of GaN Layers

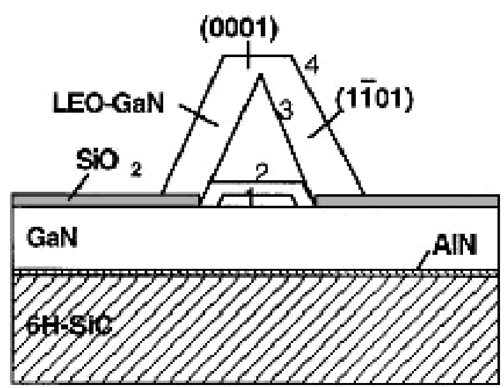






Double LEO
GaN Heterostructures

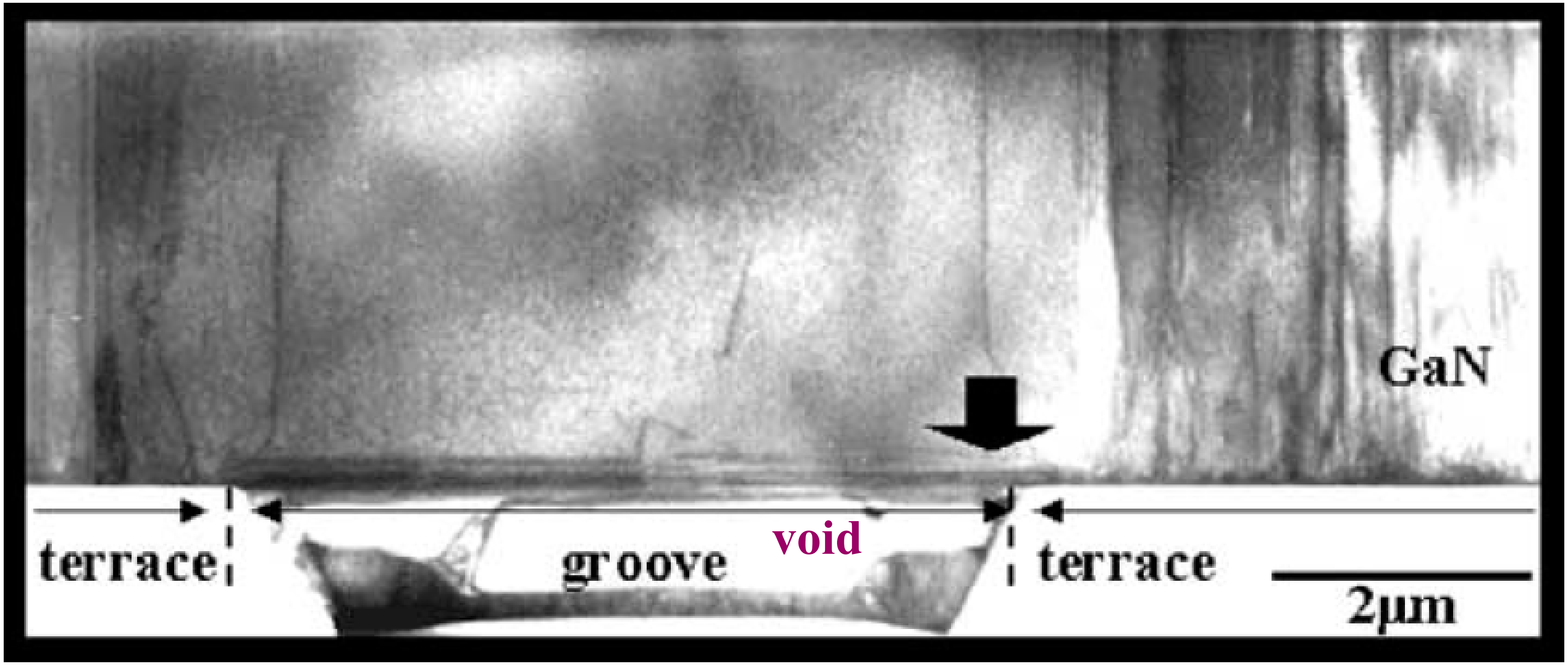




MOCVD Growth with Periodically Grooved Substrate

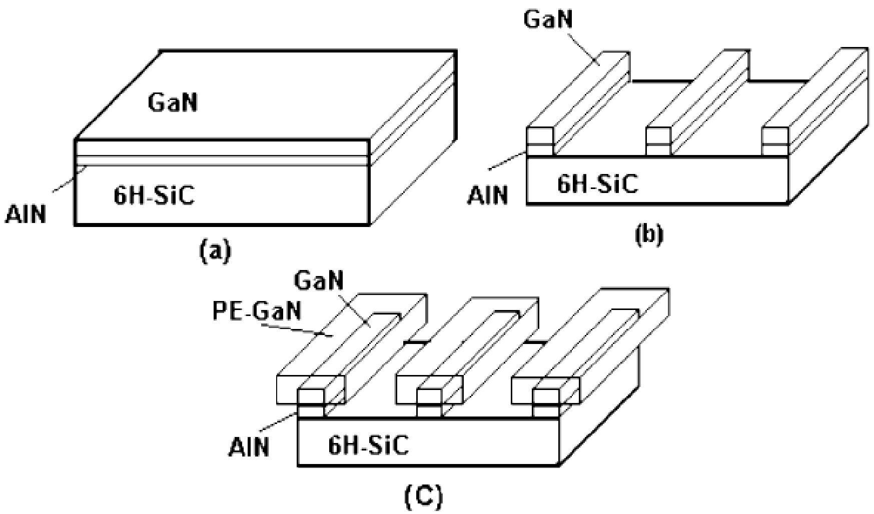
threading dislocation densities ~ 2x10^{7} cm^{-2}

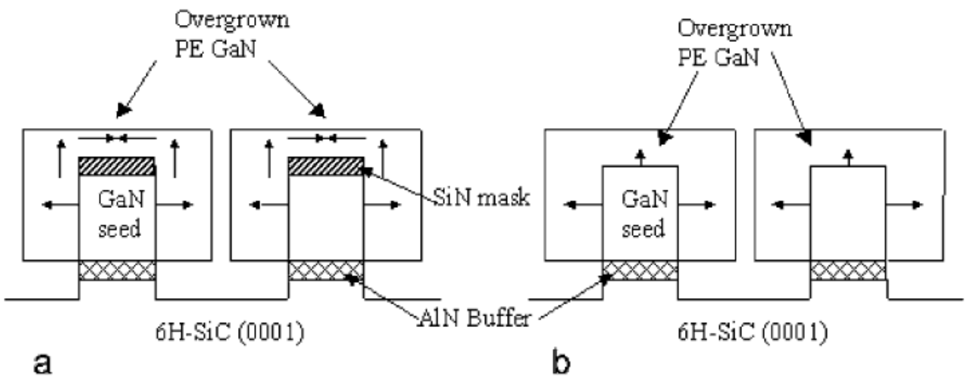
TD densities ~ 2x10^{8} cm^{-2}

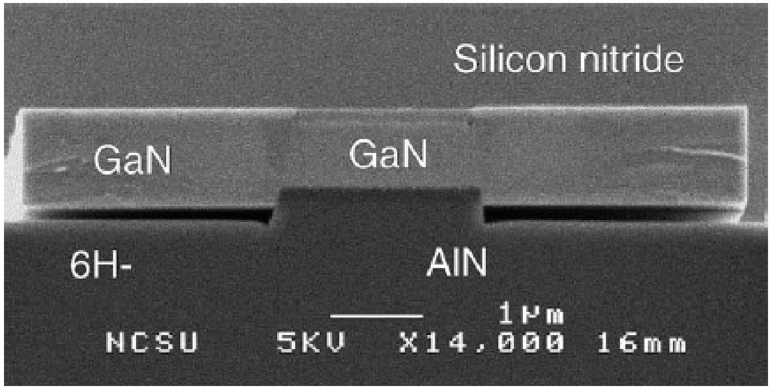


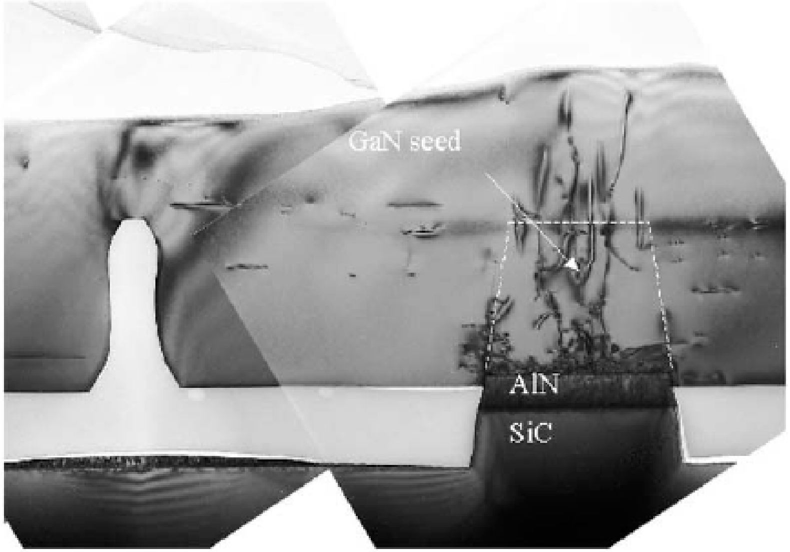
Ref.: S. Mochizuki, et al., Journal of Crystal Growth, pp. 1065–1069, 2002

Pendeo-Epitaxy



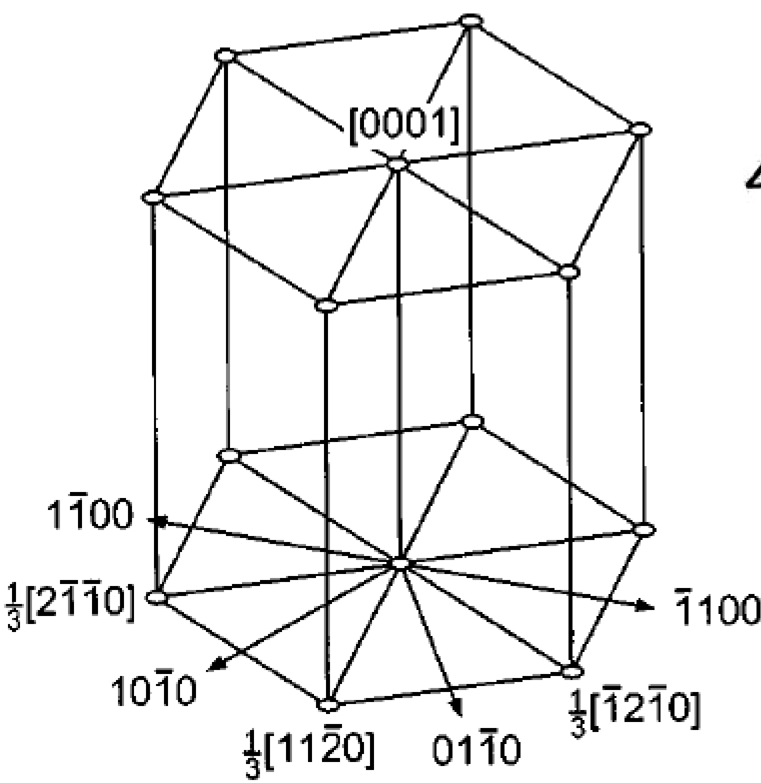


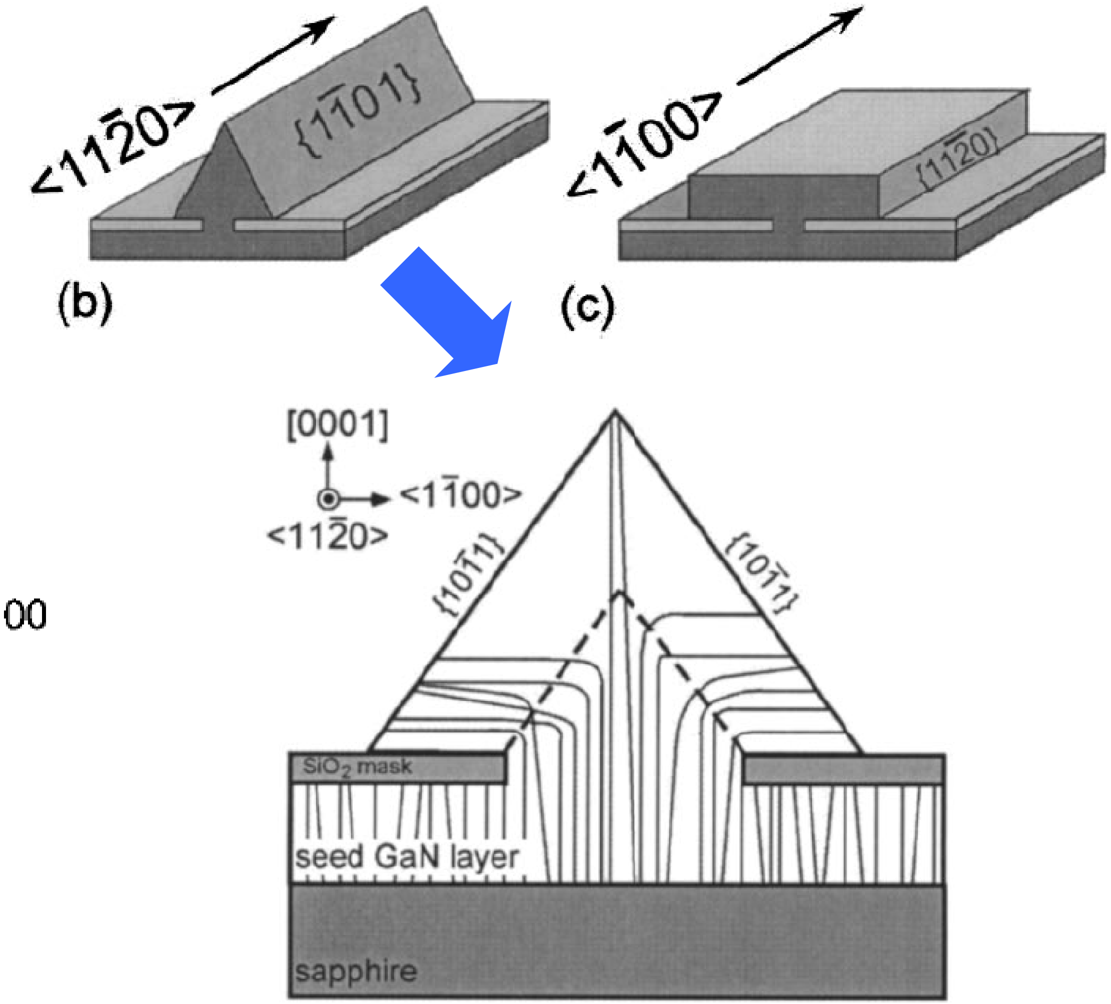




Ref.: R. F. Davis, et al., Acta Materialia 51, pp. 5961–5979, 2003

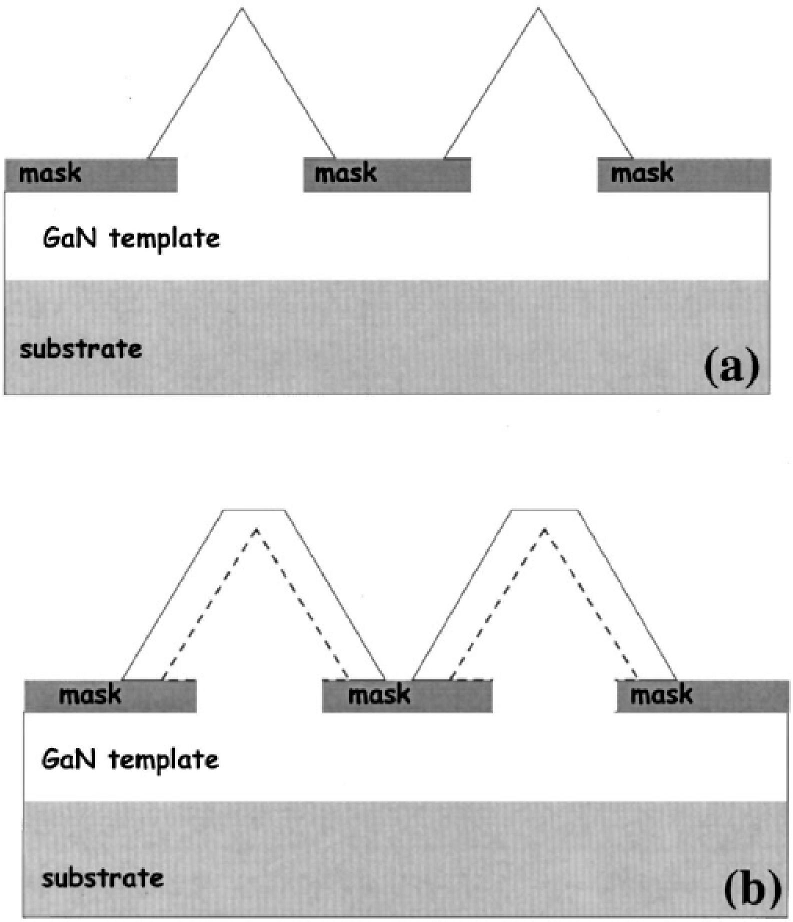
Orientation-dependent Growth in ELO

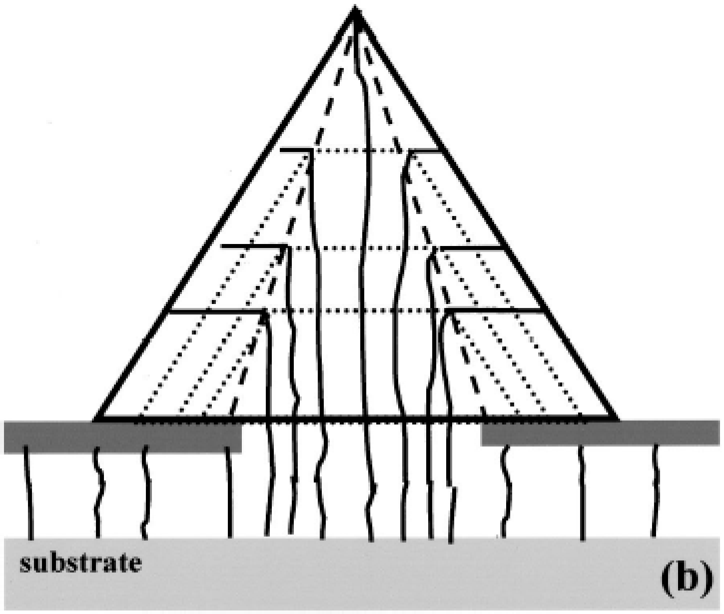




Ref. : A. E. Romanov, et al., J. Appl. Phys., pp. 106-114, 2003

Two-Step ELO

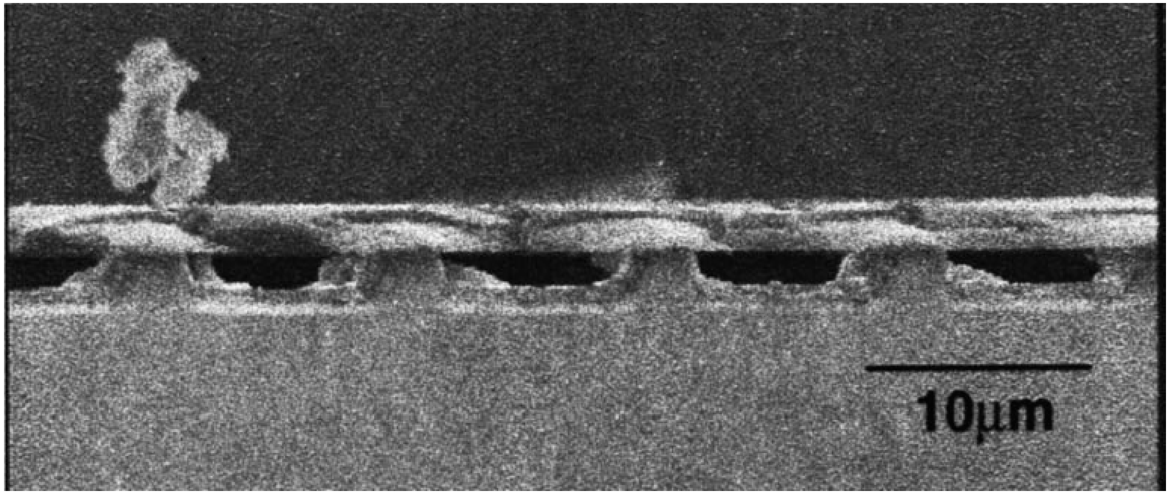




Dislocation density
- 2×10^7 cm^{-2} over the entire surface

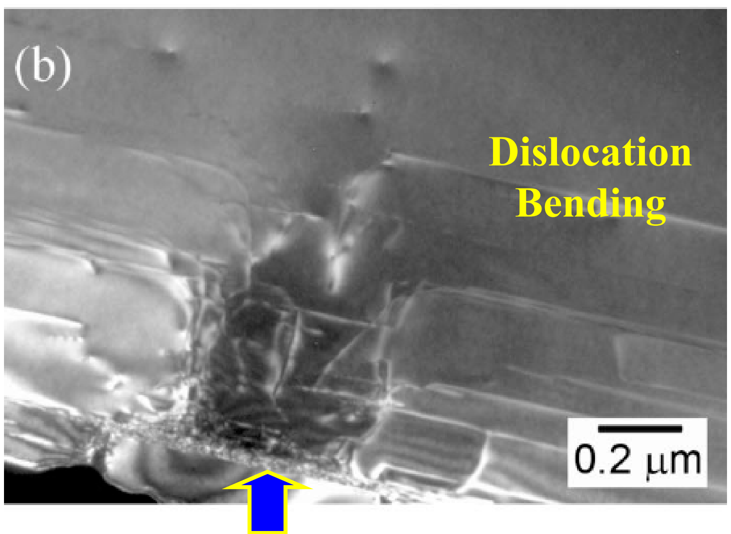
Ref. : P. Vennegues, et al., J. Appl. Phys., pp. 4175-4181, 2000

Cantilever Epitaxy – Effects of Mesa Width

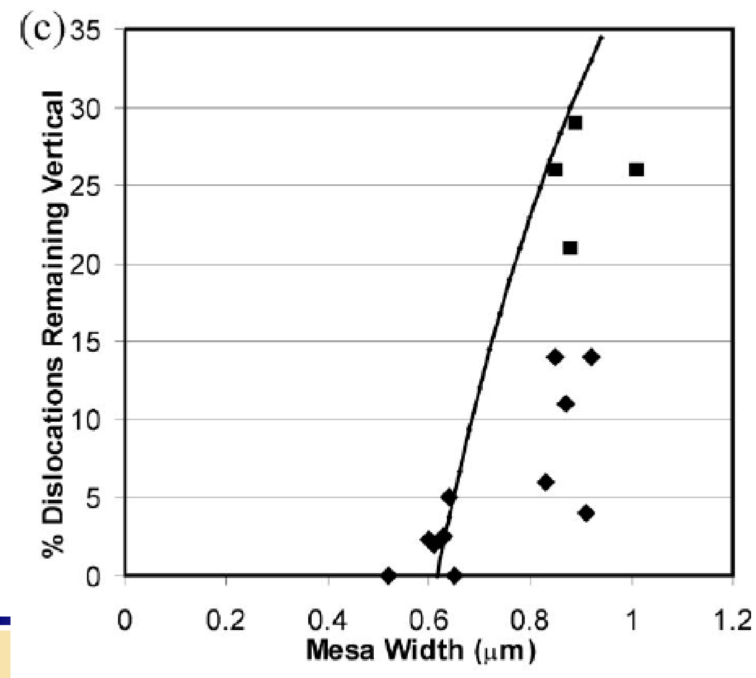


- **dislocation densities $3 – 5x10^7/cm^2$ for 0.75μm mesa width**

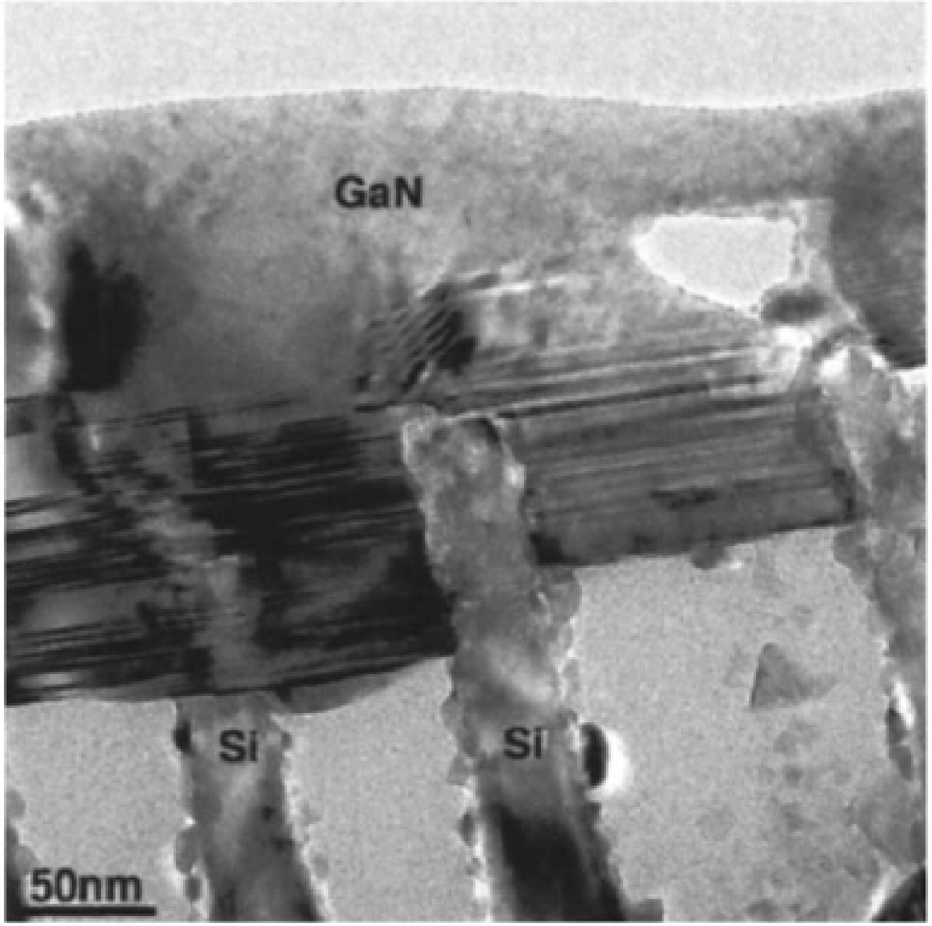
Ref. : D. M. Follstaedt, et al., Appl. Phys. Lett., pp. 2758-2760, Oct. 2002



Mesa width 0.65 μm



Nanoheteroepitaxy of GaN on Si Nanopillar Arrays

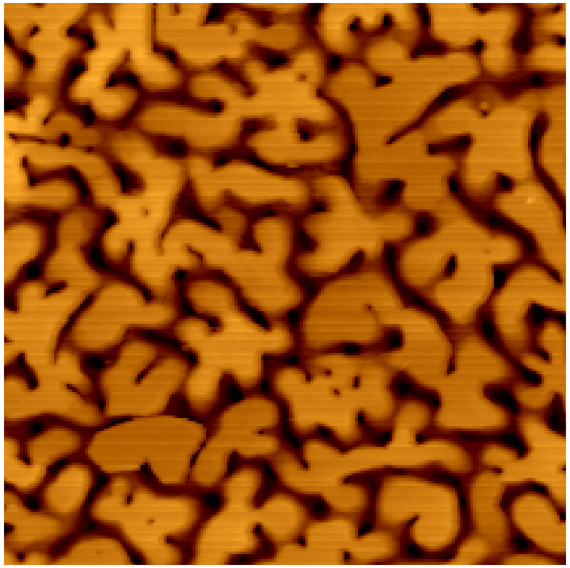


- Si nanopillars on a (111) Si substrate with an anodic-Al_2O_3 membrane, etch-mask process
- The diameter of nanopillars ~ 20–60 nm with spacing of 110 nm
- **dislocation densities - below $10^8/cm^2$ (mainly stacking faults)**

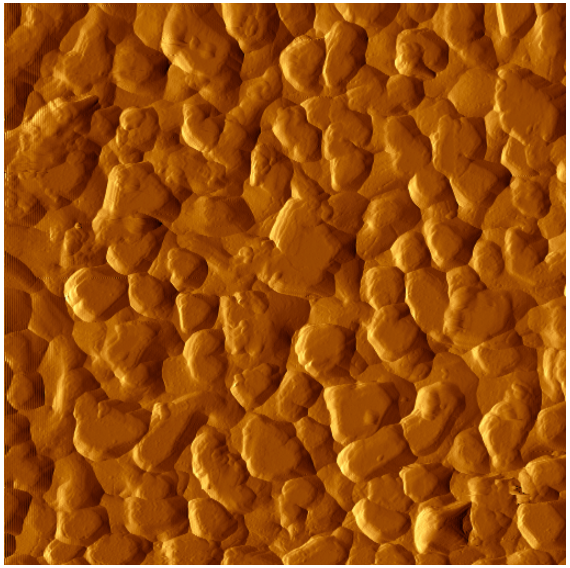
Ref. : S. D. Hersee, et al., J. Appl. Phys. 97, 124308, 2005

Surface Morphology of Ga/N-Face GaN

N-Face GaN



Ga-Face GaN



Defect (cm^{-3})	HVPE GaN Ga polar	HVPE GaN N polar
[O]	4×10^{17}	2×10^{19}
[Mg]	4×10^{16}	2×10^{17}
[C]	5×10^{16}	2×10^{17}
[V_{Ga}]	$\leqslant10^{15}$	7×10^{17}

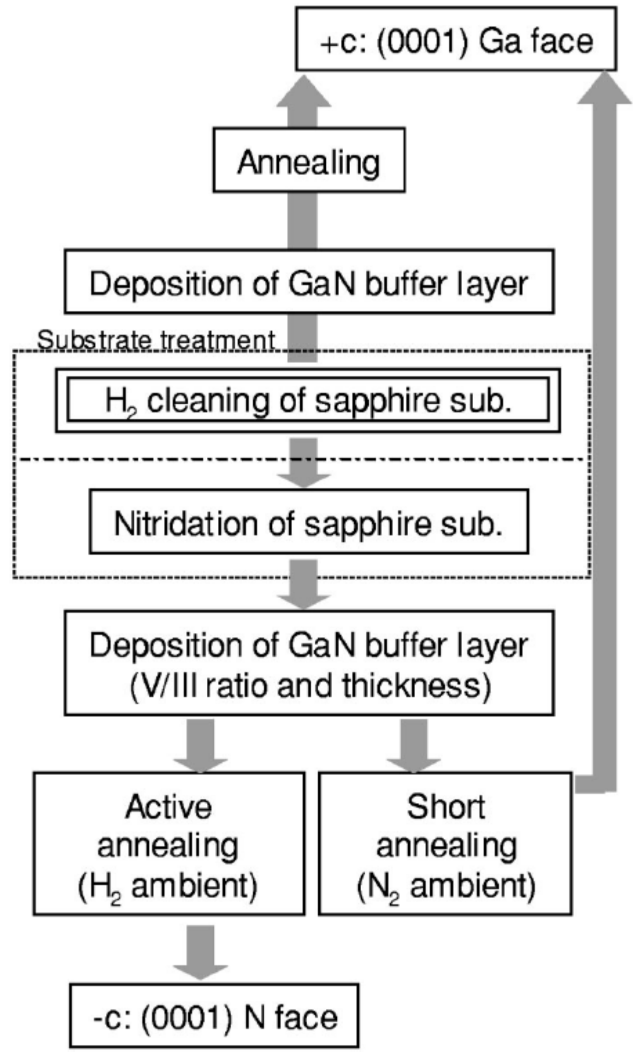
N-face GaN is rough and discontinuous, with more impurities and defects, and poor optical and electrical properties.

Control of GaN Surface Polarity in MOCVD Growth

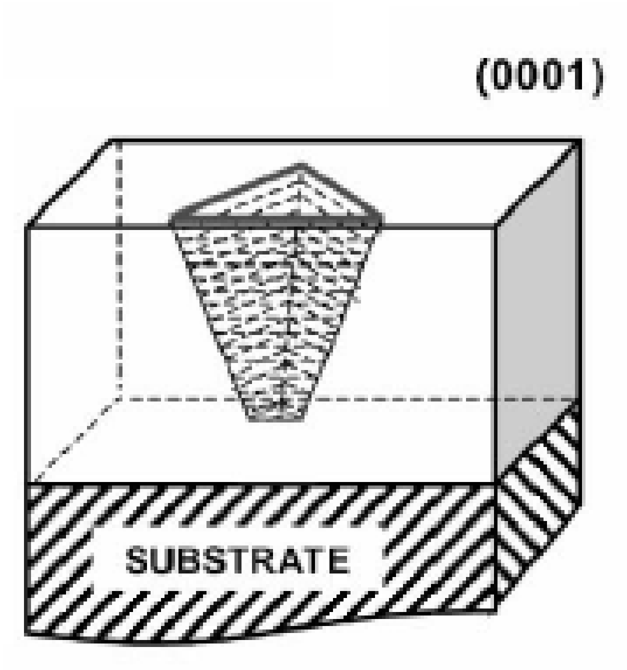
MOCVD Growth Conditions on Sapphire Substrate

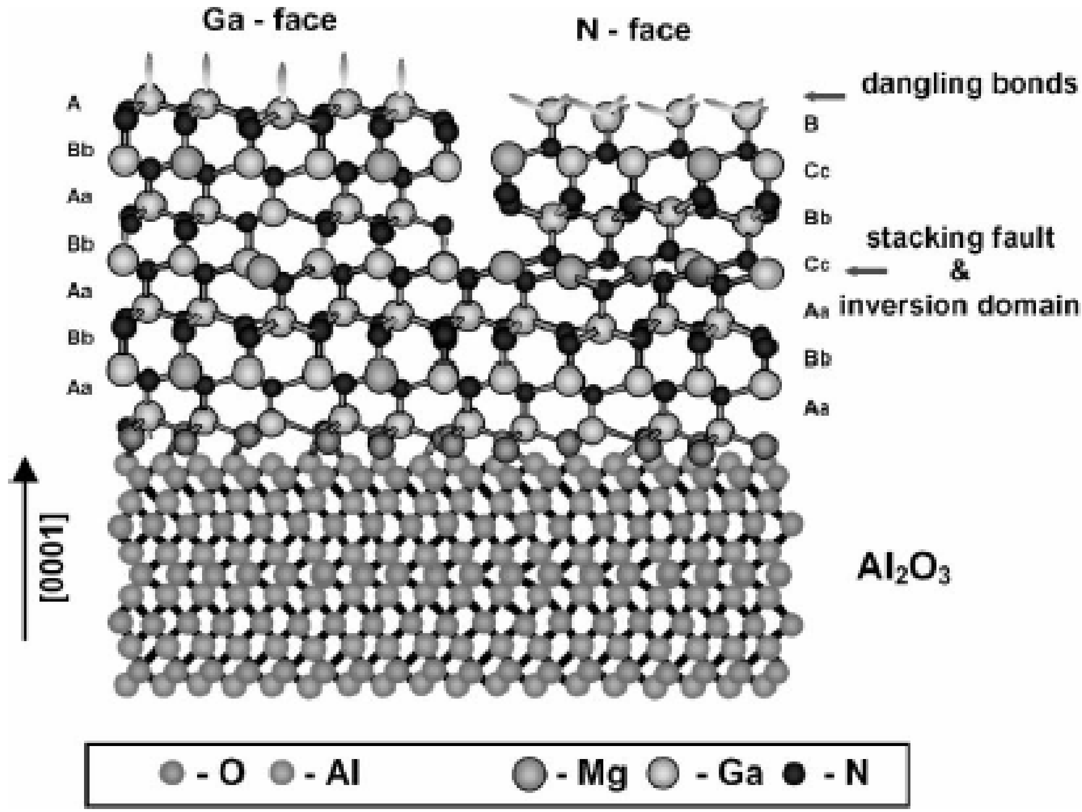
H_2 cleaning	Nitridation	V/III ratio of 20 nm buffer layer	Annealing ambient $H_2:N_2:NH_3$ (sccm)	Annealing time (min)	HT GaN layer
H_2 flow at 1080 °C for 10 min	None	5000[a]	750:500:750[a,b] 0:1250:750[c]	0–40	V/III ratio: 15 000 1.2 μm
	NH_3 flow at 1080 °C for 5 min	20 000[a)]	1250:0:750[d] 750:500:750		
		2000	750:500:750 0.1250:750		

Ref.: M. Sumiya, et al., J. Appl. Phys., pp. 1311-1319, Jan 15, 2003



Piramidal Inversion Domains



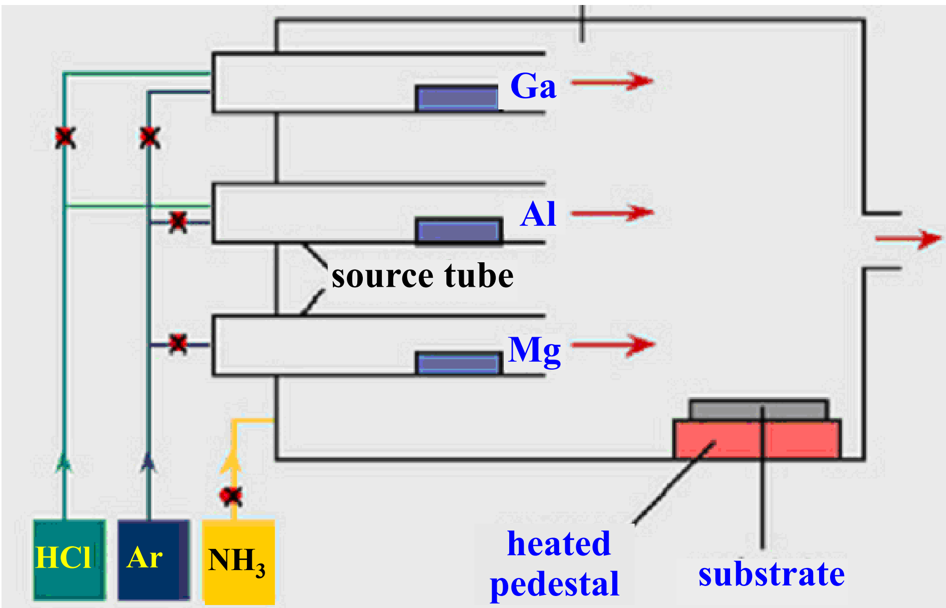


G. Martinez-Criado, et al, "Study of inversion domain pyramids formed during the GaN:Mg growth," Solid-State Electronics, p. 565-568, 2003

HVPE-Grown Quasi-Bulk GaN

Hydride Vapor-Phase Epitaxy (HVPE)

Furnace with different temperature zones



Ga + HCl → GaCl (800-900°C)

GaCl + NH_3 → GaN (1000-1100°C)

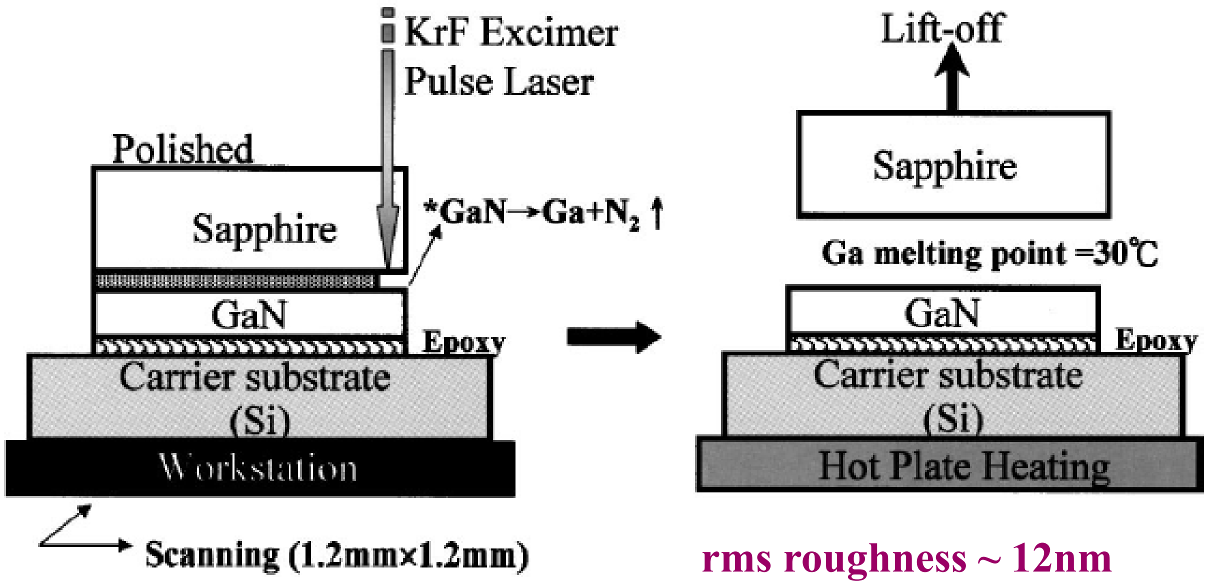
* Substrate separation after growth

- up to 100μm/hr growth rate
- ~ 1/10 consumption of NH_3 compared with MOCVD
- ~ 1/10 low cost of pure metals-

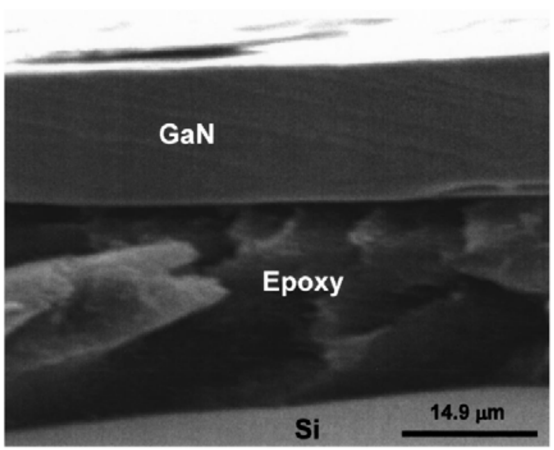
- 330 and 400 μm thick GaN wafers in three sizes (10 mm, 18 mm and 2 inch)
- Cree offers $ 2,400 for a 0.5 inch GaN substrate
- dislocation densities as low as 3×10^6 cm^{-2}

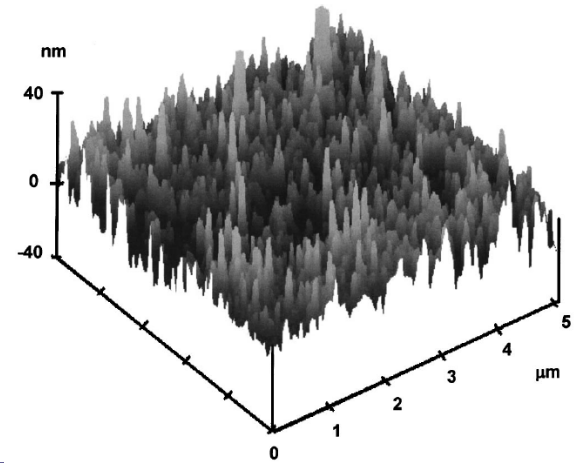
* TDI - HVPE-grown GaN-on-sapphire template for LED epi-growth. ($120 for 2 inch)
- 2~5 μm GaN buffer with dislocation densities of 10^8 cm^{-2} (without low-temp. buffer)

Laser Lift-off for GaN HVPE Film



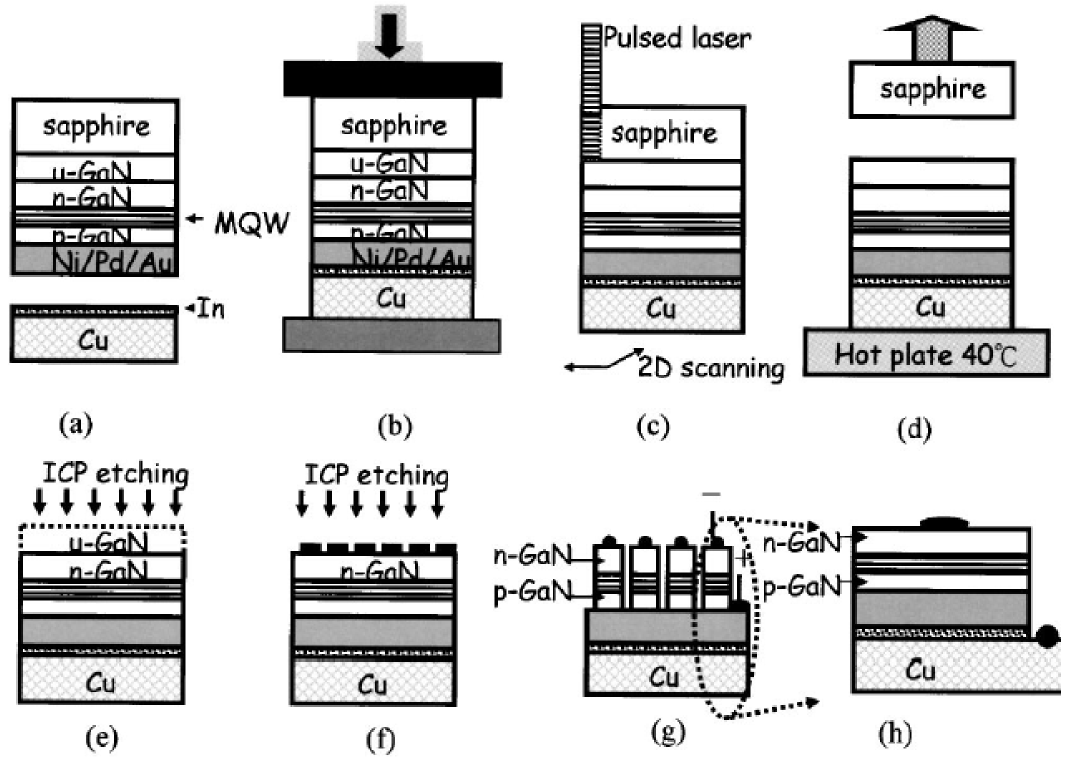
rms roughness ~ 12nm
degraded region ~ 50nm

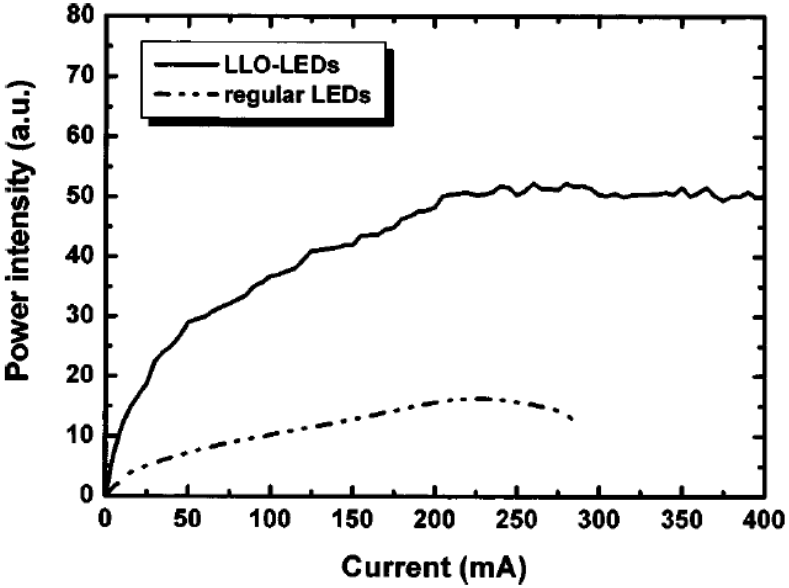




Ref. : III-V Nitride Semi-conductors, Chap. 3

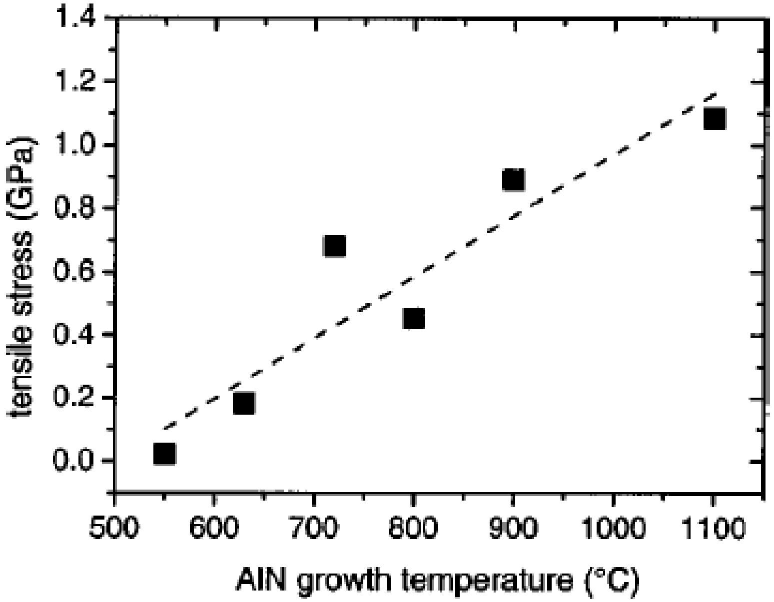
GaN LED Fabricated by Laser Lift-off Technique





Ref. : C-F. Chu, et al., J. Appl. Phys., pp. 3916-3922, April 2004

Stress Reduction with Low-Temperature AlN Interlayer



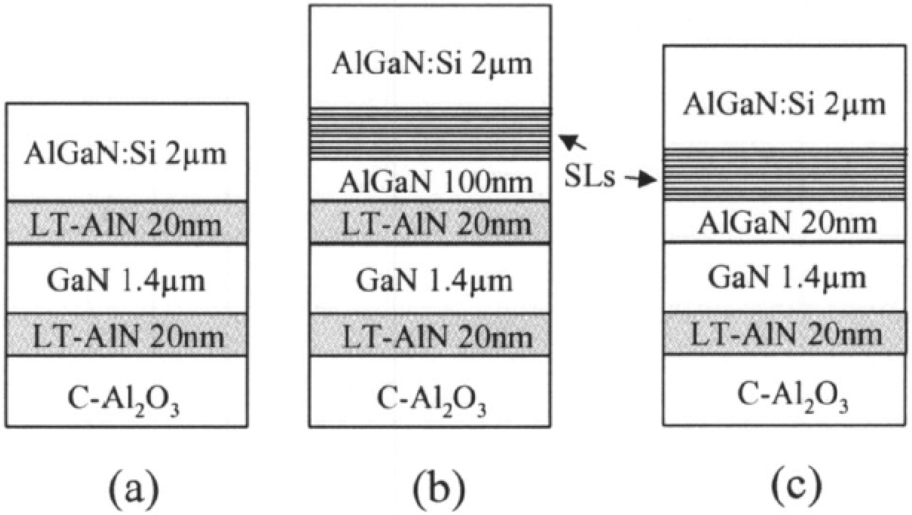
Average tensile stress of 1.3µm thick GaN layer grown on 12nm thick AlN buffer

- Relaxed AlN buffer at low temp growth

Sample	T_{AlN} [°C]	Curvature radius [m]	Total stress [GPa]	a-AlGaN [Å]	a-GaN [Å]
A	630	14.7	−0.01	3.1653	3.1899
B	900	7.9	0.46	3.1665	3.1923
C	1145	2.9	1.13	3.1923	3.1923

Ref.: J. Blasing, et al., Appl. Phys. Lett., pp. 2722–2724, 7 October 2002

AlGaN Grown on GaN with Various Interlayers

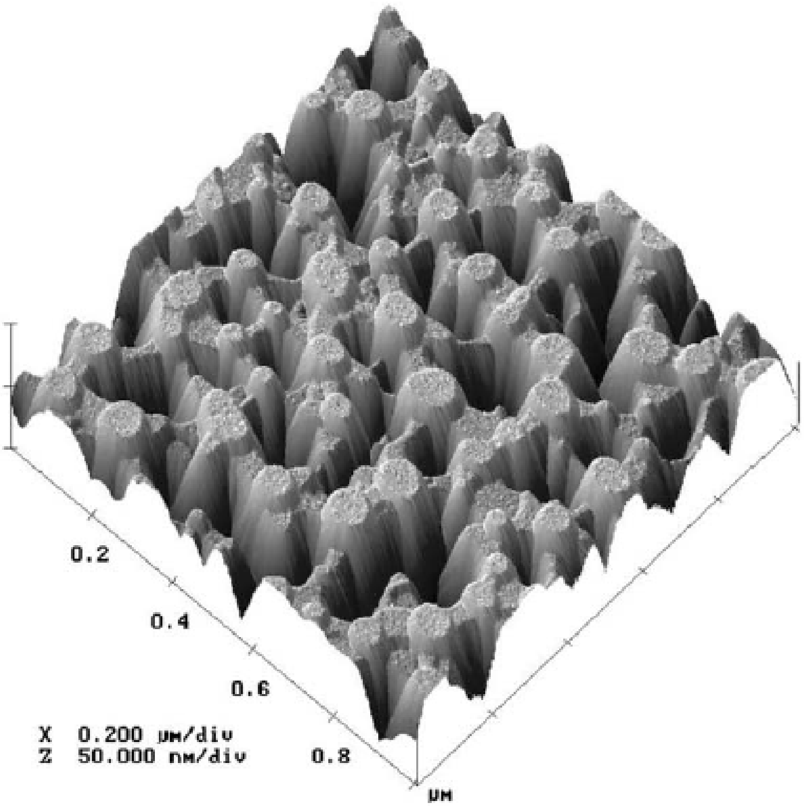


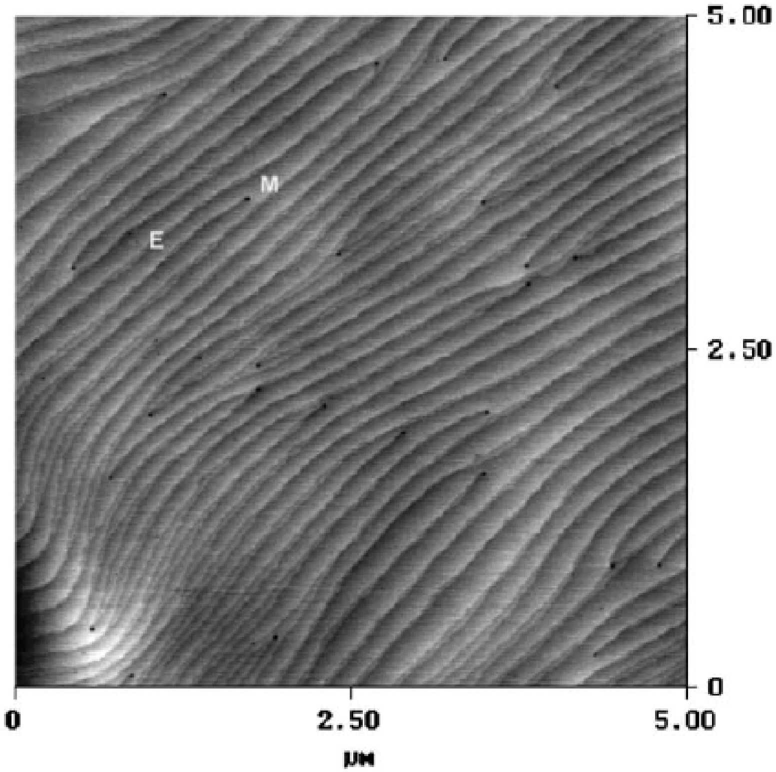
Ten period
AlN 4nm/AlGaN 36nm
Superlattices
($Al_{0.2}GaN$)

Interlayer	Surface	FWHM in (0002) ω scan (arcmin)	FWHM in $(20\bar{2}4)$ ω scan (arcmin)	Density of etch pits (cm^{-2})	Mobility (cm^2/V s) and concentration (cm^{-3})
No	Crack network	9.5	14.6		
LT-AlN	Several cracks	12.4	18.2	6×10^9	
LT-AlN and SLs	Crack free	12.1	16.9	4×10^9	Mob.: 87, Con.: 3.0×10^{18}
SLs	Crack free	6.4	11.8	2×10^9	Mob.: 161, Con.: 2.5×10^{18}
Directly on Sapphire	Crack free	14.6	23.3	7×10^9	Mob.: 38, Con.: 2.2×10^{18}

Ref.: Q. C. Chen, et al., Appl. Phys. Lett., pp. 4961–4963, 23 December 2002

Reduced Dislocation Densities with SiH_4 Treatment

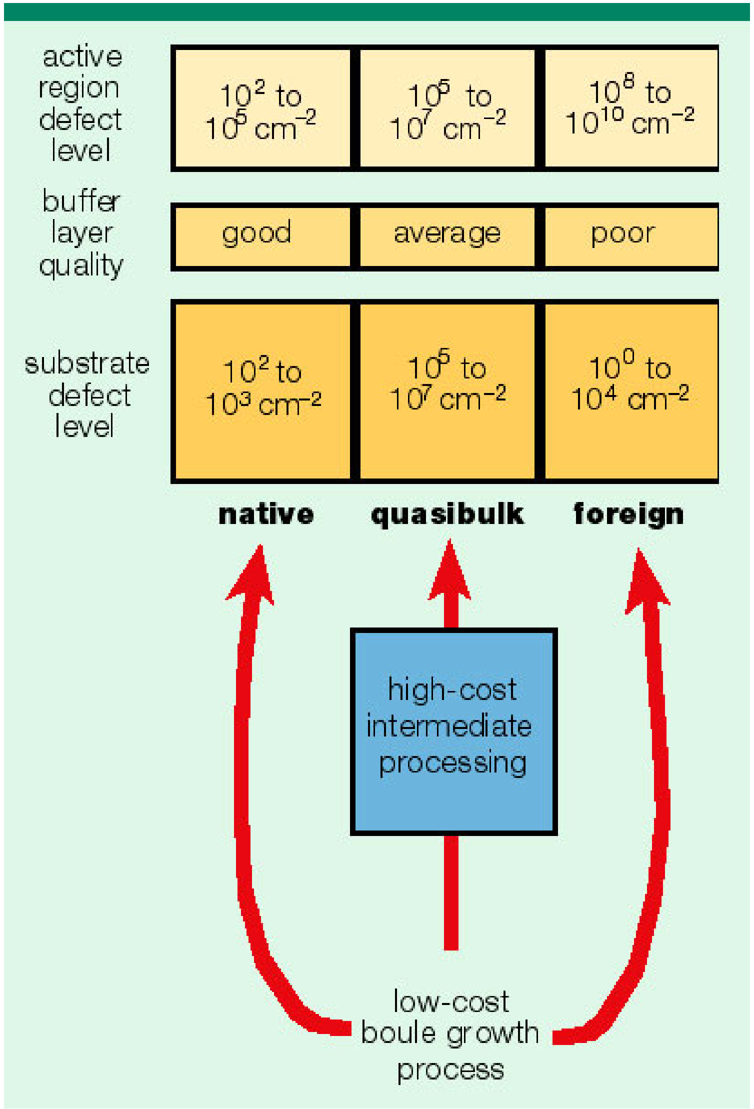




Etched surface with SiH_4 treatment at 1100°C for 300s

TD densities ~ $1x10^8$ cm^{-2} (without SiH_4 treatment, ~ $1x10^9$ cm^{-2})

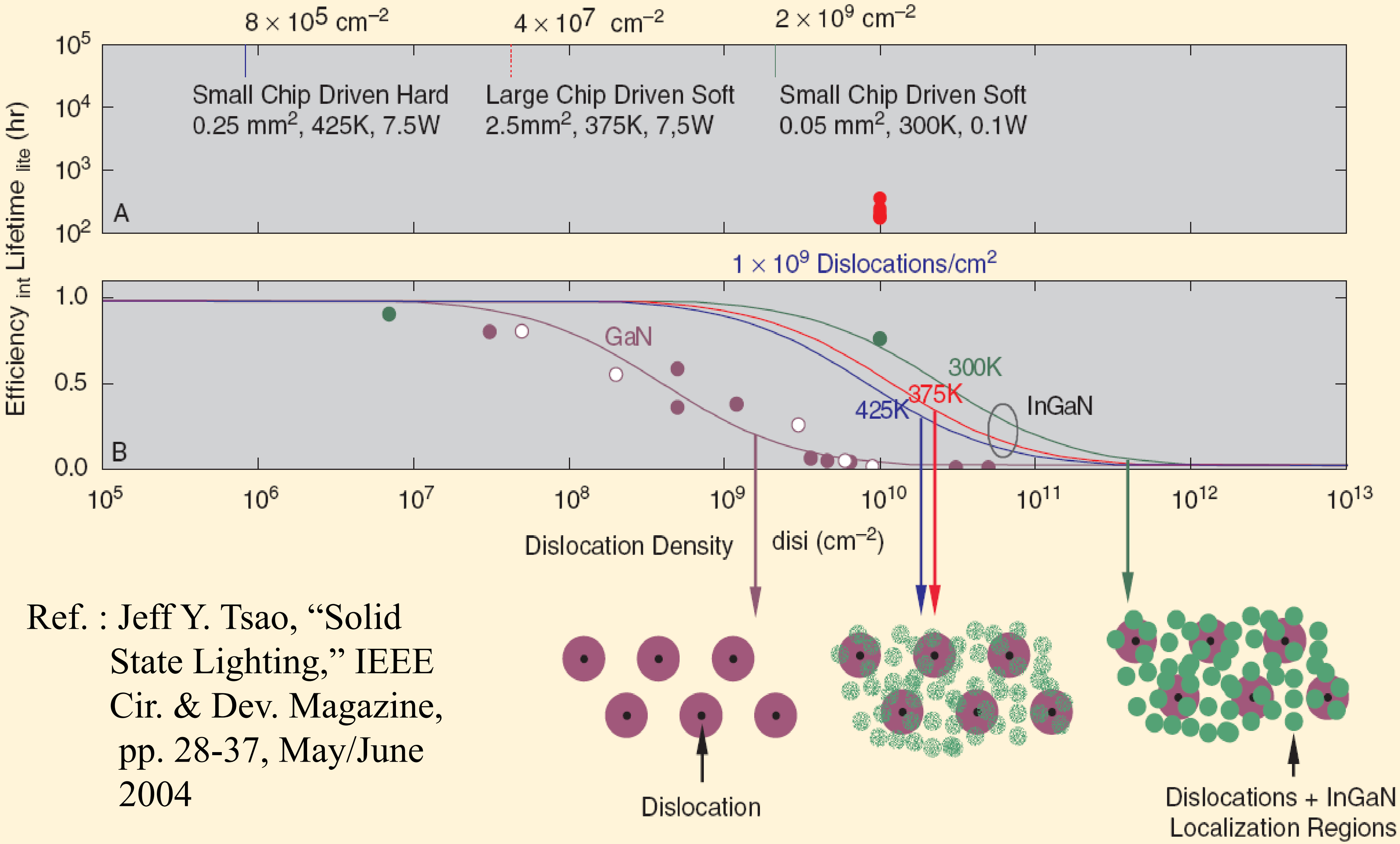
Ref.: K. Pakula, et al., Journal of Crystal Growth 267, pp. 1–7, 2004



- Bulk GaN growth with pressures of 15,000 atm and temperatures of 1600ºC ➡10 mm in diameter with TD densities of 100 cm^{-2} (commercialized by Topgan for research)
- 1~2 inch bulk AlN growth with sublimation recondensation process ➡ appropriate for Al-rich AlGaN growth for DUV laser diodes (commercialized by Crystal IS)

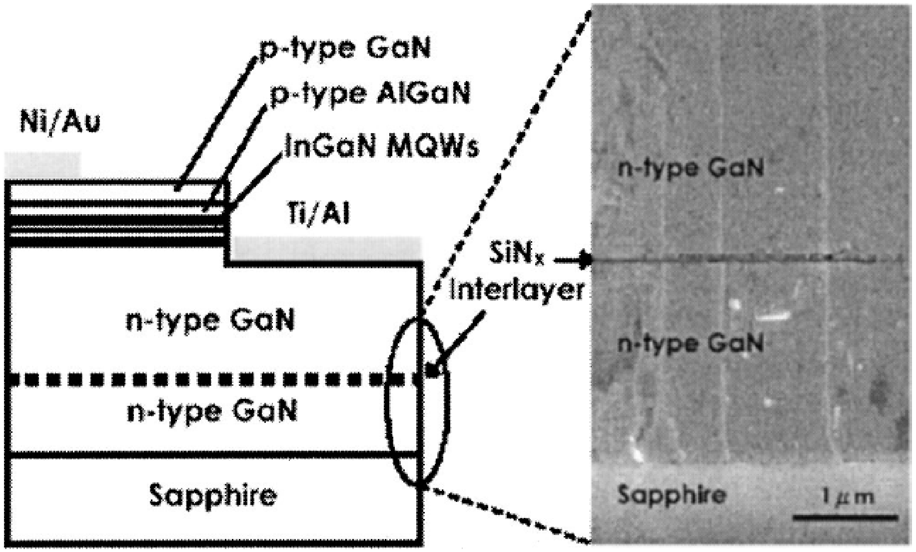
Ref. : Compound Semiconductor Magazine, Juy, Oct. 2004

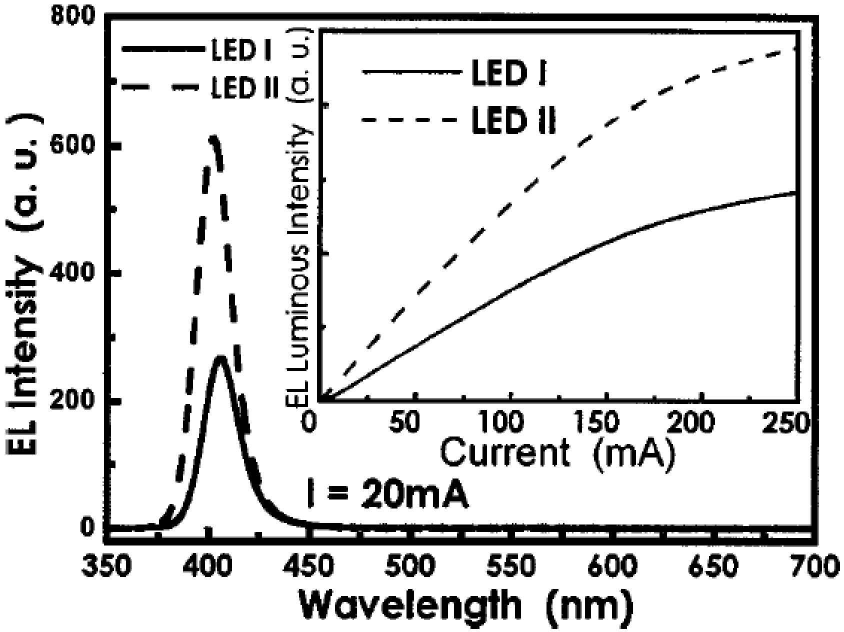
Effects of Dislocations on Light Emission Efficiency



Ref. : Jeff Y. Tsao, "Solid State Lighting," IEEE Cir. & Dev. Magazine, pp. 28-37, May/June 2004

Effects of Dislocations on LED Performance



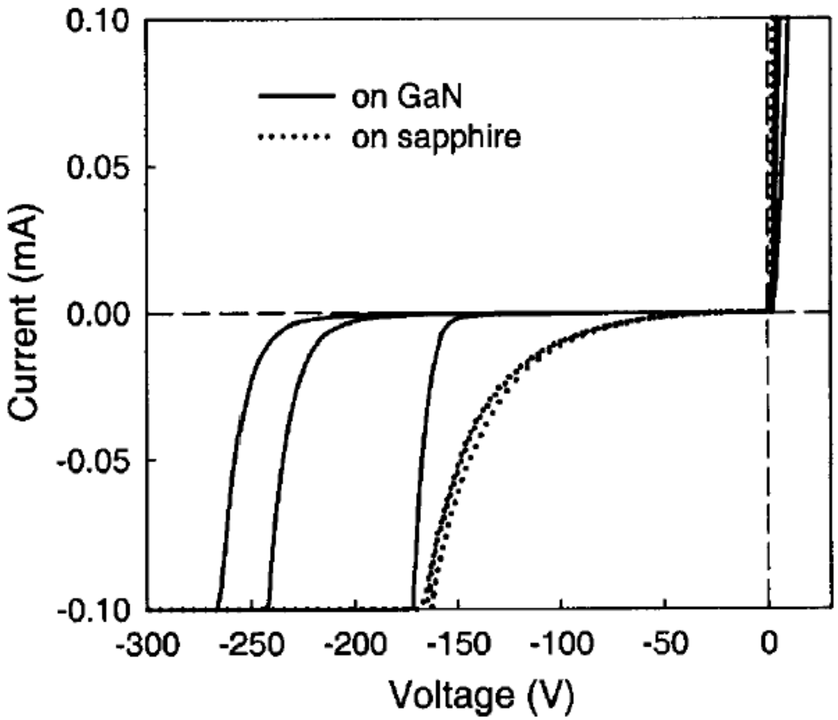


Ref. : Ru-Chin Tu, et al., Appl. Phys. Lett. pp. 3608-3610, 27 October 2003

Effects of Dislocations on Reverse Leakage Current

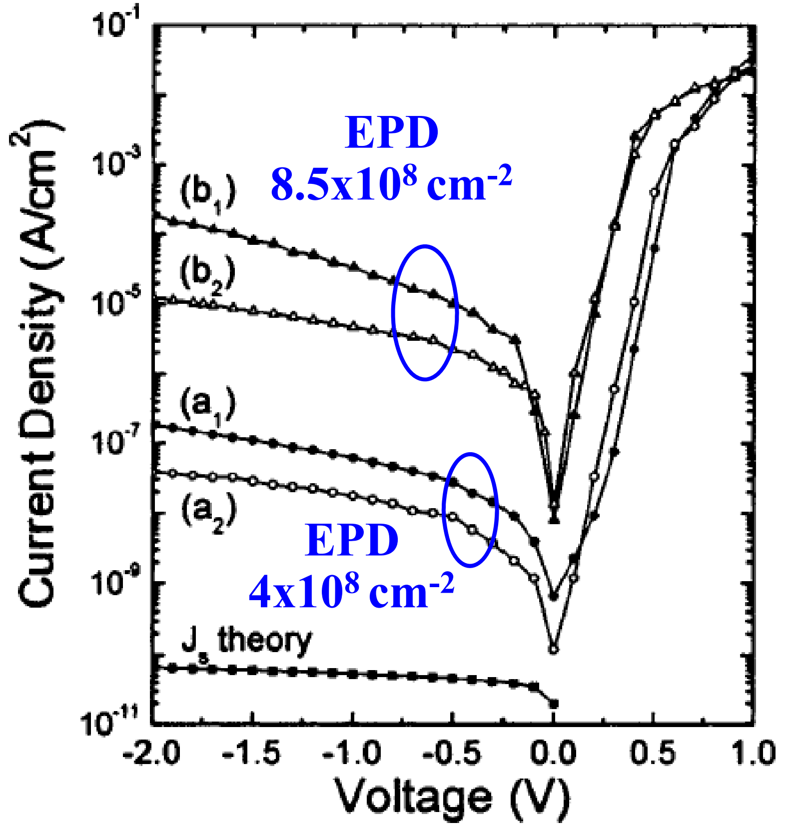
GaN PIN Rectifier

(4μm $1x10^{17}cm^{-3}$ N^- Region)



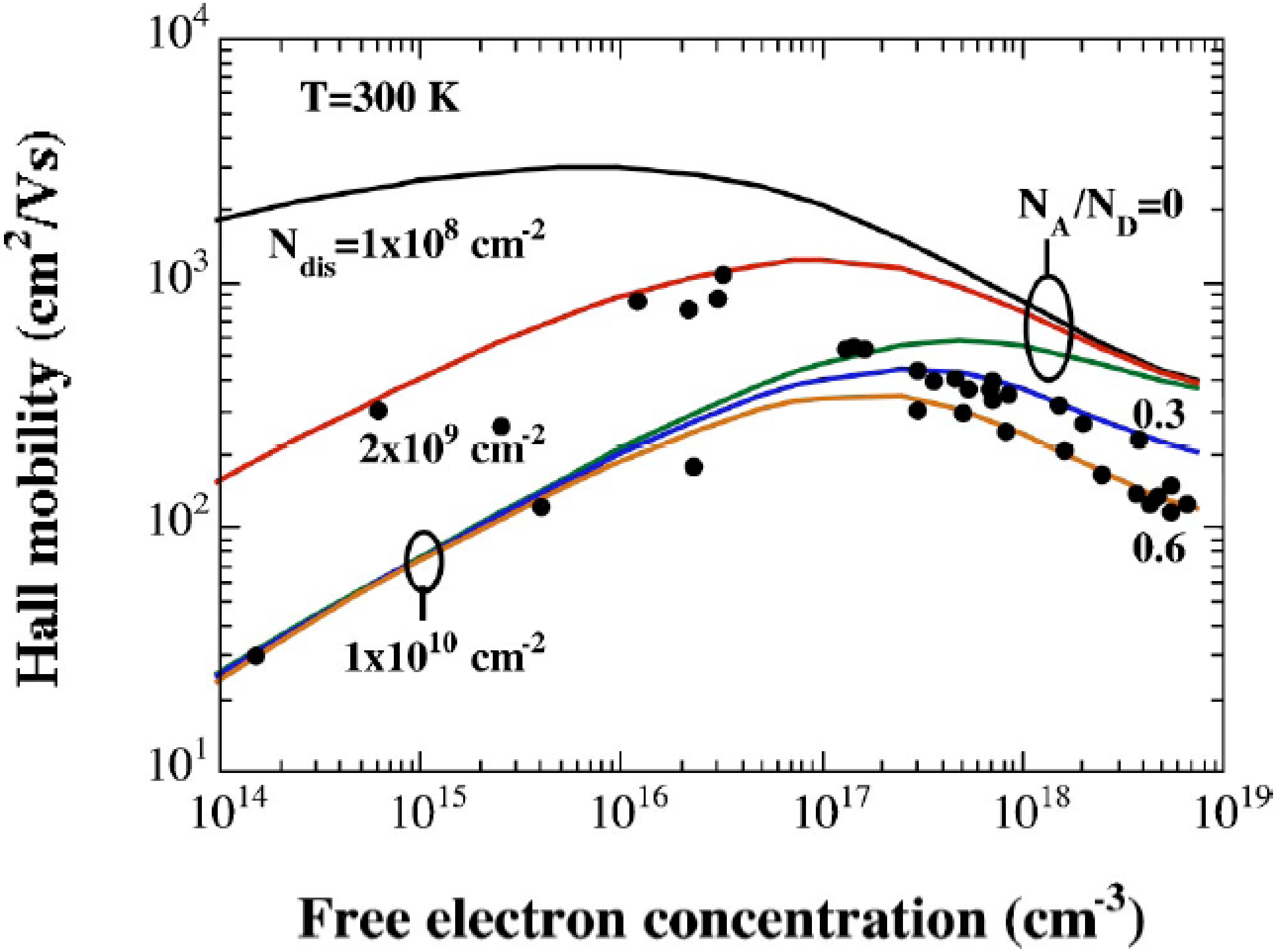
Ref. : X. A. Cao, et al., Appl. Phys. Lett. **87**, 053503, 2005

Au/n-GaN Schottky diodes



Ref. : Y. Huang, et al., J. Appl. Phys., pp. 5771-5775, 1 Nov. 2003

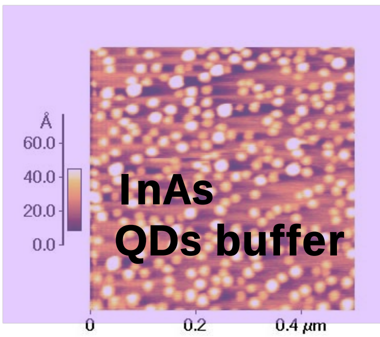
Effects of Dislocations on Hall Mobility

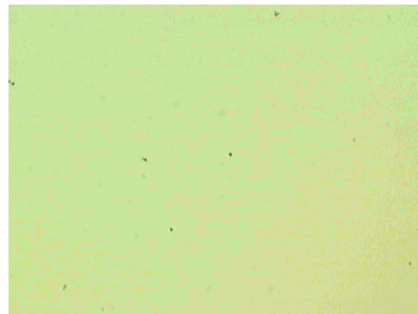


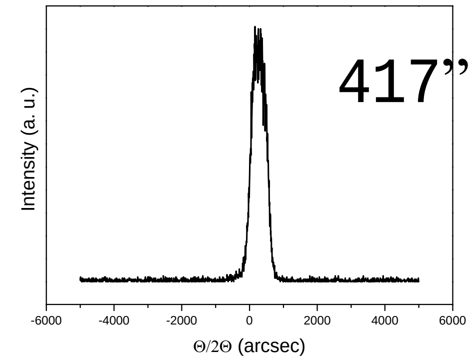
Ref. : M. N. Gurusinghe, et al., Physical Review B **67**, 235208, 2003

Hetero-Epitaxy with the Defect-Free QD Buffer layer

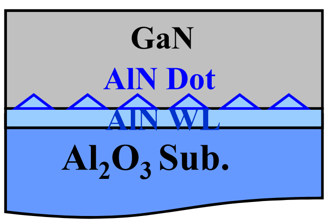
GaSb epilayer on GaAs sub.

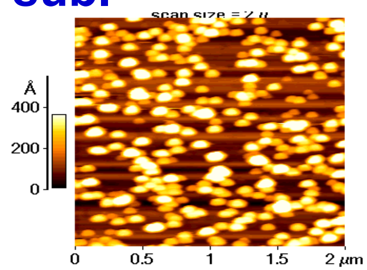


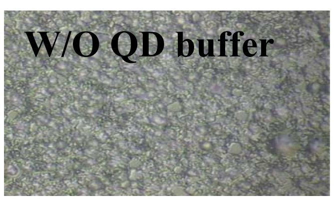


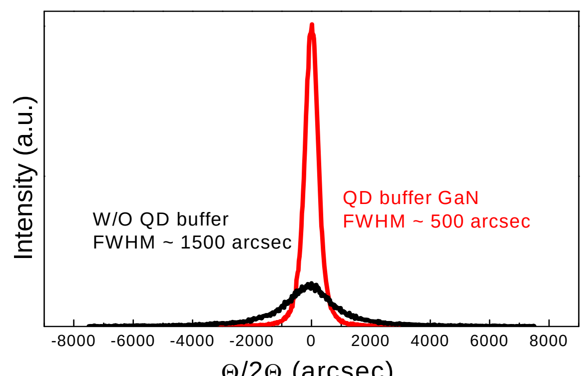


GaN epilayer on Sapphire sub.

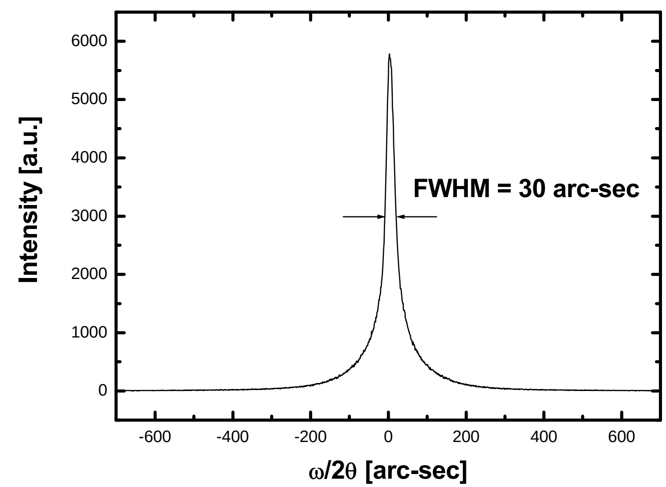








The recent GaN epilayer quality after further optimization

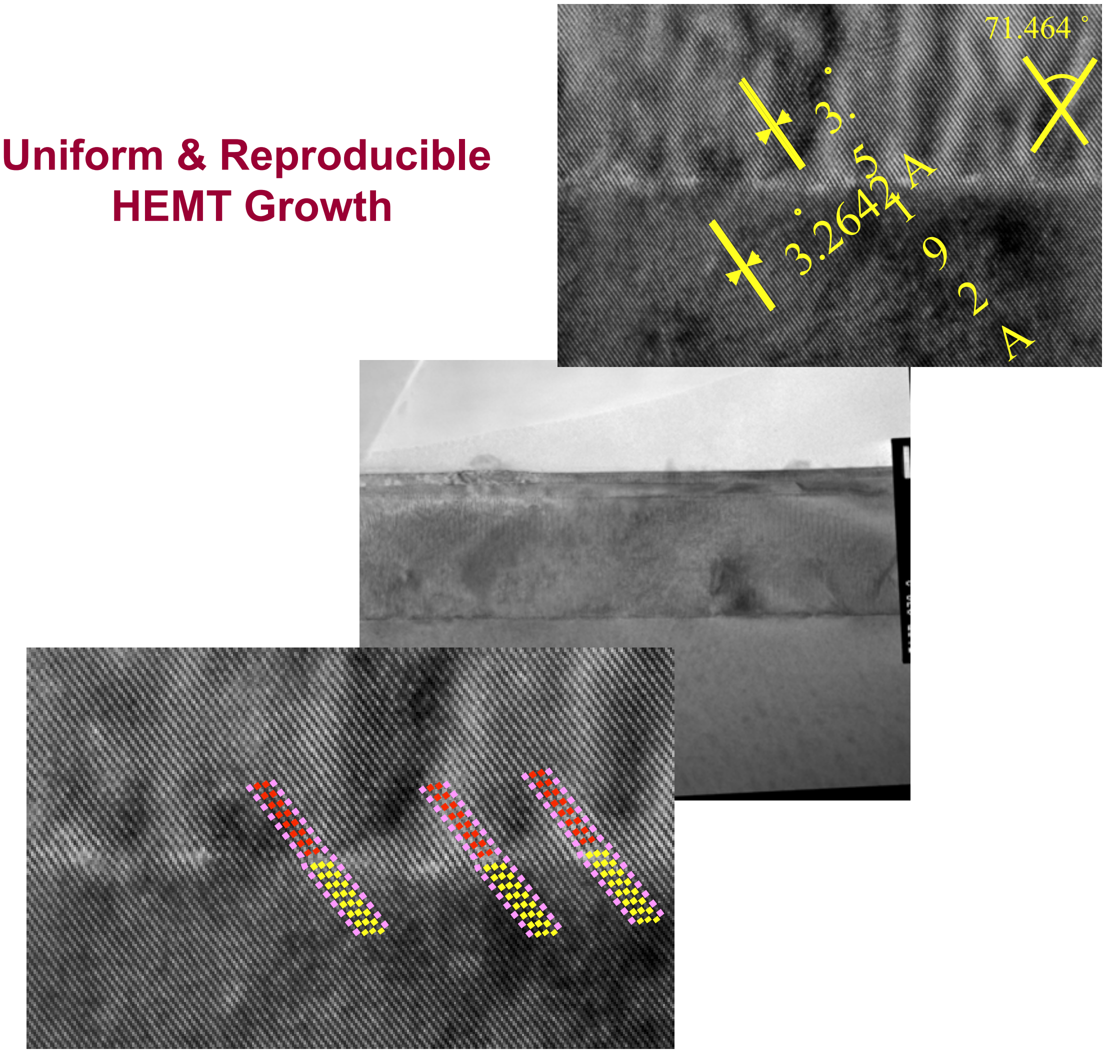


Thin barrier InAs HEMT grown using InAs QD/GaSb Buffer

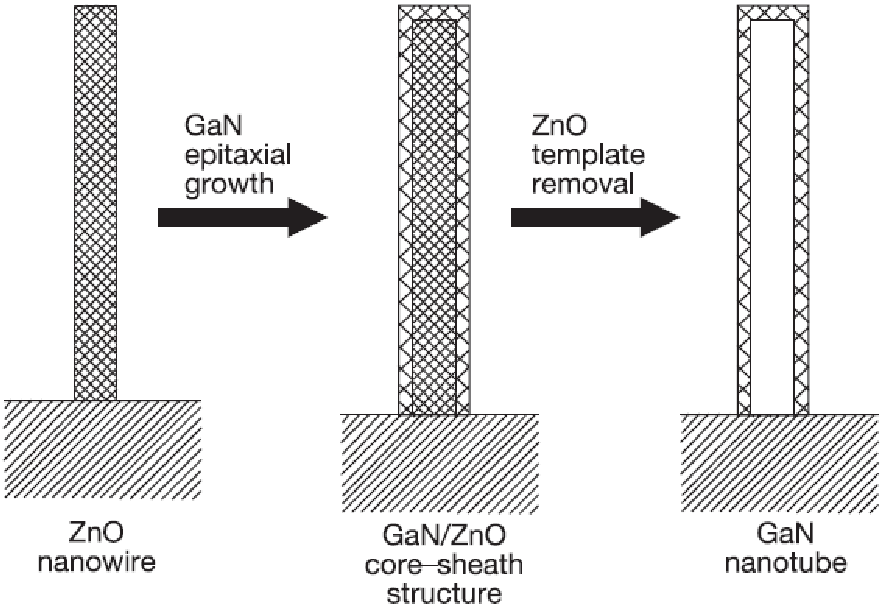
Layer	Thickness
InAs	50Å
$Al_{0.2}GaSb$	100Å
Δ-doping (5e17)	
$Al_{0.2}GaSb$	100Å
InAs	100Å
GaSb	0.5um
InAs QD	
GaAs	0.5um
SI-GaAs	

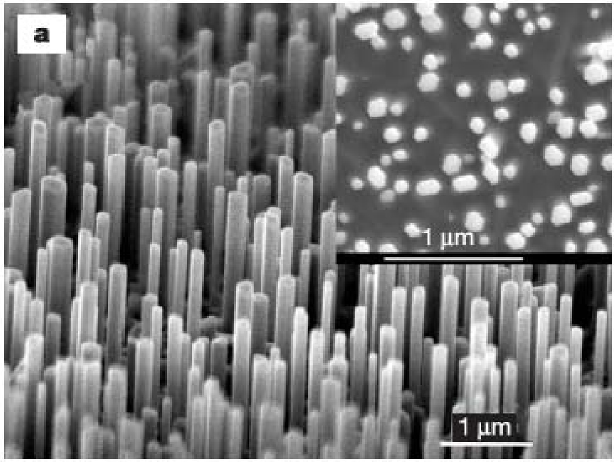
$n_s = 3.33 \times 10^{12}\ cm^{-2}$
$\mu = 8064\ cm^2/V\text{-}s$

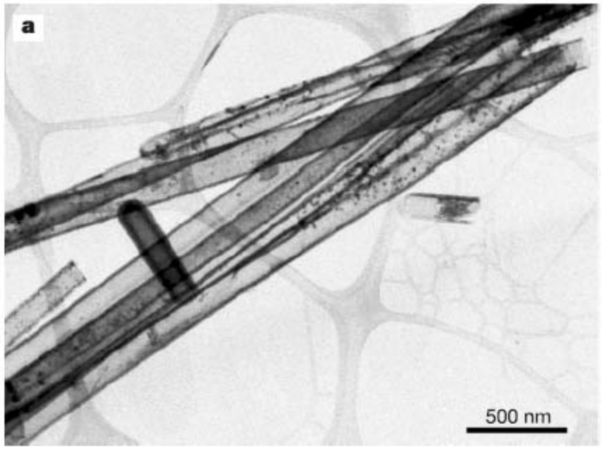
Uniform & Reproducible HEMT Growth



GaN Nanotube

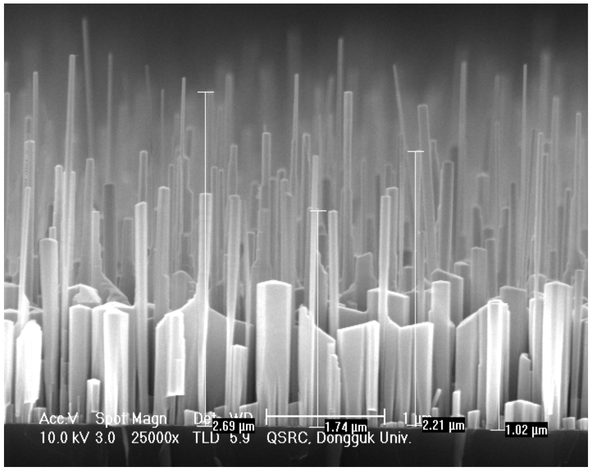


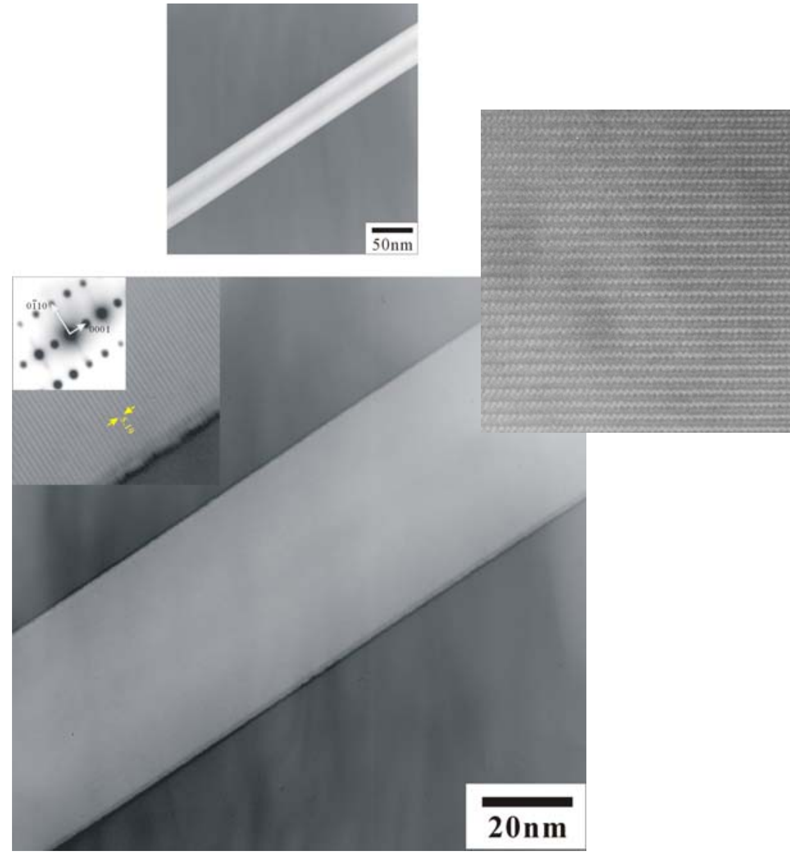




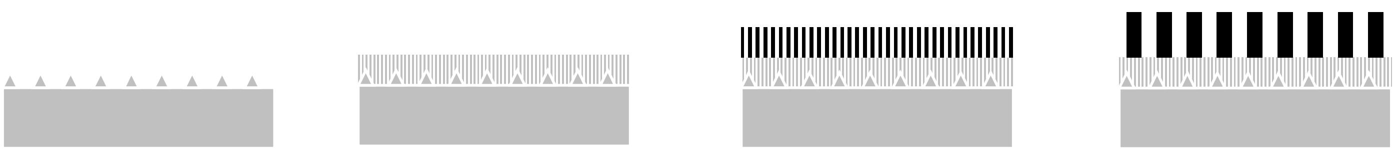
Ref: J. Goldberger, et al., NATURE, pp. 599-602, APRIL 2003

Nano-rod Formation on Si substrate with no Catalysis



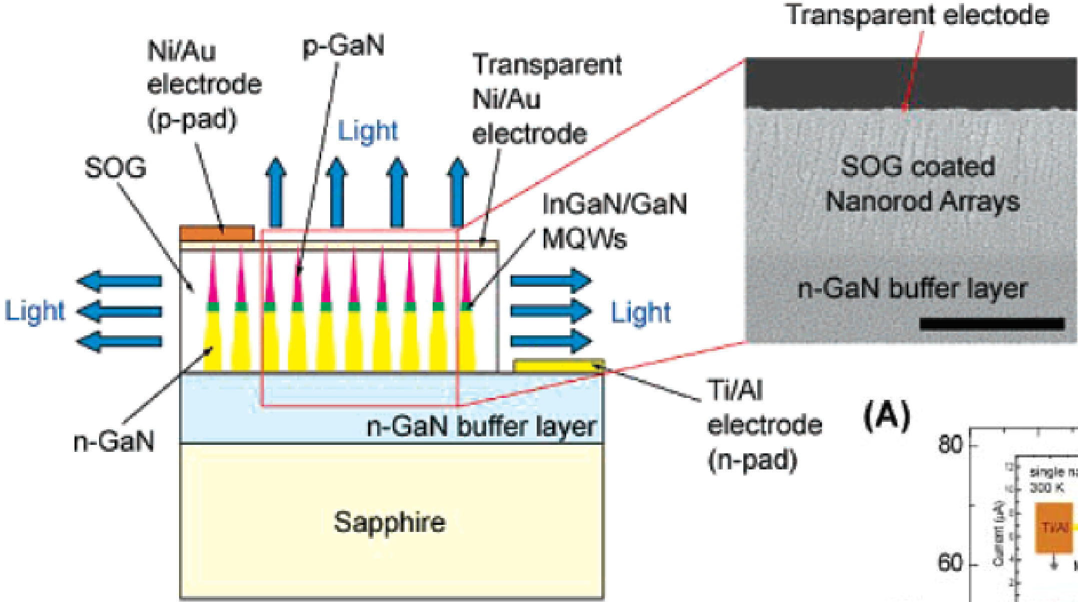


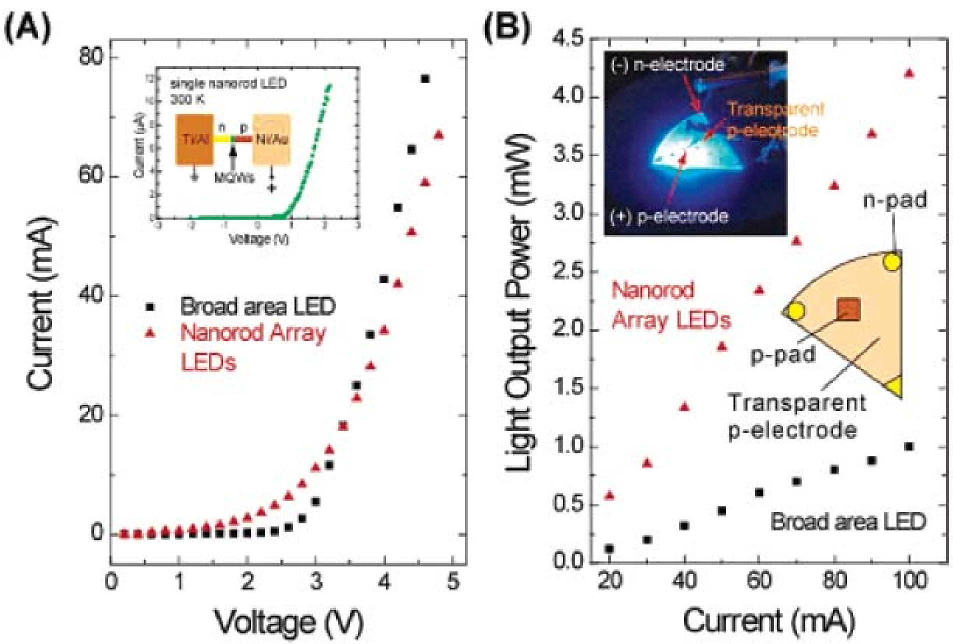
- Defect free material/structures are obtained
- Partially relaxed structure
- Diameter ranging from 5 nm~350 nm can be controlled : f_{Ga}/f_N
- Feasible for vertical device structures



(I)QD Nucleation (II)Columnar Growth (III)Selective Nanorod Growth (IV) Lateral Nanorod Growth

High Brightness InGaN/GaN MQW Nanorod LED





Ref: Hwa-Mok Kim, et al., NANO LETTERS, pp. 1059-1062, 2004