
Ch 1. Introduction

Introduction

- Computer hardware has experienced the most dramatic improvement in capabilities and costs ever experienced by humankind.
- Logic design is one of the disciplines that has enabled the digital revolution which has dramatically altered our lives.

Design

- What is design?
 - the process of coming up with a solution to a problem
 - while meeting some criteria for size, cost, power, beauty, elegance, etc.
- The divide-and-conquer approach
 - Has been developed to handle the complexity of the process
 - We breakdown the problem into smaller pieces, deal with constraints beyond their control, put all the pieces together to solve the bigger problem.

Logic Design

- The logic designer's job
 - To choose the right components to solve a logic design problem while meeting constraints (e.g., size, cost, performance, and power consumption)
- Digital components
 - have input and output wires which carry digital logic values (i.e., 0 and 1).
 - Arbitrary information can be represented using this digital abstraction.
 - Transistors react to the voltage levels on the input wires.
 - Sequential logic circuits' outputs react to the current values on the input wires and to the past history of values on those same input wires.

Contemporary Logic Design

- Important trends in contemporary Logic Design
 - larger and larger designs
 - shorter and shorter time to market
 - cheaper and cheaper products
- Scale
 - pervasive use of computer-aided design tools over hand methods
 - multiple levels of design representation
- Time
 - emphasis on abstract design representations
 - programmable rather than fixed function components
 - automatic synthesis techniques
 - importance of sound design methodologies
- Cost
 - higher levels of integration
 - use of simulation to debug designs
 - simulate and verify before you build

A Brief History of Logic Design

- 1850: George Boole invents Boolean algebra
 - maps logical propositions to symbols
 - permits manipulation of logic statements using mathematics
- 1938: Claude Shannon links Boolean algebra to switches
 - his Masters' thesis
- 1946: ENIAC . . . The world's first completely electronic computer
 - 18,000 vacuum tubes
 - several hundred multiplications per minute
- 1947: Shockley, Brittain, and Bardeen invent the transistor
 - replaces vacuum tubes
 - enable integration of multiple devices into one package
 - gateway to modern electronics

A Brief History of Logic Design (cont'd)

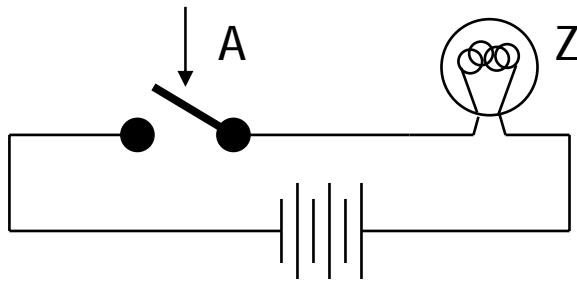
- 1960s: A large catalog of logic components
 - Texas Instruments TTL data book
 - Arbitrary logic circuits could be built from these basic primitives.
- 1975: The introduction of Programmable Array Logic (PAL)
 - collections of switches in regular arrangements
 - increase levels of integration
 - make it easier for designers to change the wiring pattern
- 1984: Field-programmable gate arrays introduced by Xilinx
 - Logic circuits can be altered over times.
 - Synthesis tools have followed with the appropriate compilation.

Computation: abstract vs. implementation

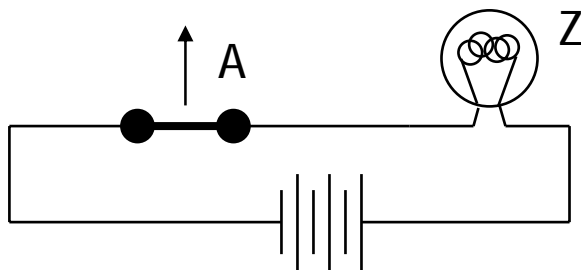
- Up to now, computation has been a mental exercise (paper, programs)
- This class is about physically implementing computation using physical devices that use voltages to represent logical values
- Basic units of computation are:
 - representation: "0", "1" on a wire
set of wires (e.g., for binary ints)
 - assignment: $x = y$
 - data operations: $x + y - 5$
 - control:
 - sequential statements: $A; B; C$
 - conditionals: $\text{if } x == 1 \text{ then } y$
 - loops: $\text{for } (i = 1 ; i == 10, i++)$
 - procedures: $A; \text{proc}(\dots); B;$
- We will study how each of these are implemented in hardware and composed into computational structures

Switches: basic building block of digital computers

- Implementing a simple circuit (arrow shows action if wire changes to “1”):



close switch (if A is “1” or asserted)
and turn on light bulb (Z)

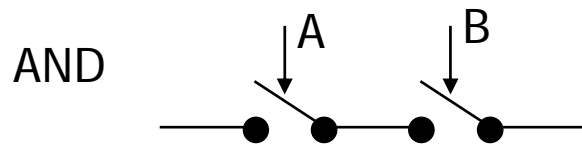


open switch (if A is “0” or unasserted)
and turn off light bulb (Z)

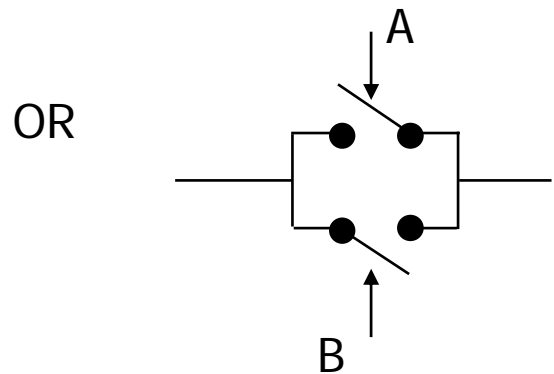
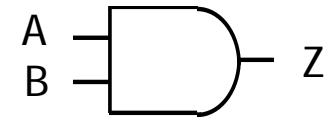
$$Z = A$$

Switches (cont'd)

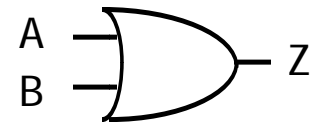
- Compose switches into more complex ones (Boolean functions):



$$Z = A \text{ and } B$$



$$Z = A \text{ or } B$$

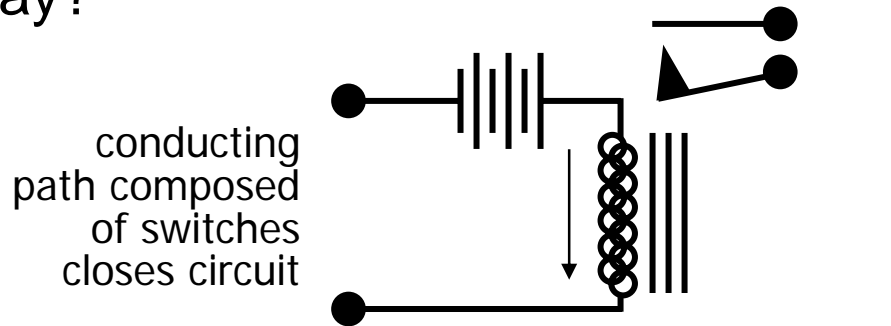


Switching networks

- Switch settings
 - determine whether or not a conducting path exists to light the light bulb
- To build larger computations
 - use a light bulb (output of the network) to set other switches (inputs to another network).
- Connect together switching networks
 - to construct larger switching networks, i.e., there is a way to connect outputs of one network to the inputs of the next.

Relay networks

- A simple way to convert between conducting paths and switch settings is to use (electro-mechanical) relays.
- What is a relay?



current flowing through coil magnetizes core and causes normally closed (nc) contact to be pulled open

when no current flows, the spring of the contact returns it to its normal position

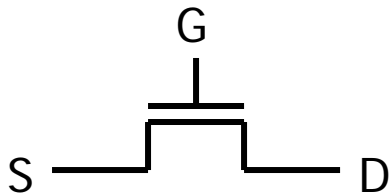
What determines the switching speed of a relay network?

Transistor networks

- Relays aren't used much anymore
 - Relay circuits were large and slow
- Modern digital systems are designed in CMOS technology
 - MOS stands for Metal-Oxide on Semiconductor
 - C is for complementary because there are both normally-open and normally-closed switches
- MOS transistors act as voltage-controlled switches
 - similar, though easier to work with than relays.

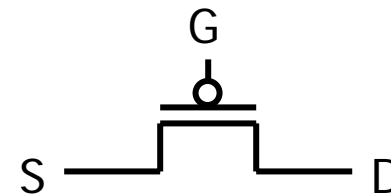
MOS transistors

- MOS transistors have three terminals: drain, gate, and source
 - they act as switches in the following way:
if the voltage on the gate terminal is (some amount) higher/lower than the source terminal then a conducting path will be established between the drain and source terminals



n-type

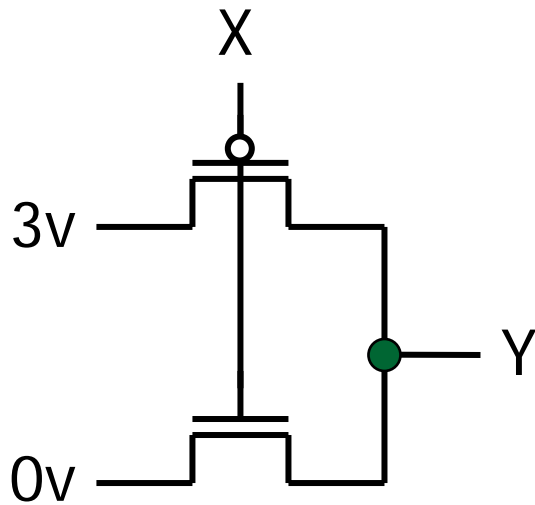
open when voltage at G is low
closed when voltage at G is high



p-type

closed when voltage at G is low
open when voltage at G is high

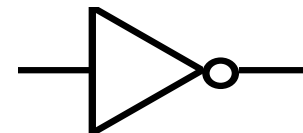
CMOS network



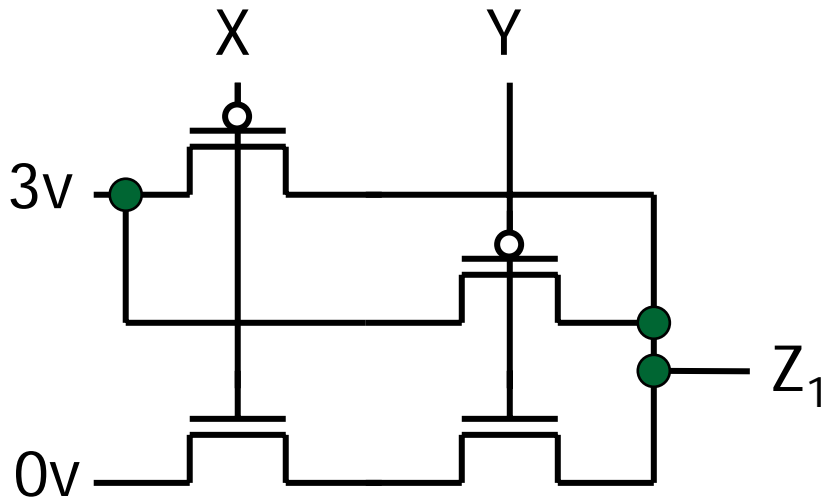
what is the
relationship
between X and Y ?

X	Y
0 volts	
3 volts	

NOT

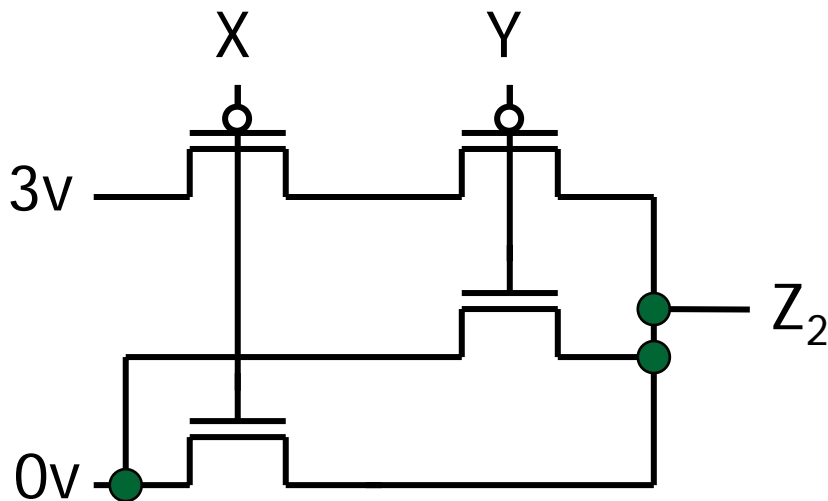


Two CMOS transistors networks



what is the relationship between X, Y and Z?

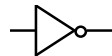
X	Y	Z1	Z2
0 volts	0 volts		
0 volts	3 volts		
3 volts	0 volts		
3 volts	3 volts		



Combinational logic symbols

- Common combinational logic systems have standard symbols called logic gates

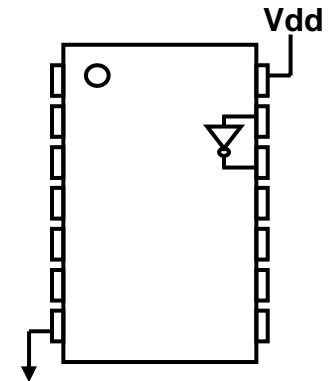
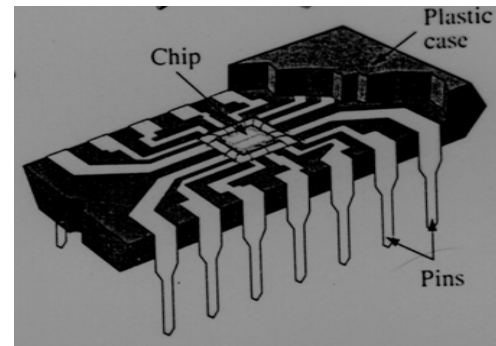
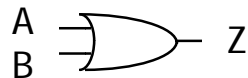
- Buffer, NOT



- AND, NAND



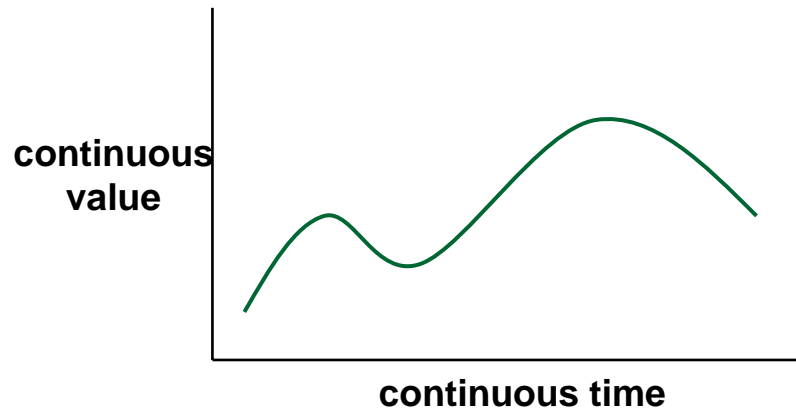
- OR, NOR



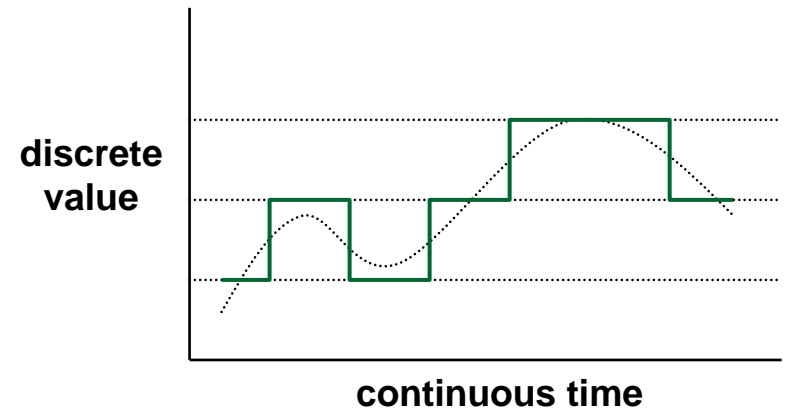
easy to implement
with CMOS transistors
(the switches we have
and use most)

Digital vs. analog

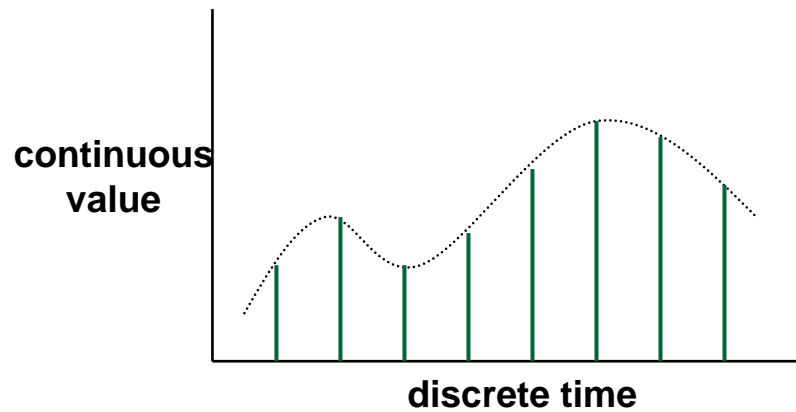
analog



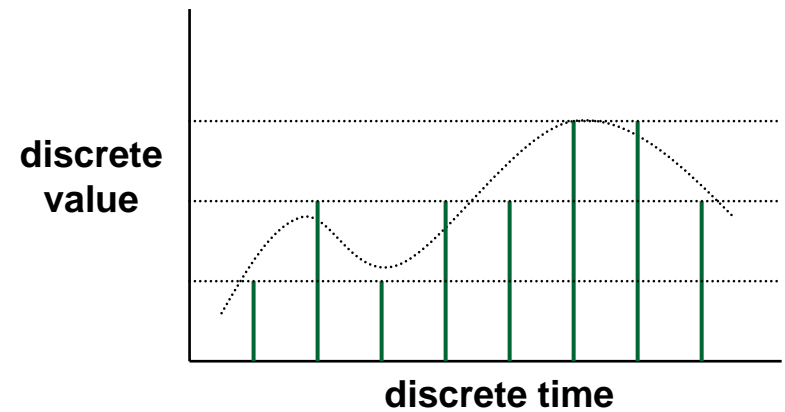
quantized



sampled



digital



Why digital/binary?

- Why digital?
 - Human processes in digital
 - e.g. analog vs. digital watch
 - Robust : immune to noise by reshaping
 - e.g. LP vs. CD
- How many quantization levels?
 - Binary (represented by bits, i.e. 0's and 1's) is the most popular
- Why binary?
 - Can use simple switches (on and off)
 - Regarded as decision making (true and false) --> simple logical model
 - Reliability (big noise margin)

An example : Calendar

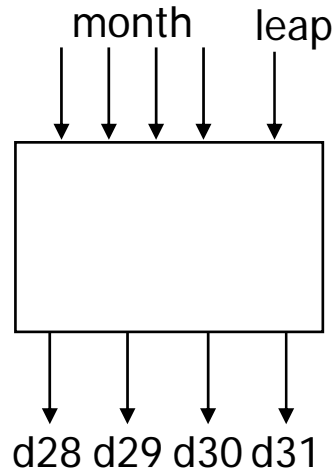
- Calendar subsystem: number of days in a month (to control watch display)
 - used in controlling the display of a wrist-watch LCD screen
 - inputs: month, leap year flag
 - outputs: number of days

Implementation in software

```
integer number_of_days (month, leap_year_flag)
{
    switch (month) {
        case `january': return (31);
        case `february': if (leap_year_flag == 1) then
            return (29) else return (28);
        case `march': return (31);
        ...
        case `december': return (31);
        default: return (0);
    }
}
```

Implementation as a combinational digital system

- Encoding:
 - how many bits for each input/output?
 - binary number for month
 - four wires for 28, 29, 30, and 31
- Behavior:
 - combinational
 - truth table specification



month	leap	d28	d29	d30	d31
0000	-	-	-	-	-
0001	-	0	0	0	1
0010	0	1	0	0	0
0010	1	0	1	0	0
0011	-	0	0	0	1
0100	-	0	0	1	0
0101	-	0	0	0	1
0110	-	0	0	1	0
0111	-	0	0	0	1
1000	-	0	0	0	1
1001	-	0	0	1	0
1010	-	0	0	0	1
1011	-	0	0	1	0
1100	-	0	0	0	1
1101	-	-	-	-	-
111-	-	-	-	-	-

Combinational example (cont'd)

- Truth-table to logic to switches to gates

- $d_{28} = 1$ when month=0010 and leap=0

- $d_{28} = m_8' \cdot m_4' \cdot m_2 \cdot m_1' \cdot \text{leap}'$

- $d_{31} = 1$ when month=0001 or month=0011 or ... month=1100

- $d_{31} = (m_8' \cdot m_4' \cdot m_2' \cdot m_1) + (m_8' \cdot m_4' \cdot m_2 \cdot m_1) + \dots$
 $(m_8 \cdot m_4 \cdot m_2' \cdot m_1')$

- $d_{31} =$ can we simplify more?

symbol
for and

symbol
for or

symbol
for not

month	leap	d28	d29	d30	d31
0001	-	0	0	0	1
0010	0	1	0	0	0
0010	1	0	1	0	0
0011	-	0	0	0	1
0100	-	0	0	1	0
...					
1100	-	0	0	0	1
1101	-	-	-	-	-
111-	-	-	-	-	-
0000	-	-	-	-	-

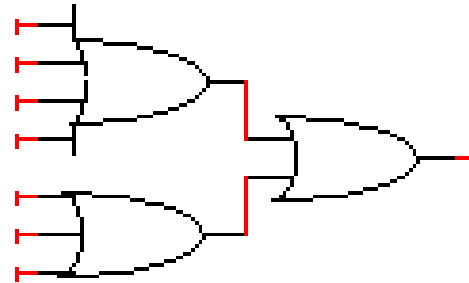
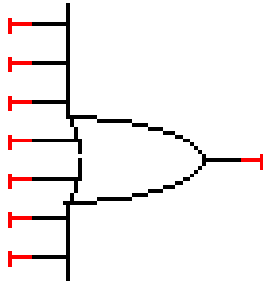
Combinational example (cont'd)

- $d_{28} = m_{8'} \cdot m_{4'} \cdot m_2 \cdot m_{1'} \cdot \text{leap}'$
- $d_{29} = m_{8'} \cdot m_{4'} \cdot m_2 \cdot m_{1'} \cdot \text{leap}$
- $d_{30} = (m_{8'} \cdot m_{4'} \cdot m_2' \cdot m_{1'}) + (m_{8'} \cdot m_{4'} \cdot m_2 \cdot m_{1'}) + (m_{8'} \cdot m_{4'} \cdot m_2' \cdot m_1) + (m_{8'} \cdot m_{4'} \cdot m_2 \cdot m_1)$
 $= (m_{8'} \cdot m_{4'} \cdot m_{1'}) + (m_{8'} \cdot m_{4'} \cdot m_1)$
- $d_{31} = (m_{8'} \cdot m_{4'} \cdot m_2' \cdot m_1) + (m_{8'} \cdot m_{4'} \cdot m_2 \cdot m_1) + (m_{8'} \cdot m_{4'} \cdot m_2' \cdot m_{1'}) + (m_{8'} \cdot m_{4'} \cdot m_2 \cdot m_{1'}) + (m_{8'} \cdot m_{4'} \cdot m_2' \cdot m_1) + (m_{8'} \cdot m_{4'} \cdot m_2 \cdot m_{1'})$



Combinational example (cont'd)

- $d_{31} = (m_8' \cdot m_4' \cdot m_2' \cdot m_1) + (m_8' \cdot m_4' \cdot m_2 \cdot m_1) + (m_8' \cdot m_4 \cdot m_2' \cdot m_1) + (m_8' \cdot m_4 \cdot m_2 \cdot m_1) + (m_8 \cdot m_4' \cdot m_2' \cdot m_4') + (m_8 \cdot m_4' \cdot m_2 \cdot m_1') + (m_8 \cdot m_4 \cdot m_2' \cdot m_1')$



- Alternate realizations for a 7-input OR function

Another example : Combination Lock

- Door combination lock:
 - punch in 3 values in sequence and the door opens; if there is an error the lock must be reset; once the door opens the lock must be reset
 - inputs: sequence of input values, reset
 - outputs: door open/close
 - memory: must remember combination
or always have it available as an input

Implementation in software

```
integer combination_lock ( ) {
    integer v1, v2, v3;
    integer error = 0;
    static integer c[3] = 3, 4, 2;

    while (!new_value( ));
    v1 = read_value( );
    if (v1 != c[1]) then error = 1;

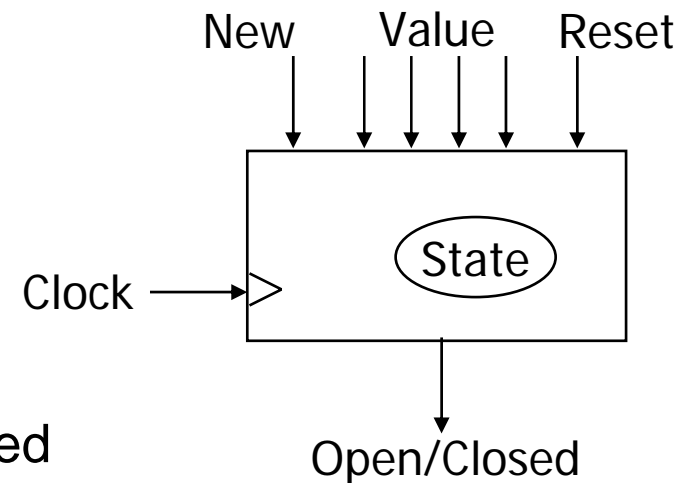
    while (!new_value( ));
    v2 = read_value( );
    if (v2 != c[2]) then error = 1;

    while (!new_value( ));
    v3 = read_value( );
    if (v2 != c[3]) then error = 1;

    if (error == 1) then return(0); else return (1);
}
```

Implementation as a sequential digital system

- Encoding:
 - how many bits per input value?
 - how many values in sequence?
 - how do we know a new input value is entered?
 - how do we represent the states of the system?
- Behavior:
 - clock wire tells us when it's ok to look at inputs (i.e., they have settled after change)
 - sequential: sequence of values must be entered
 - sequential: remember if an error occurred
 - finite-state specification



Sequential example (cont'd): abstract control

- Finite-state diagram

- states: 5 states

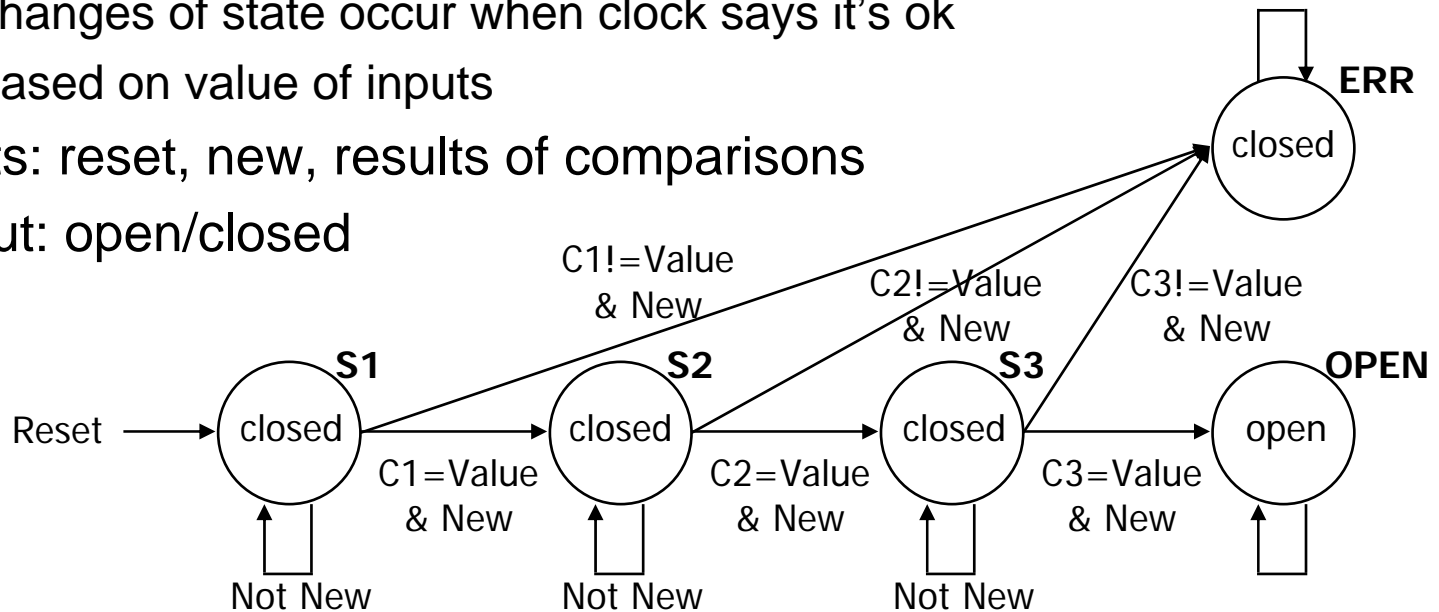
- represent point in execution of machine
- each state has outputs

- transitions: 6 from state to state, 5 self transitions, 1 global

- changes of state occur when clock says it's ok
- based on value of inputs

- inputs: reset, new, results of comparisons

- output: open/closed



Sequential example (cont'd): data-path vs. control

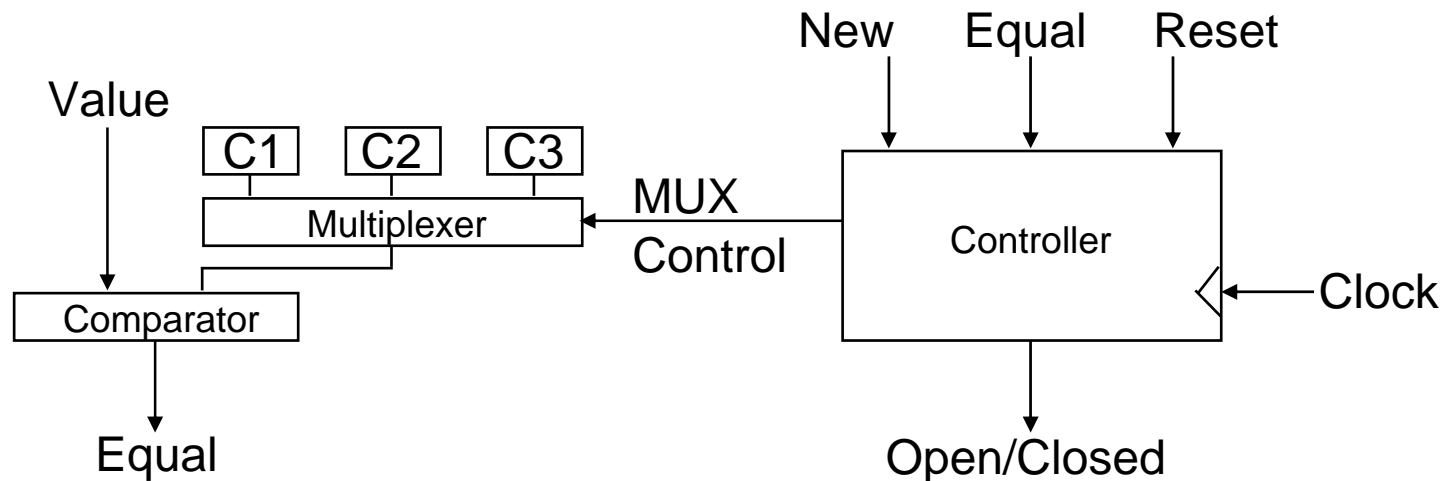
- Internal structure

- data-path

- storage for combination
- comparators

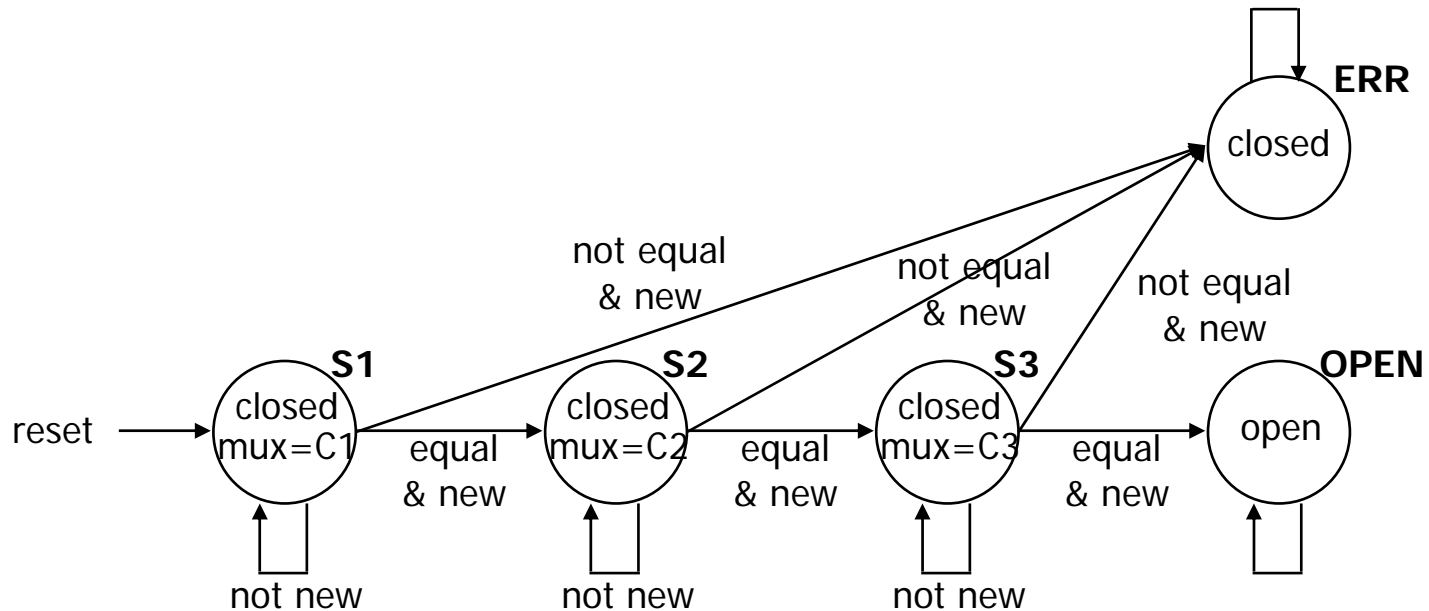
- control

- finite-state machine controller
- control for data-path
- state changes controlled by clock



Sequential example (cont'd): finite-state machine

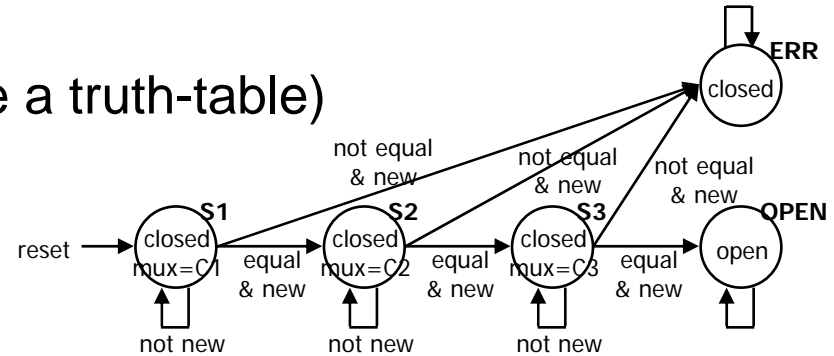
- Finite-state machine
 - refine state diagram to include internal structure



Sequential example (cont'd): finite-state machine

- Finite-state machine

- generate state table (much like a truth-table)



reset	new	equal	state	next state	mux	open/closed
1	-	-	-	S1	C1	closed
0	0	-	S1	S1	C1	closed
0	1	0	S1	ERR	-	closed
0	1	1	S1	S2	C2	closed
0	0	-	S2	S2	C2	closed
0	1	0	S2	ERR	-	closed
0	1	1	S2	S3	C3	closed
0	0	-	S3	S3	C3	closed
0	1	0	S3	ERR	-	closed
0	1	1	S3	OPEN	-	open
0	-	-	OPEN	OPEN	-	open
0	-	-	ERR	ERR	-	closed

Sequential example (cont'd): encoding

■ Encode state table

- state can be: S1, S2, S3, OPEN, or ERR
 - needs at least 3 bits to encode: 000, 001, 010, 011, 100
 - and as many as 5: 00001, 00010, 00100, 01000, 10000
 - choose 4 bits: 0001, 0010, 0100, 1000, 0000
- output mux can be: C1, C2, or C3
 - needs 2 to 3 bits to encode
 - choose 3 bits: 001, 010, 100
- output open/closed can be: open or closed
 - needs 1 or 2 bits to encode
 - choose 1 bits: 1, 0

Sequential example (cont'd): encoding

- Encode state table
 - state can be: S1, S2, S3, OPEN, or ERR
 - choose 4 bits: 0001, 0010, 0100, 1000, 0000
 - output mux can be: C1, C2, or C3
 - choose 3 bits: 001, 010, 100
 - output open/closed can be: open or closed
 - choose 1 bits: 1, 0

reset	new	equal	state	next state	mux	open/closed
1	–	–	–	0001	001	0
0	0	–	0001	0001	001	0
0	1	0	0001	0000	–	0
0	1	1	0001	0010	010	0
0	0	–	0010	0010	010	0
0	1	0	0010	0000	–	0
0	1	1	0010	0100	100	0
0	0	–	0100	0100	100	0
0	1	0	0100	0000	–	0
0	1	1	0100	1000	–	1
0	–	–	1000	1000	–	1
0	–	–	0000	0000	–	0

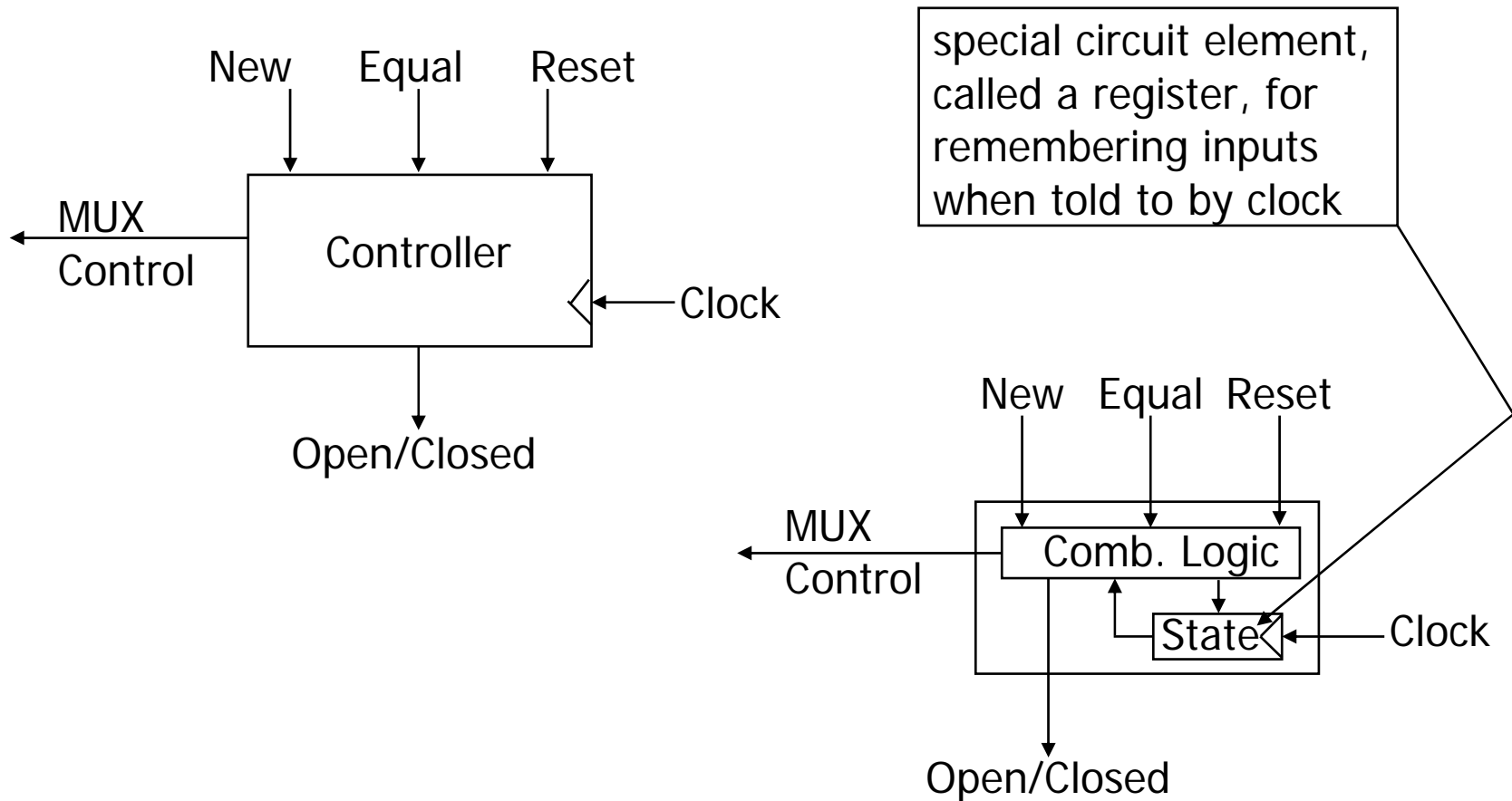
good choice of encoding!

mux is identical to last 3 bits of state

open/closed is identical to first bit of state

Sequential example (cont'd): controller implementation

- Implementation of the controller



Design hierarchy

