Lecture 21:

CMOS-MEMS (1)

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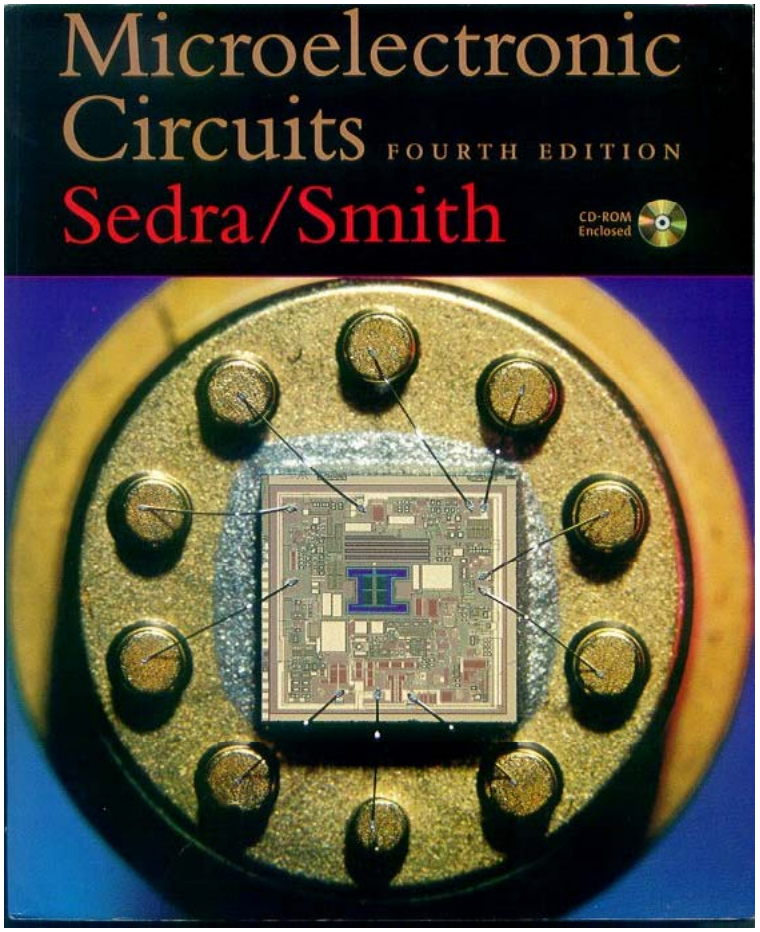
- What is CMOS-MEMS
- Basic CMOS fabrication
- Monolithic vs. hybrid integration
- Pre-CMOS integration
- Intermediate-CMOS integration
- Post-CMOS integration

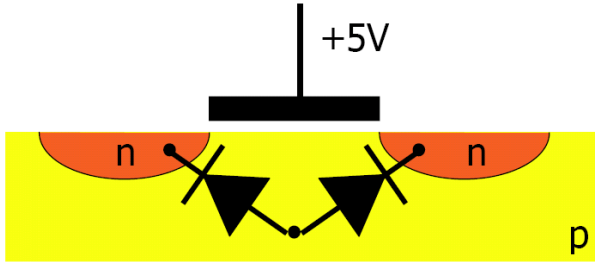
What is CMOS-MEMS?

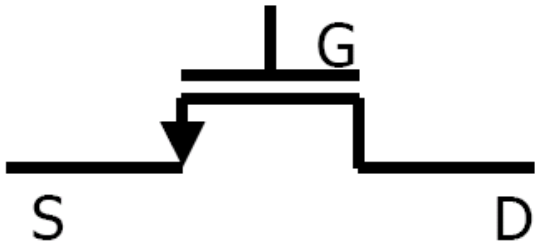
- Tight integration of sensor and electronics

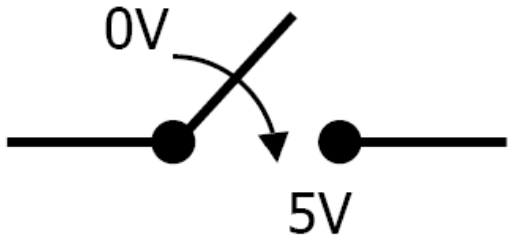


Basic CMOS fabrication: NMOS

- N-channel Metal Oxide Semiconductor
  - Positive charges on gate creates “n-type” channel in p-doped substrate

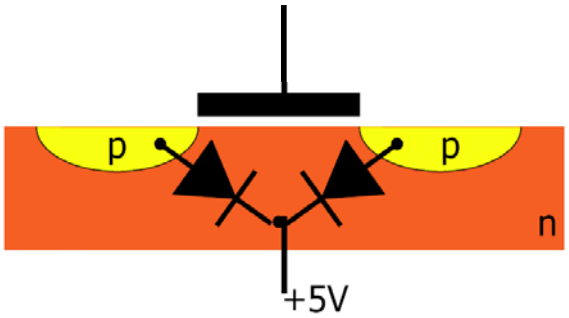


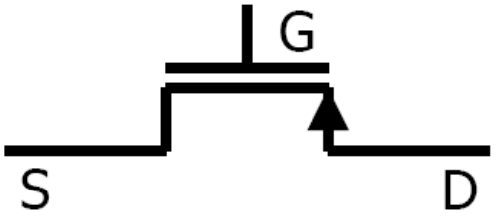


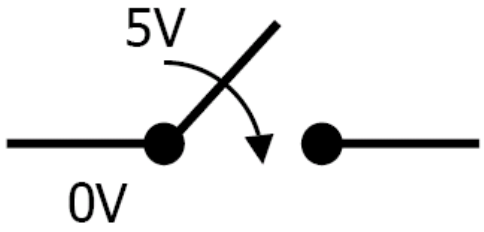


Basic CMOS fabrication: PMOS

- P-channel Metal Oxide Semiconductor
  - Negative charges on gate creates “p-type” channel in n-doped substrate

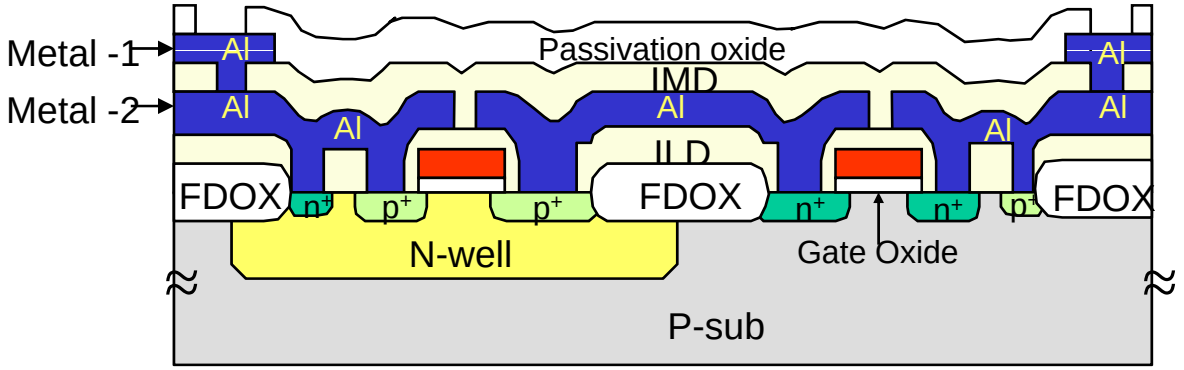






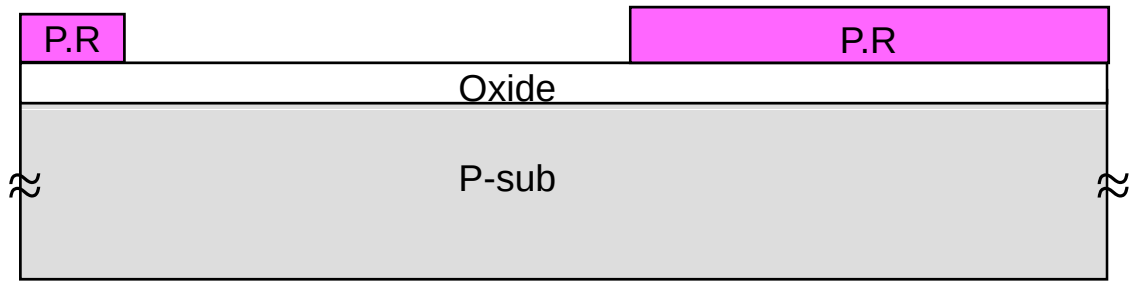
Typical CMOS fabrication flow

- Mask sequence (1P2M, ISRC1.5 process)
  - Well mask
  - Active mask
  - Field VT mask
  - Gate mask
  - N+ S/D mask
  - P+ S/D mask
  - Contact mask
  - Metal-1 mask
  - Via mask
  - Metal-2 mask
  - Pad mask



Typical CMOS fabrication flow (Cont'd)

1) Starting Material
   - •Dopant type : p-type (boron)
   - •Orientation : (100)
   - •Resistivity : 13±2Ω
   - •Wafer size : 4 inch
2) Wafer Inspection
3) Wafer Identification
4) Initial cleaning
   - •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
   - •HF (10:1) 10sec.
   - •D.I. Water rinse and dry
5) Initial oxidation
   - •Temperature : 1000C 130min.
   - •Thickness : 6000±6000Å
6) Well mask
   - •Mask I.D. : NWL
   - •HMDS. P/R coat, soft bake
   - •Align, Exposure
   - •Develop, CD check
   - •Hard bake



Typical CMOS fabrication flow (Cont'd)

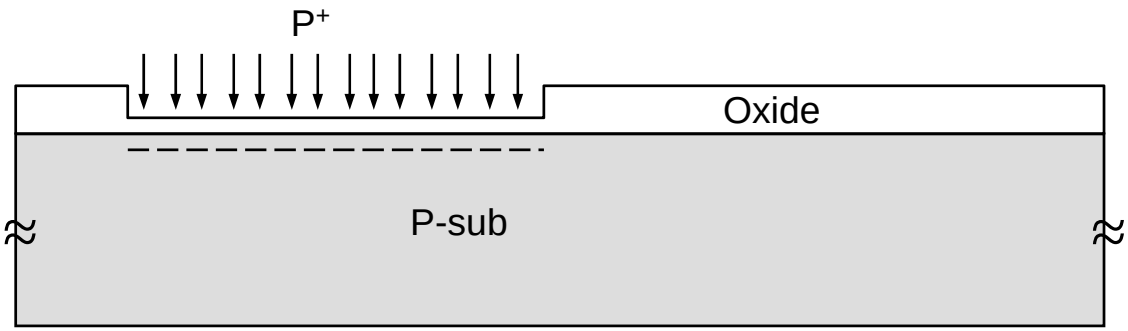
7) Oxide etch
- 7:1 BHF 6min

8) P/R strip
- H_2SO_4 : H_2O_2 (4:1) 10min. 120°C

3) Clean
- H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- HF (10:1) 10sec.
- D.I. Water rinse and dry

10) Thin oxidation
- Temperature : 950 °C, 31min.
- Thickness : 250±20Å

11) Well implantation
- Ion species : $_{31}P^+$
- Dose : $3.6x10^{12}/cm^2$
- Energy : 120keV



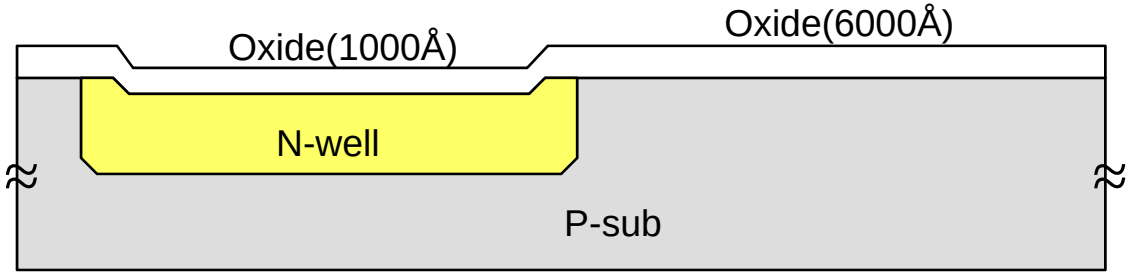
Typical CMOS fabrication flow (Cont'd)

12) Clean

- H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- HF (10:1) 10sec.
- D.I. Water rinse and dry

13) Well drive-in

- Temperature : 1100°C, 600min. N_2 + 1100 °C, 600min. O_2
- Thickness : 1000±100Å



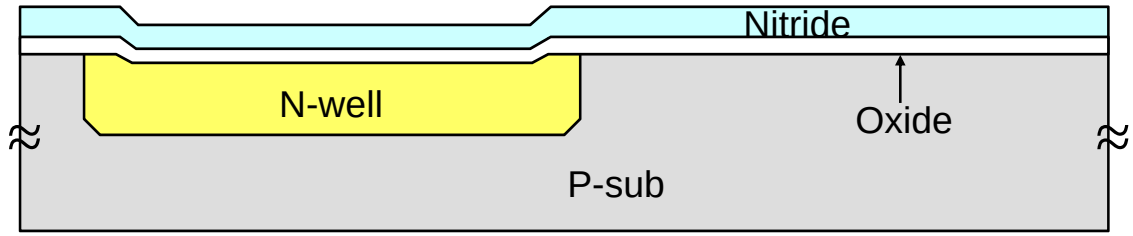
Typical CMOS fabrication flow (Cont'd)

14) Oxide strip
- •7:1 BHF

15) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •HF (10:1) 10sec.
- •D.I. Water rinse and dry

16) Buffer oxidation
- •Temperature : 1000 °C
- •Thickness : 450±40Å

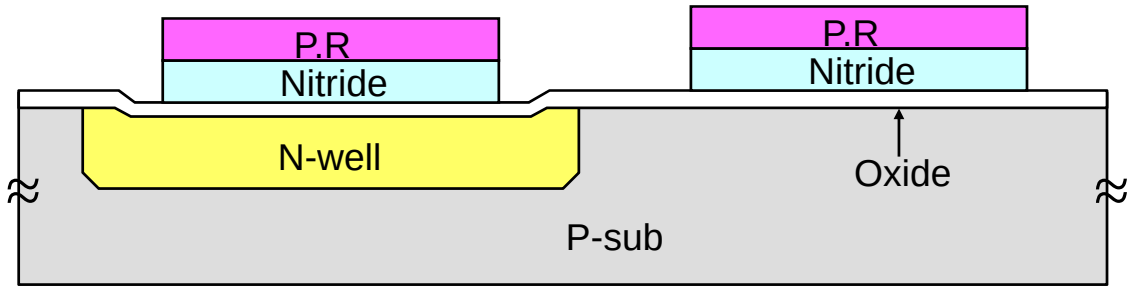
10) Nitride oxidation
- •Temperature : 785°C
- •Thickness : 1600±100Å



Typical CMOS fabrication flow (Cont'd)

18) Active mask
- •Mask I.D. : ACT
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check
- •Hard bake

19) Nitride etch
- •Reactant gas : CF_4+O_2

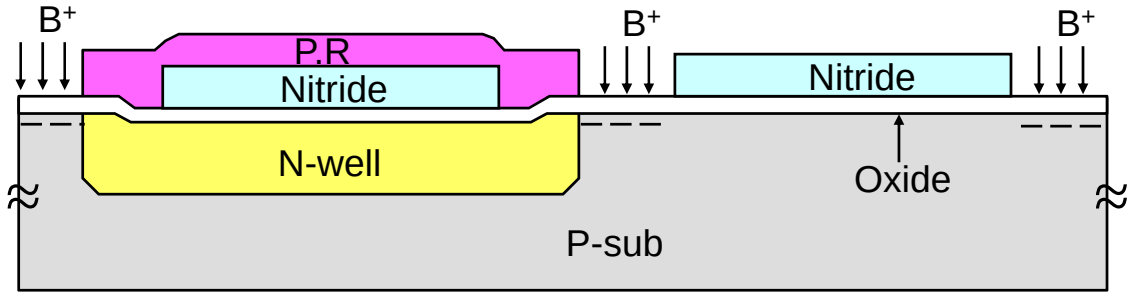


Typical CMOS fabrication flow (Cont'd)

20) P/R strip
- H_2SO_4 : H_2O_2 (4:1) 120°C

21) Field V_T mask
- Mask I.D. : FVT
- HMDS. P/R coat, soft bake
- Align, Exposure
- Develop, CD check
- Hard bake

22) Field implantation
- Ion species : $_{11}B+$
- Dose : $2.0x10^{13}/cm^2$
- Energy : 35keV



Typical CMOS fabrication flow (Cont'd)

23) P/R strip
- •H_2SO_4 : H_2O_2 (4:1) 120°C

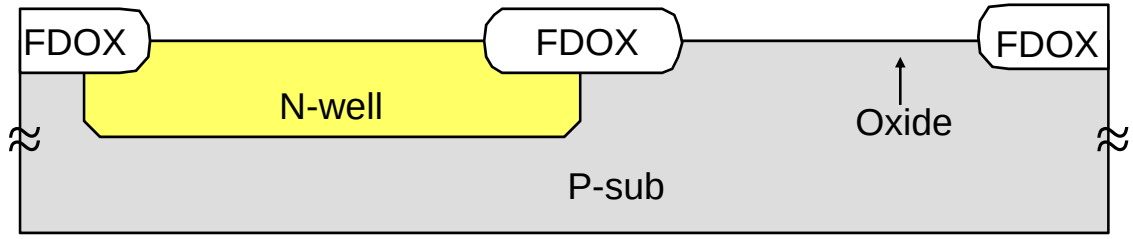
24) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •HF (10:1) 10sec.
- •D.I. Water rinse and dry

25) Field oxidation
- •Temperature : 950°C, 415min.
- •Thickness : 5500±500Å

26) Oxide strip
- •7:1 BHF 40sec.

27) Nitride strip
- •H_3PO_4 160°C

28) Buffer oxide strip
- •7:1 BHF 40sec.

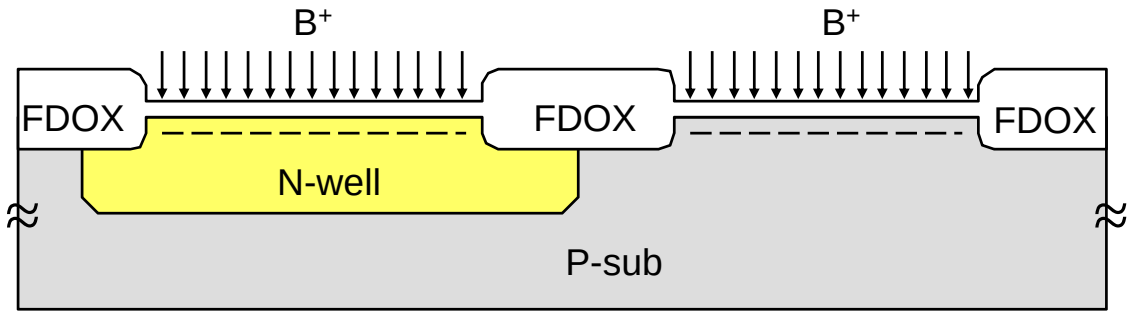


Typical CMOS fabrication flow (Cont'd)

29) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •HF (10:1) 10sec.
- •D.I. Water rinse and dry

30) Sacrificial oxidation
- •Temperature : 1000°C, 33min.
- •Thickness : 450±40Å

31) V_T implantation
- •Ion species : $_{11}B^+$
- •Dose : $1.5x10^{12}/cm^2$
- •Energy : 40keV



Typical CMOS fabrication flow (Cont'd)

32) Oxide strip
- •7:1 BHF 40sec.

33) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •HF (10:1) 10sec.
- •D.I. Water rinse and dry

34) Gate oxidation
- •Temperature : 950°C, 31min.
- •Thickness : 250±20Å

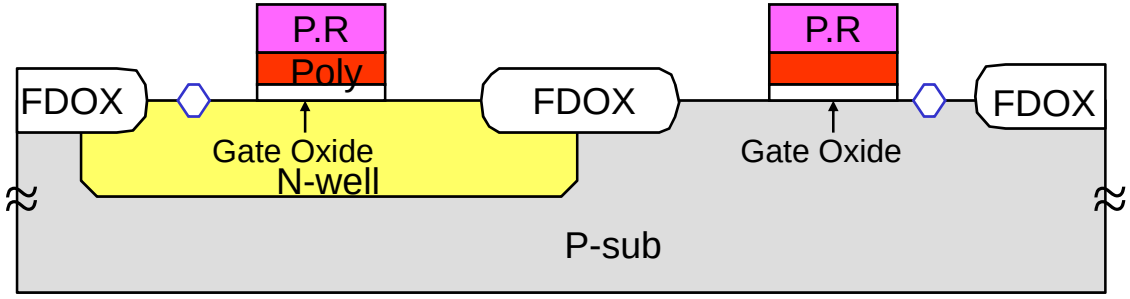
35) Poly deposition
- •Temperature : 625°C
- •Thickness : 3500±300Å

36) $POCl_3$ doping
- •Temperature : 900°C
- •20Ω/□ on poly

37) Deglaze
- •10:1 HF 30sec.

38) Gate mask
- •Mask I.D. : PLY
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

39) Poly etch
- •Reactant gas : Cl_2+He

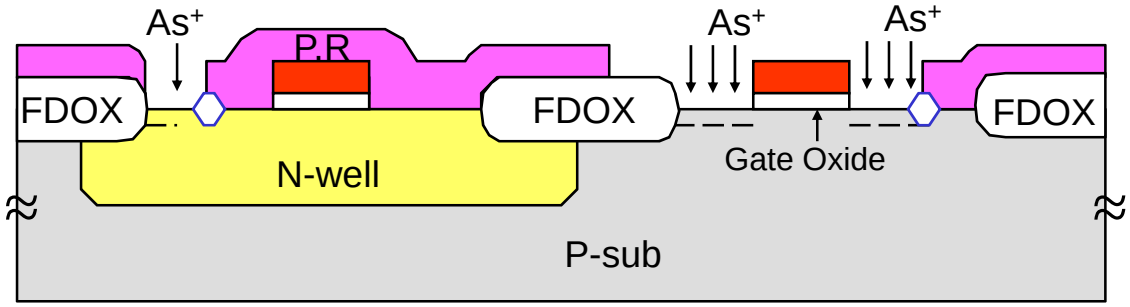


Typical CMOS fabrication flow (Cont'd)

40) P/R strip
- •H_2SO_4 : H_2O_2 (4:1) 120°C

41) N^+ S/D mask
- •Mask I.D. : NSD
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

42) N+ S/D implantation
- •Ion species : $_{75}As^+$
- •Dose : $5x10^{15}/cm^2$
- •Energy : 80keV



Typical CMOS fabrication flow (Cont'd)

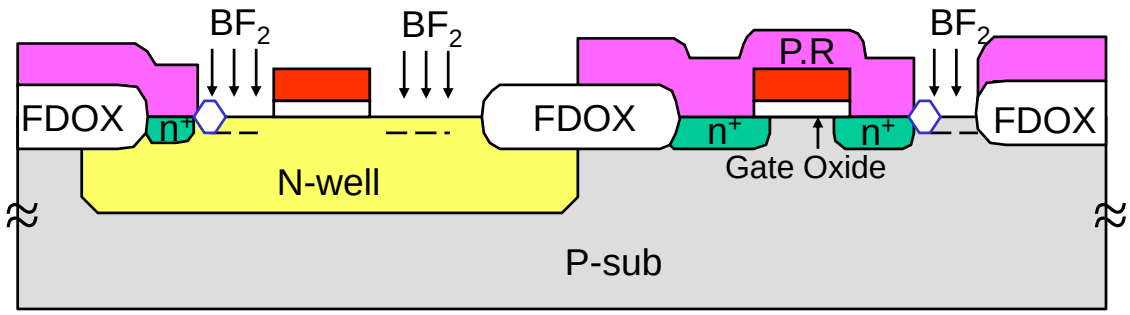
43) P/R strip
- •O_2 plasma
- •H_2SO_4 : H_2O_2 (4:1) 120°C

44) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •D.I. Water rinse and dry

45) Anneal
- •Temperature : 950°C, 30min.

46) P^+ S/D mask
- •Mask I.D. : PSD
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

47) N+ S/D implantation
- •Ion species : $_{49}BF_2^+$
- •Dose : $3x10^{15}/cm^2$
- •Energy : 40keV



Typical CMOS fabrication flow (Cont'd)

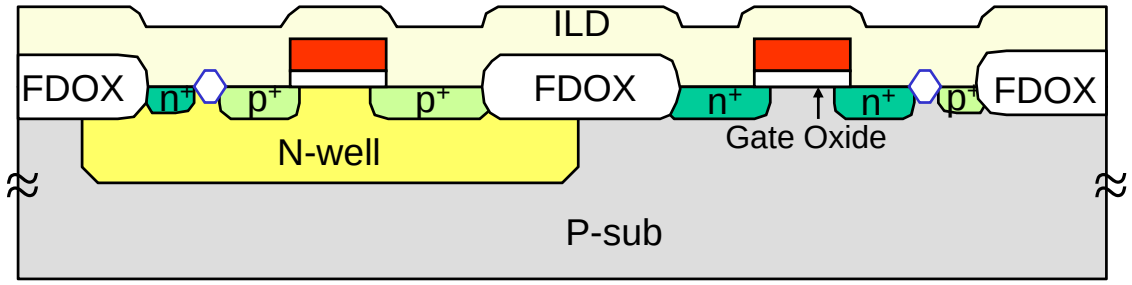
48) P/R strip
- •O_2 plasma
- •H_2SO_4 : H_2O_2 (4:1) 120°C

49) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •D.I. Water rinse and dry

50) Anneal
- •Temperature : 950°C, 30min.

51) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •D.I. Water rinse and dry

52) ILD deposition
- •Temperature : 375°C
- •Undoped LTO : 7wt%, LTO : TEOS (1000Å : 4000Å : 2000Å)



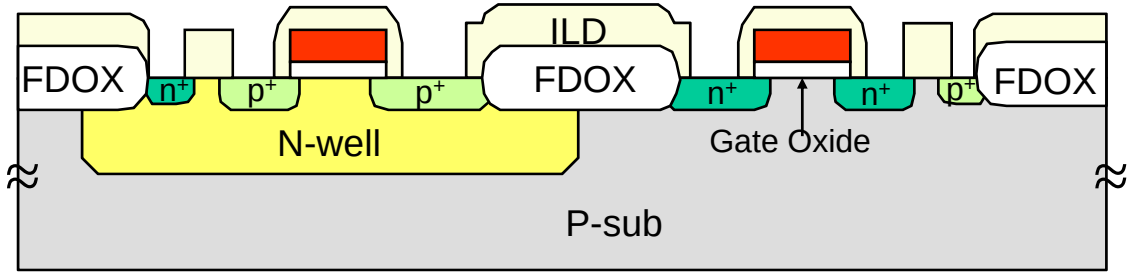
Typical CMOS fabrication flow (Cont'd)

53) Clean
- •H_2SO_4 : H_2O_2 (4:1) 10min. 120°C
- •D.I. Water rinse and dry

54) Reflow
- •Temperature : 950°C, 30min.

55) Contact mask
- •Mask I.D. : CNT
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

56) Contact etch (Wet+RIE)
- •RIE : CHF_3+CF_4+Ar



Typical CMOS fabrication flow (Cont'd)

57) P/R strip
- •O_2 plasma
- •H_2SO_4 : H_2O_2 (4:1) 120°C

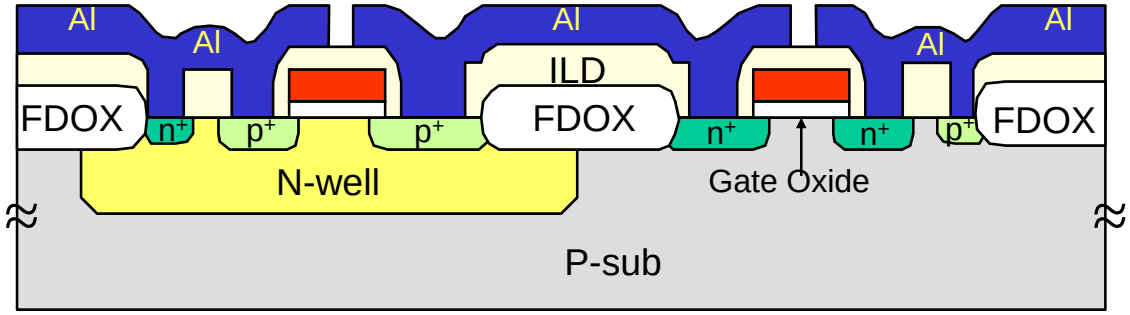
58) Clean
- •50:1 BHF, 120sec.

59) Metal deposition
- •Target : Al-1% Si
- •Thickness : 0.7μm

60) Metal-1 mask
- •Mask I.D. : MT1
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

61) Metal etch
- •Reactant gas : BCl_3+Cl_2 RIE

62) P/R strip
- •O_2 plasma
- •Solvent



Typical CMOS fabrication flow (Cont'd)

63) IMD deposition
- •TEOS 8000Å

64) VIA mask
- •Mask I.D. : VIA
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

65) VIA etch
- •RIE : CHF_3+CF_4+Ar

66) P/R strip
- •O_2 plasma
- •H_2SO_4 : H_2O_2 (4:1) 120°C

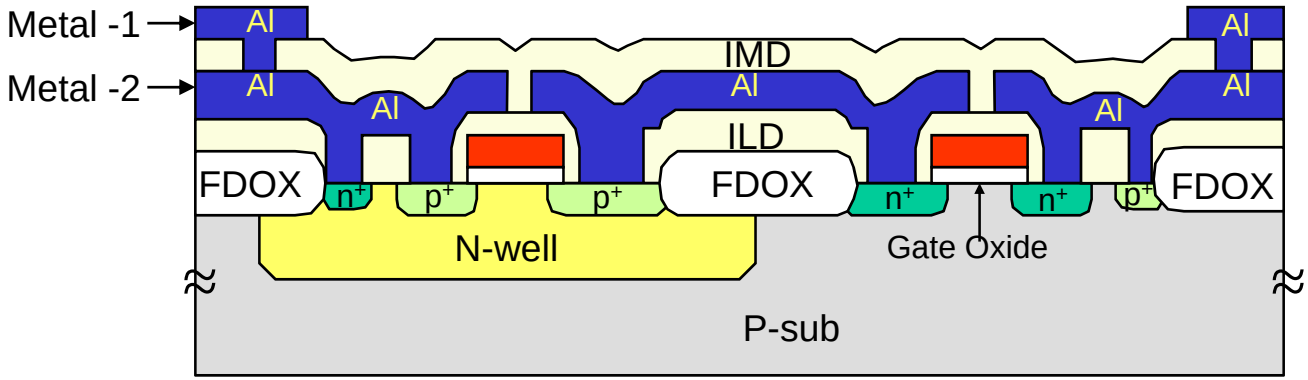
67) Pre-metal cleaning
- •50:1 BHF

68) Metal-2 deposition
- •Target : Al-1% Si
- •Thickness : 1μm

69) Metal-2 mask
- •Mask I.D. : MT2
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

70) Metal-2 etch
- •Reactant gas : BCl_3+Cl_2 RIE

71) P/R strip
- •O_2 plasma
- •Solvent



Typical CMOS fabrication flow (Cont'd)

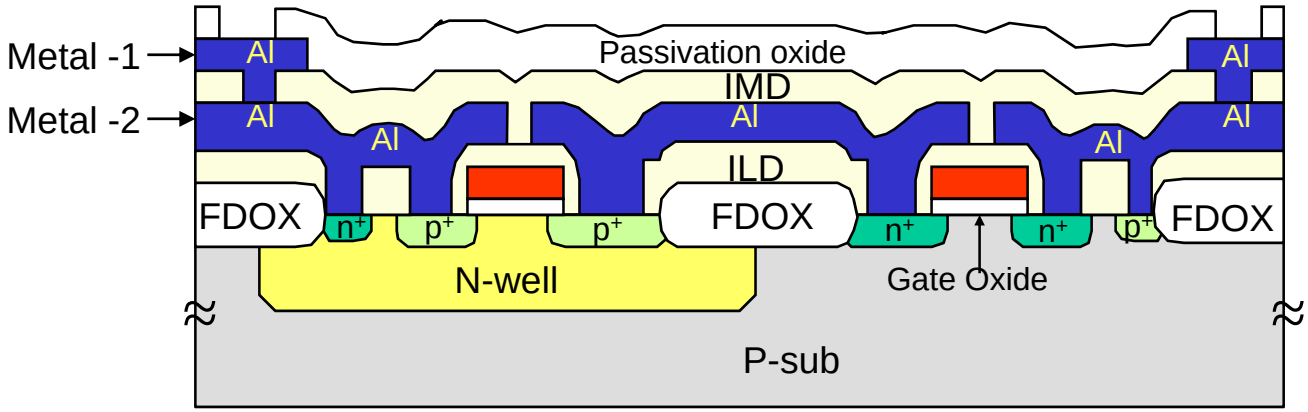
72) Passivation oxide
- •Thickness : TEOS 1μm

73) Pas mask
- •Mask I.D. : PAD
- •HMDS. P/R coat, soft bake
- •Align, Exposure
- •Develop, CD check •Hard bake

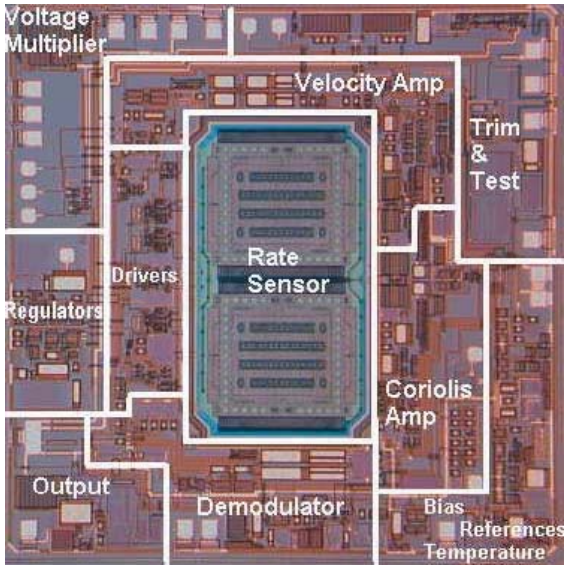
74) Pad etch
- •RIE : CHF_3+CF_4+Ar

75) P/R strip
- •O_2 plasma
- •H_2SO_4 : H_2O_2 (4:1) 120°C

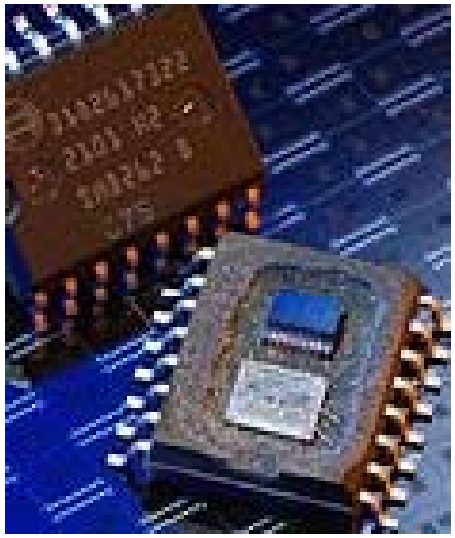
76) Alloy
- •Temperature : 450°C, 30min.
- •Ambient : 25% H_2 in N_2



Monolithic vs. Hybrid integration



Monolithic integration



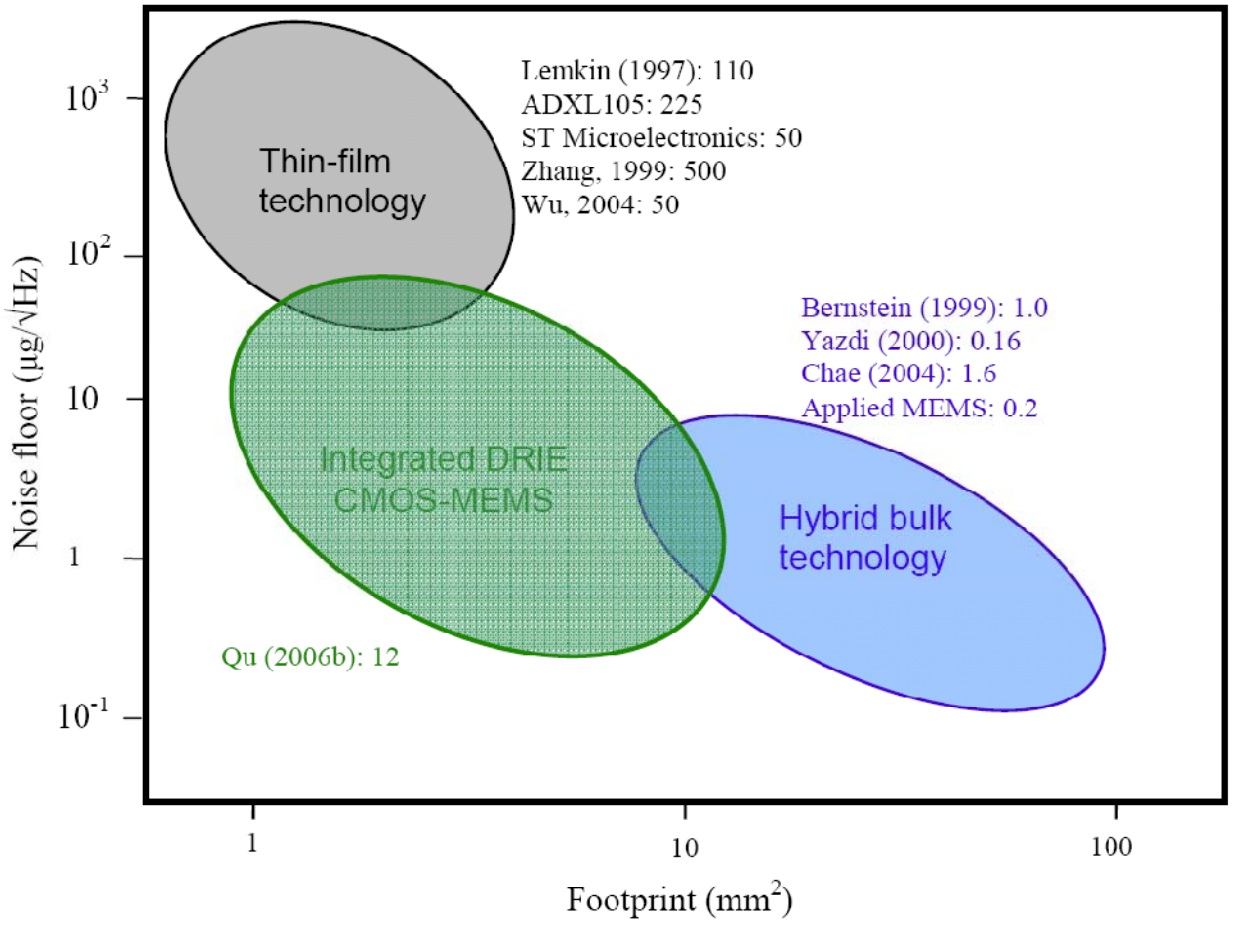
Hybrid integration

Monolithic vs. Hybrid integration (Cont'd)

	Monolithic integration	Hybrid integration
Integration	Single-chip integration	-Two-chip implementation -Integrated on a package
Process	Complicate process for iMEMS	Special processes are allowed (bulk micromachining, wafer bonding, etc.)
Cost	Low	High
Size	Small	Large
Performance	Low	High

Monolithic vs. Hybrid integration (Cont'd)

- Accelerometer case



Monolithic integration

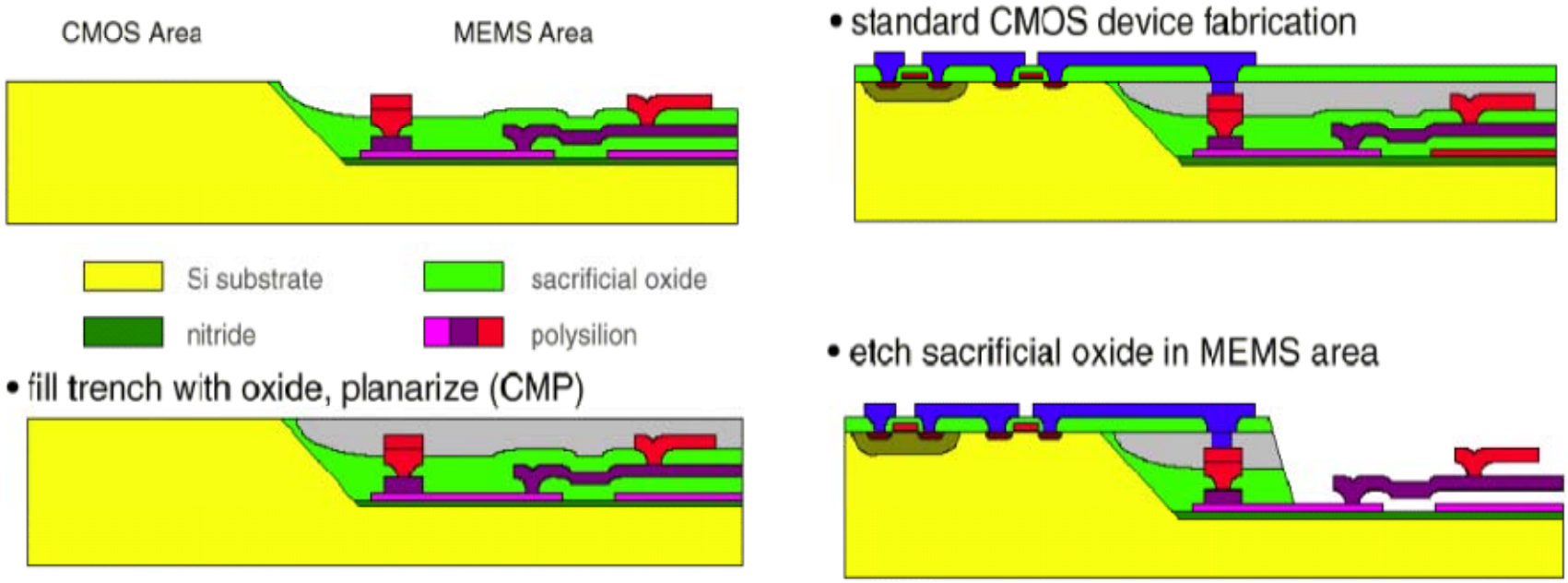
	Surface micromachining	Bulk micromachining
Pre-CMOS	Sandia Lab. (XL & gyro)	U. Michigan (pressure)
Intermediate-CMOS	Infineon (pressure) ADI (XL & gyro) Toyota (pressure)	
Post-CMOS (etching)		Motorola (pressure) Bosch (pressure) Carnegie M. (XL & gyro)
Post-CMOS (add-on layer)	Delphi (gyro) Texas Inst. (Mirror) UC. Berkeley (XL & gyro)	

Monolithic integration (Cont'd)

	Advantages	Disadvantage
CMOS	-Standard CMOS process	-limited application
Pre-CMOS	-No high temperature process during CMOS process	-Contamination issue in CMOS process
Intermediate-CMOS	-Optimized process for your device	-Complex and non-standard process
Post-CMOS (etching)	-Standard CMOS process can be used -Simple micromachining process	-High temperature micromachining process can affect to CMOS circuit
Post-CMOS (add-on layer)		

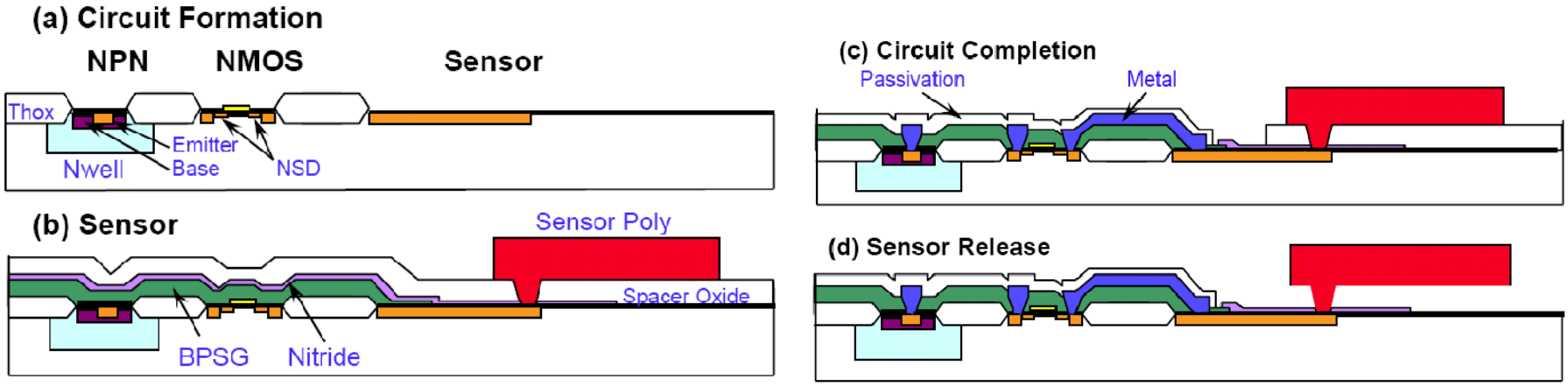
Pre-CMOS integration

- Pre-CMOS process example (Sandia Lab.)
  - CMP to planarize the wafer for regular CMOS processing
  - Wet etch to release MEMS structures
  - Need a dedicated production line



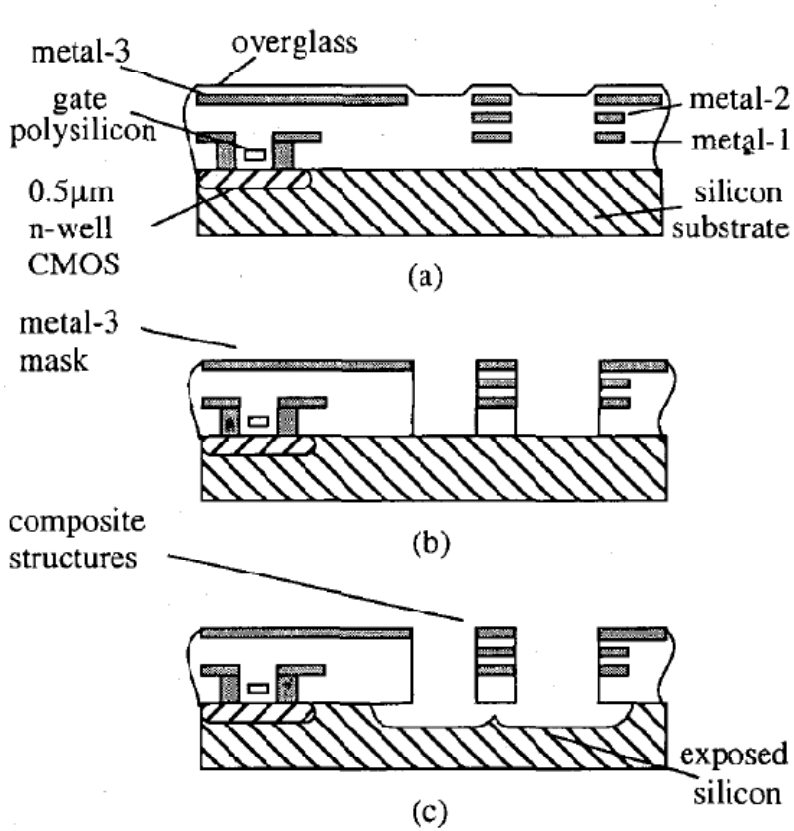
Intermediate-CMOS integration

- Intermediate-CMOS process example (ADI)
  - Form transistors on bare wafers first
  - Then deposit and anneal MEMS structural materials
  - No CMP needed
  - Wet etch to release MEMS structures
  - Need a dedicated production line



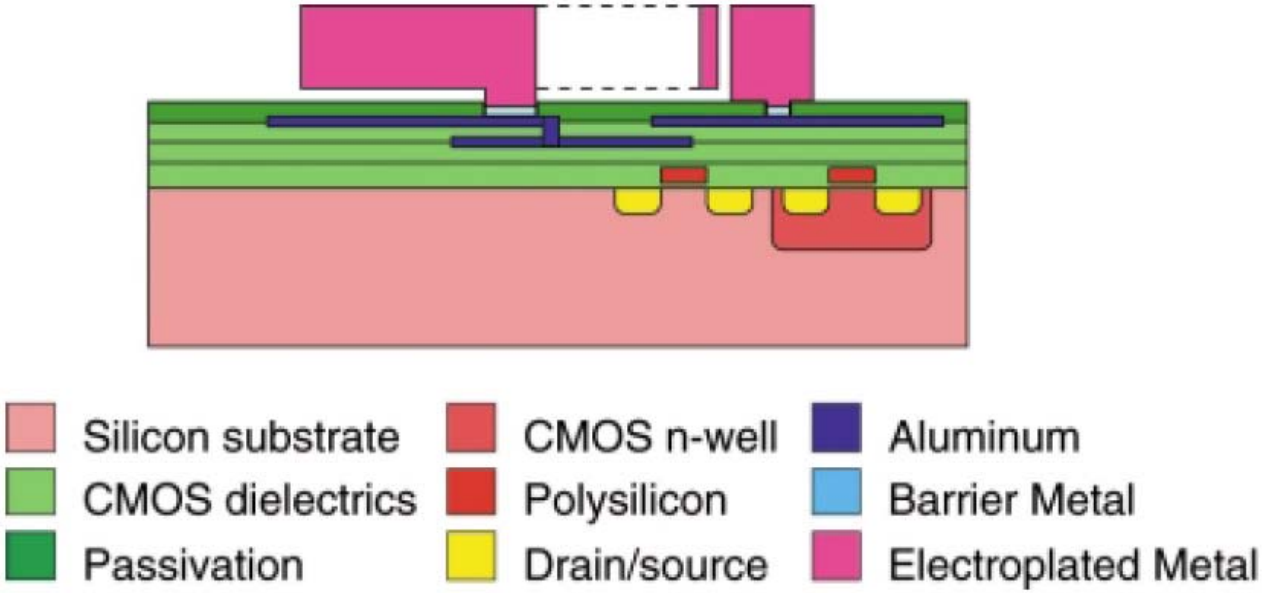
Post-CMOS integration (Isotropic etching)

- Post-CMOS process example (CMU)
  - Standard CMOS process
  - Top metal for MEMS mask
  - Isotropic etch for release



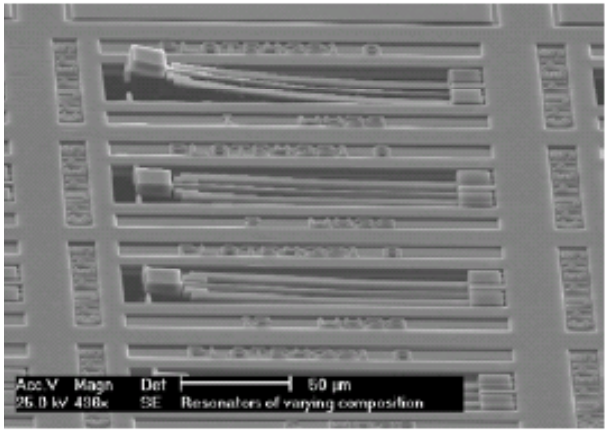
Post-CMOS integration (Electroplating)

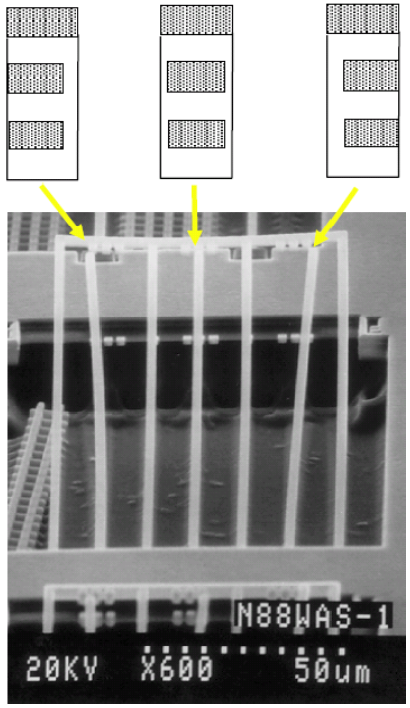
- Post-CMOS process example (U. of Michigan & Delphi)
  - Standard CMOS process
  - Electroplating for MEMS structure
  - Wet etch to release MEMS structures



Fabrication Issues on CMOS-MEMS

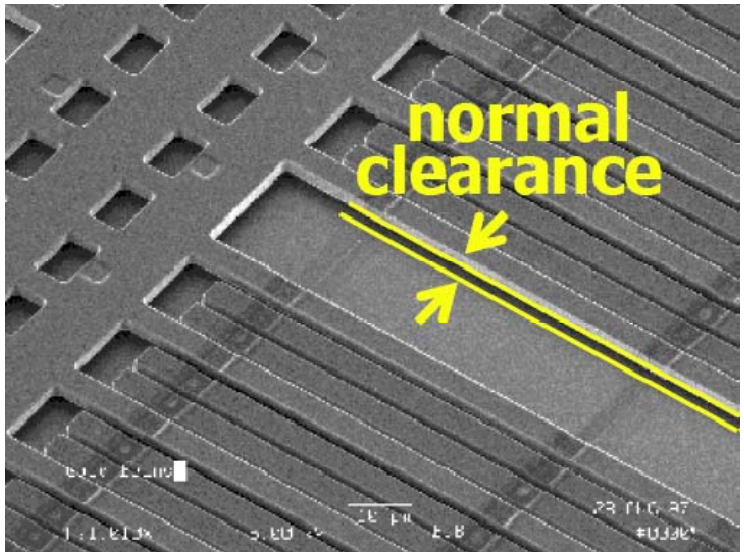
- Vertical curl in thin structure
  - Metal misalignment
  - Residual stress gradient

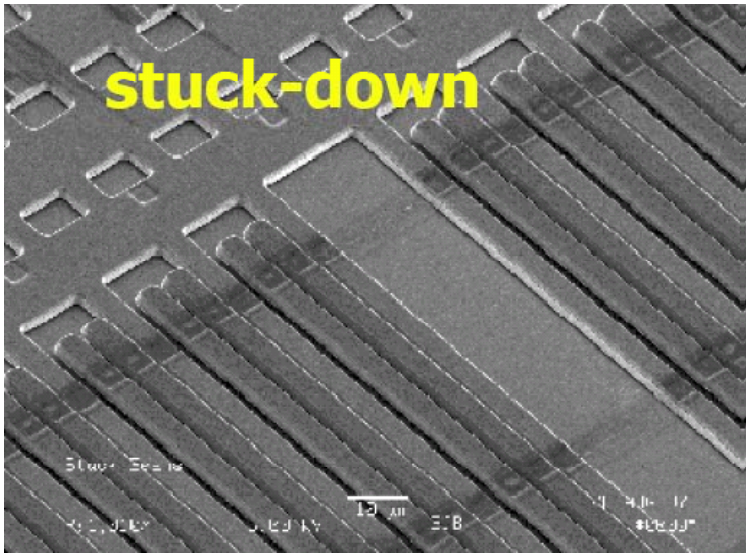




Fabrication Issues on CMOS-MEMS (Cont'd)

- Stiction problem
  - Surface tension in wet release





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