

VLSI IMPLEMENTATION OF AN ADAPTIVE EQUALIZER FOR ATSC DIGITAL TV RECEIVERS

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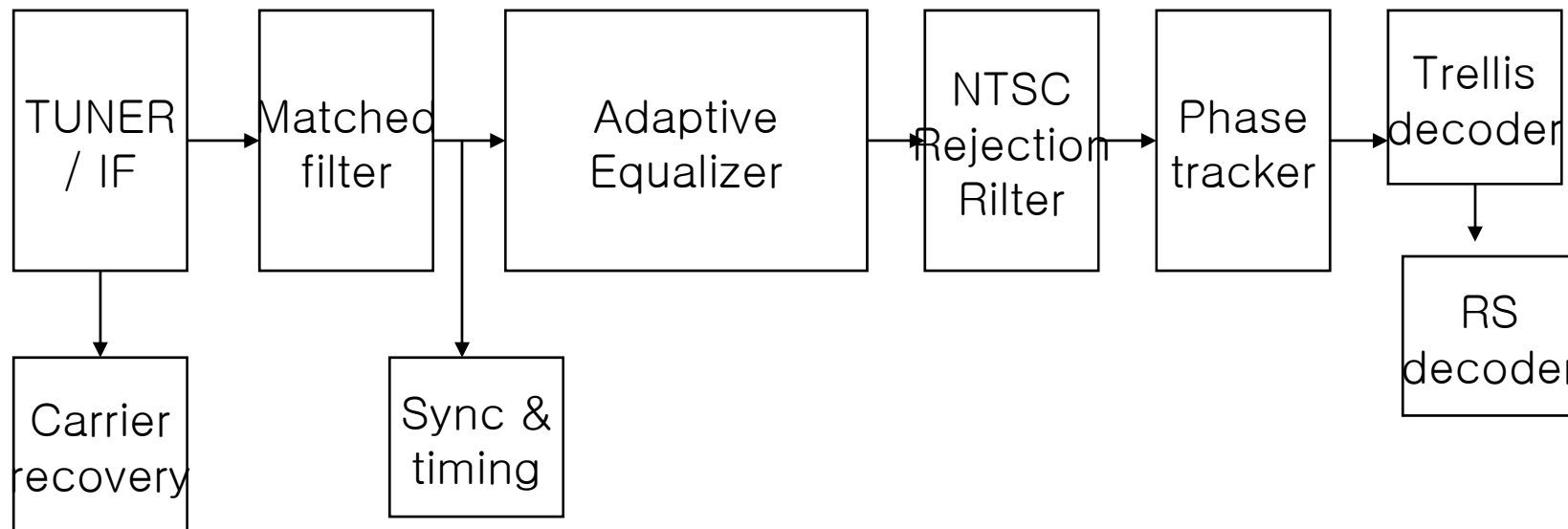
Contents

- Introduction
- Adaptive Filter Algorithms
 - Decision directed and blind adaptive
 - G-Pseudo Algorithms
- Optimization of Filter Word-lengths
 - Error thresholding & accumulation methods
- VLSI Design
 - Time multiplexing ratio selection
 - Programmable error calculation processor
- Results and Conclusion

Introduction

- ATSC Digital TV (Receivers)
 - USA standard/ maybe Korean
 - VSB modulation of digital data (similar to QAM, but only real-part is concerned)
 - Long length of adaptive filtering is needed (broadcasting – long channel delay, wideband, single carrier)
 - Co-channel interference with NTSC signal

ATSC Receiver Architecture

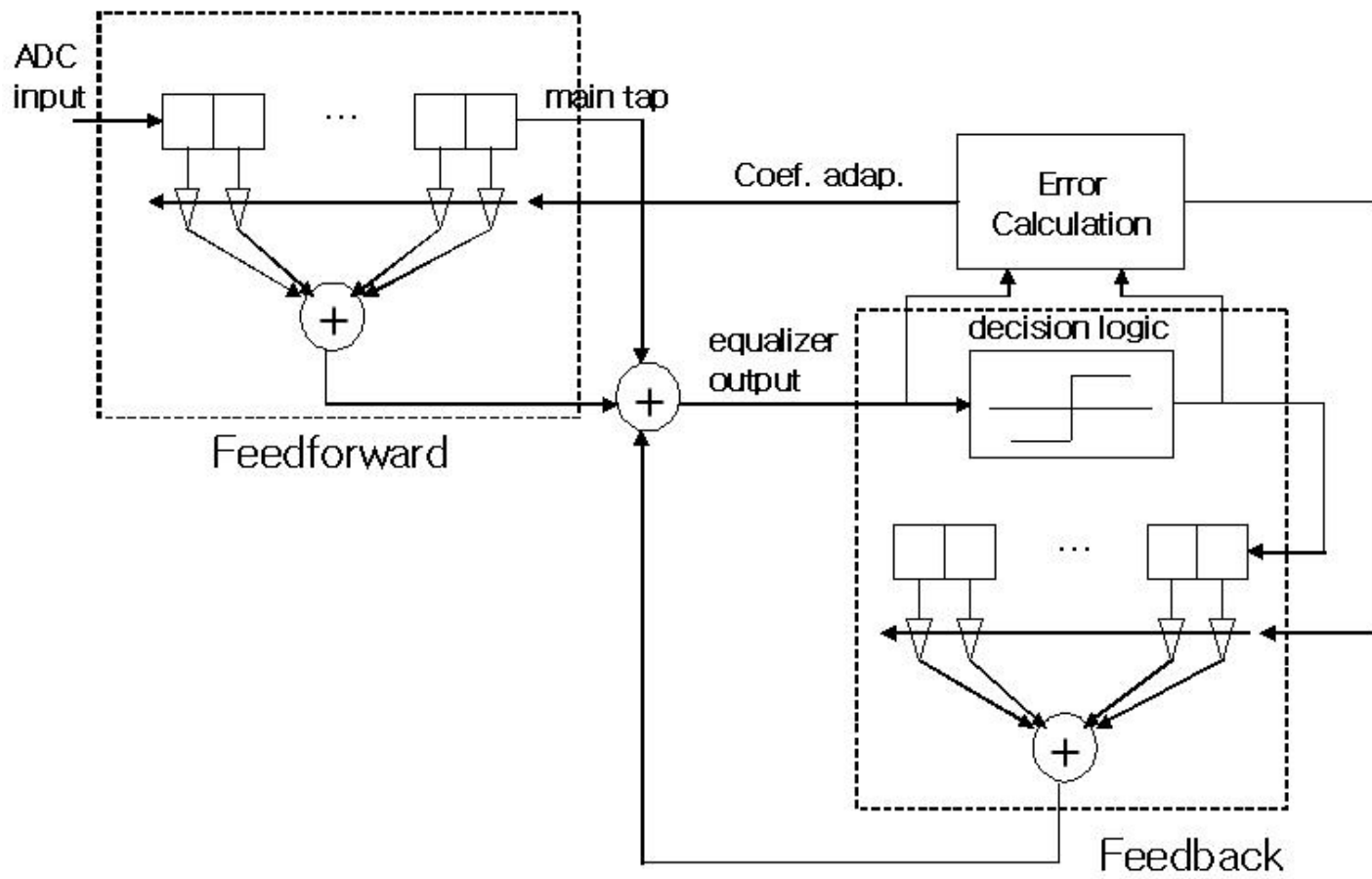


Adaptive filter:

Filter length is determined by the length of delay in the channel (256 norm

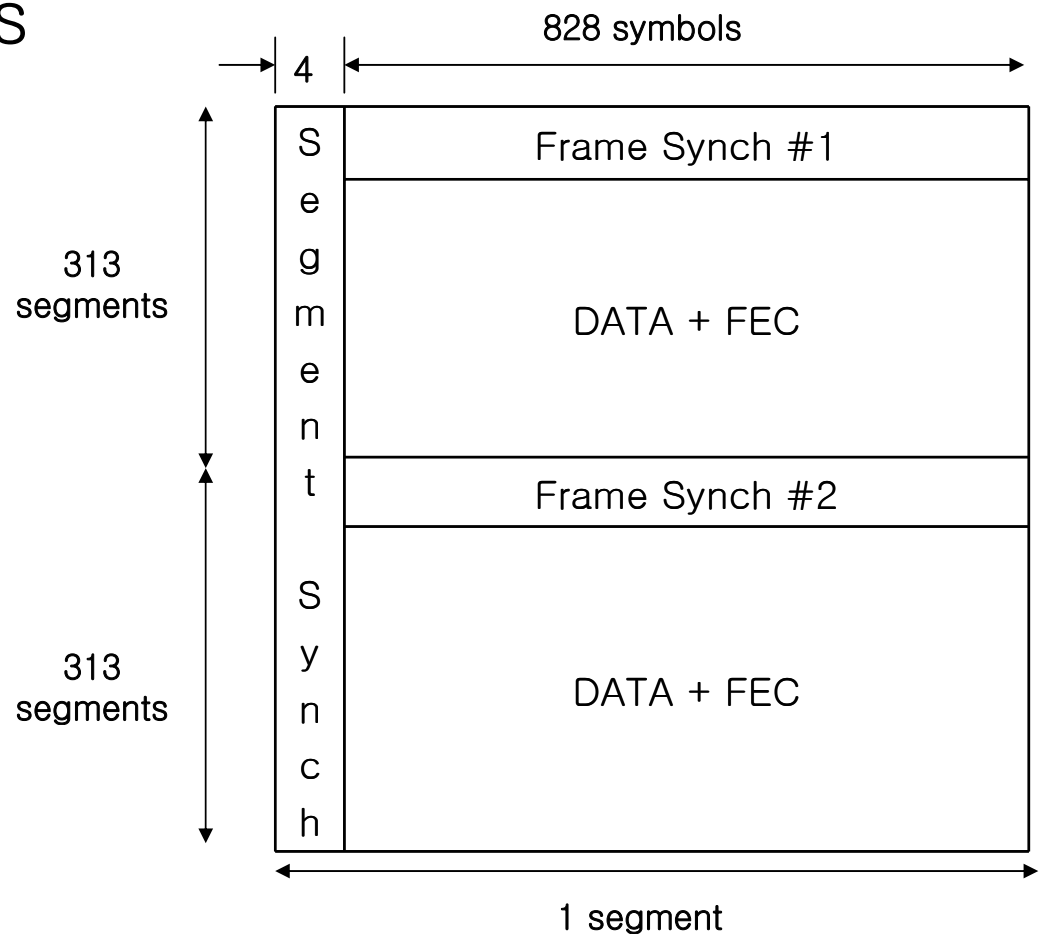
Design choice:

- Adaptation algorithms: fast convergence
- Filter word-length
- Architecture Design – 4 times/8 times multiplexed design
(circuit size/power) with programmable



ATSC Signal

- Each frame contains frame synch signal, every 16 msec.
- Frame synch is used for reference signal in adaptive equalization
- Conventional reference based initialization: need to wait until the synch field.



Decision Directed & Blind Algorithms

- Decision directed algorithms:
 - uses the error signal directly for adaptation
 - $d[n]$ is from decision results or reference data.
 - fast adaptation, but requires the eye-opening (wrong decision propagates ..)
- Blind adaptation:
 - Utilizes the statistical characteristics of the output signal, not relying on exact decision result
 - Can converge without needing the reference data
 - Slow adaptation, large word-length for filter coefficients

$$y(n) = \sum_k c_k(n)x(n-k)$$
$$e(n) = y(n) - d(n)$$
$$c_k(n+1) = c_k(n) - \mu e(n)x(n-k)$$

$$y(n) = \sum_k c_k(n)x(n-k)$$
$$e(n) = \Phi'(y(n))$$
$$c_k(n+1) = c_k(n) - \mu e(n)x(n-k)$$

G-Pseudo Algorithm

- Employs both decision directed and blind algorithms
- $e[n] = k_1 e_{DD}(n) + k_2 e_{DD}(n) e_{Blind}(n)$
 - $K_1 = k_2 = 1$
- $e[n] = |e_{DD}(n)| (K_1 \text{sgn}(e_{DD}(n)) + K_2 e_{blind}(n))$
 - <- when the eye is closed, the 2nd term contributes more to the total error.
 - <- works as the DD algorithm when the eye is open.
 - <- combines the advantages of both DD and blind algorithms

Optimization of Filter Word-lengths

- Blind algorithm needs to employ a very small adaptation step size because the adaptation is stochastic
 - 0.0001 for the decision directed
 - 0.0000003 for the G-pseudo
- Filter word-length needs to be long (DD: 13bits, Blind: 20 bits)

Adaptation time according to the filter word-length in the blind mode.

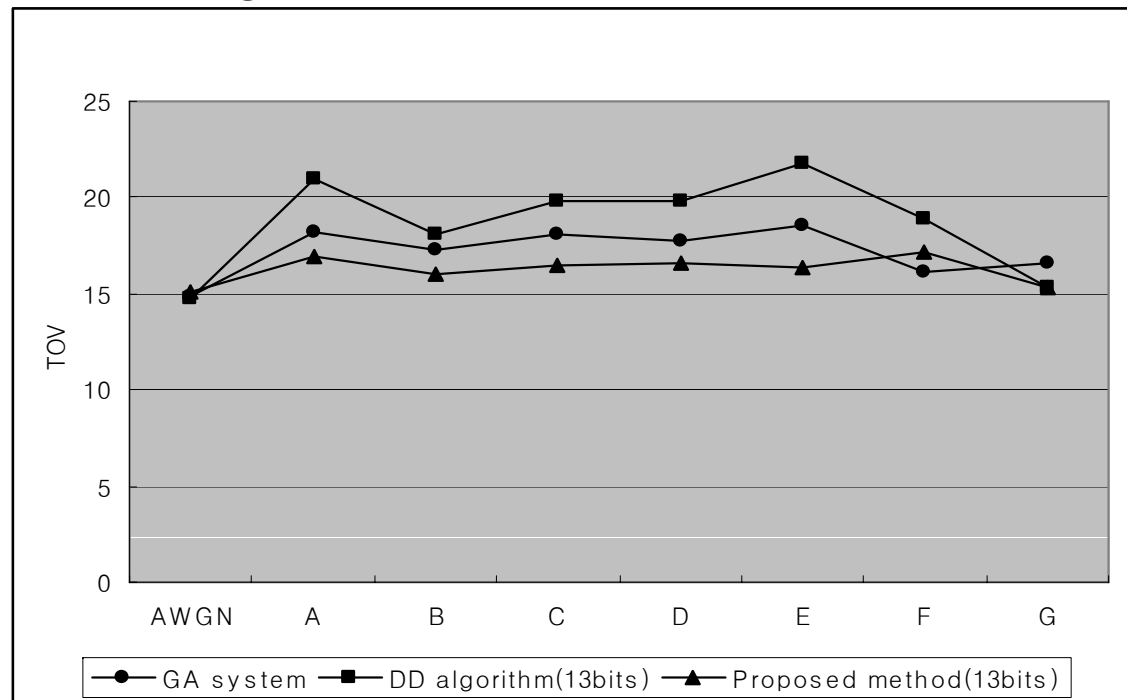
Coefficients word-length	Convergence time (number of symbols)
14	68000
15	51000
16	42000
17	38000
Floating-point	32000

Word-length Reduction for Blind Algorithms(1)

- Error threshold method
 - applies some threshold values to both the error and the input signal in order to neglect small changes, and only increases or decreases the filter coefficients value by 1.
- Error accumulation method
 - equips a small extra register at each filter tap, and increases/decreases the value of the registers according to $m \cdot e[n] \cdot x(n-i)$. When the value of the register overflows or underflows, it increases or decreases the value of the filter coefficients.

Word-length Reduction for Blind Algorithms(2)

- We employed the combined method
 - if ($|e(n)| > \text{threshold}$) {
 - if ($|x(n-i)| > \text{threshold}_x$) (4)
 - $ci(n+1) = ci(n) + 2 \text{sgn}(e(n)*x(n-i))2^{-(B-1)}$
 - else if ($|x(n-i)| > 0$)
 - $ci(n+1) = ci(n) + \text{sgn}(e(n)*x(n-i)) 2^{-(B-1)}$
 - }



Delayed adaptation

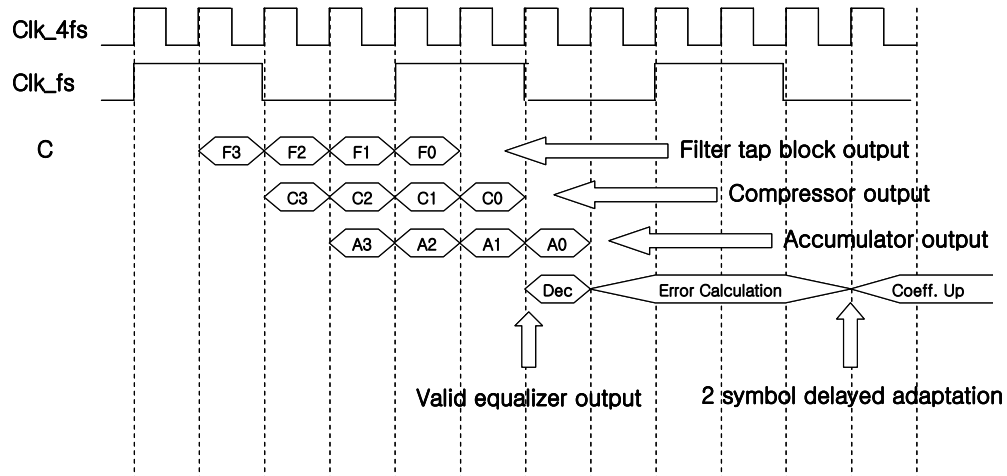
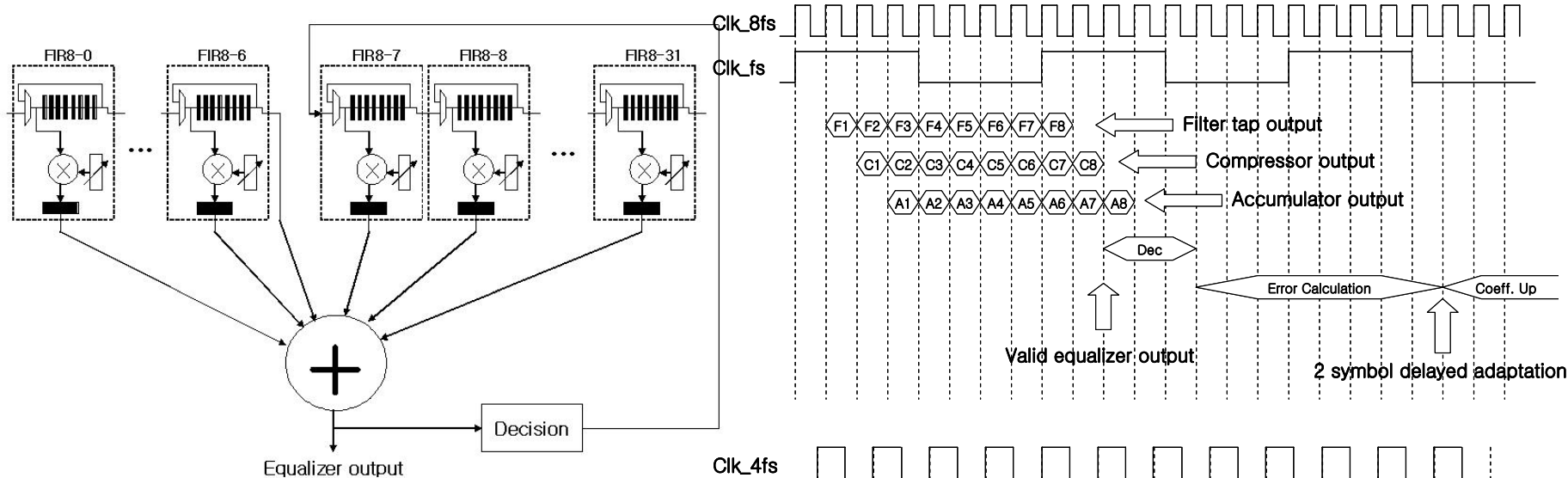
- Conduct adaptation using the error of the previous results
- Inevitable when there are pipelining delays in the filter ← high order filter requires more number of pipelining reg.
- Time-multiplexing helps, 1 symbol equals D delays
- 1 symbol/2 symbol delayed adaptation
 - Not much performance difference

Ghost Canceling for NTSC Reception

- Ghost canceling for NTSC reception
- Issues
 - The feedback path (decision feedback path in the adaptive filter) needs to have a higher word-length (8 bit if allowed).
 - Simulation results: 6 bit results in about 40 dB PSNR.
 - GCR signal restoration

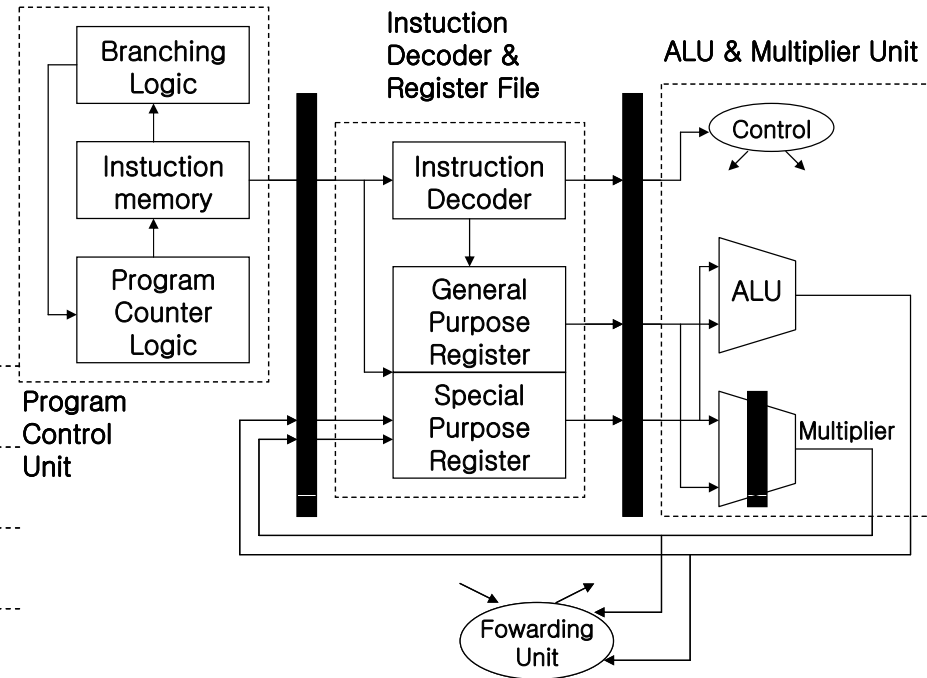
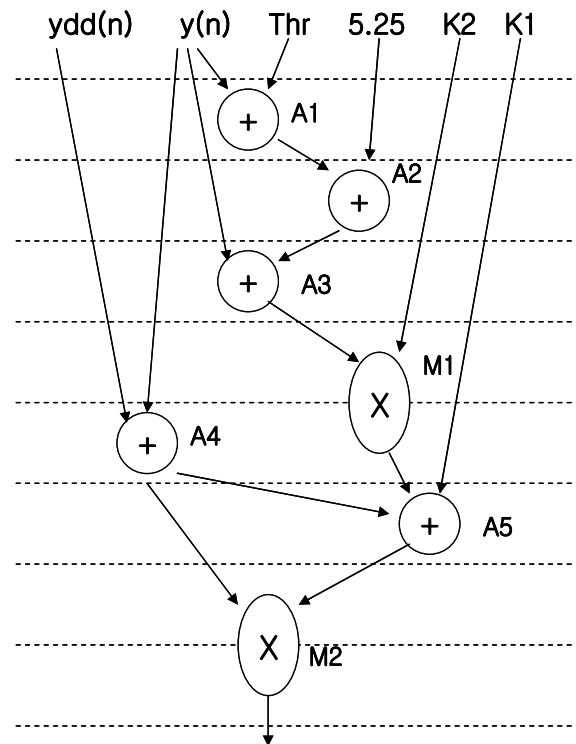
VLSI Design

- Algorithm optimization is done
- Architecture optimization for chip area, power consumption, and software programmability
- Time-multiplexing ratio ($f_{\text{sampling}} = 10.76 \text{ MHz}$)
 - $D = 4$ or 8 ?
 - Larger D means less chip area for multipliers (combinational logic)
- Error calculation unit architecture
 - Programmable or hardwired?



Programmable Error Calculation Processor

- Need to support various adaptation modes
- The blind eq. algorithm requires 8 cycles with one pipelined multiplier and one adder.



Implementation Comparisons

Estimation of chip area (NAND gate equiv.)

	4fs	8fs
Comb. Logic	64,328	32,895
Seq. Logic	51,513	43,821
Interconnection	103,385	62,761
Total	219,226	139,478

Estimation of power consumption (mW)

	4fs	8fs
Cell	184	288
Net	122	180
Total	306	468

Concluding Remarks

We implemented an adaptive equalizer for ATSC TV. This chip is (has)

- (1) robust to dynamic channels
- (2) low hardware complexity due to wordlength optimization and combining error accumulation and error thresholding method
- (3) programmable error calculation processor
- (1) time-multiplexed architecture optimized for area and power consump.

Die Size	8mm*8mm (0.35 mm)
TOV in the system level	15.3 dB
Channel acquisition time	within 0.2 sec
NTSC co-channel interference	D/U = 2 dB
AGC gain	more than 60 dB
Frequency lock	-200KHz ~ 250 KHz

Adaptive Equalization with Comb-filtered Signal

- Comb filtering for NTSC co-channel interference rejection
- Requires a different blind algorithm

