Goal;

To introduce the trend of MOSFET structures in terms of the gate material and the gate insulator material and other MOSFEF structures than the conventional MOSFET built on the bulk silicon;

SOI MOSFET
Double gate MOSFET
FINFET and tri gate MOSFET

A. Trend of the conventional CMOSFET structures

ref. Plummer et. al., " Material and Process Limits in Silicon VLSI Technology," p. 240, Proceeding of IEEE, 2001

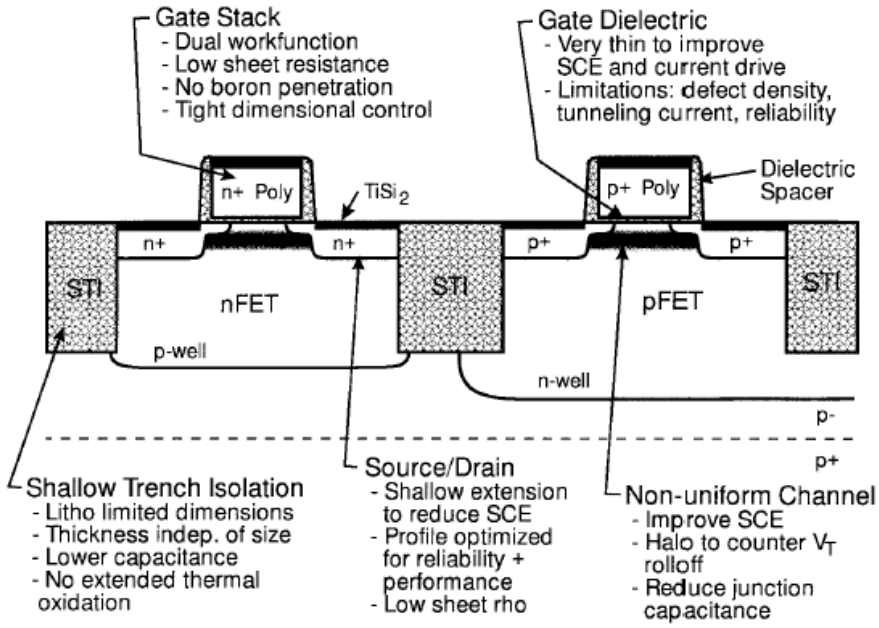
As explained in the sections 5-5, MOS limit may come from the increase in the drain leakage and gate leakage mainly due to ;

a) difficulty in controlling the electrostatics in lateral direction(electric field from the drain)
b) increase in tunneling current in vertical direction(GIDL and gate tunneling)

Difficulty in a) above is more serious for PMOSFET due to the unbalanced work function difference if N+ polysilicon is used.

A-1: CMOS type 1;

In order to ease the problems associated with the scaling, many innovations in the device structures have been proposed and utilized in the manufacturing.



- the figure in the above summarizes the factors to be considered in the bulk CMOS design. In the lecture, no attempts are made in the detailed design consideration of the channel doping. Please refer the reference and rf's in the chapter 1-1. Instead the metal gate material options will be covered briefly, since it may give effects to the channel doping for reasonable V_T.

- Metal gate instead of poly-silicon

Metal gate instead of poly-silicon has been proposed as means of the substitute to the polysilicon since polysilicon is not suitable to the new high k materials. The side effects(benefits) are low resistance and the no gate depletion.

Problems are the difficulty in reducing V_{th} without decreasing the channel doping if the midgap material is used.

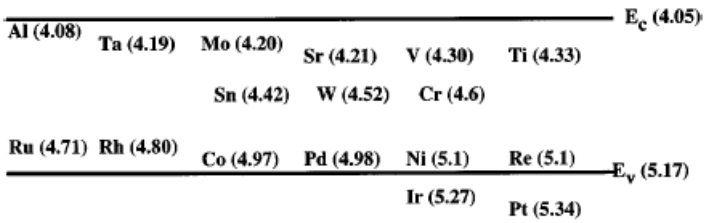
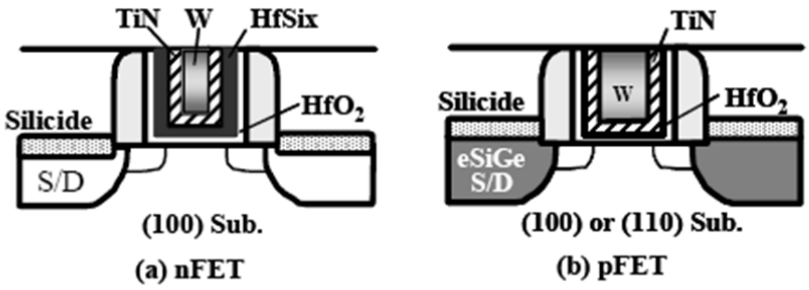


Fig. 12. Workfunctions of possible metal gates.

A-1: CMOS type 2 adopting 'mobility enhancement' and 'high k material'



- In the above picture, a typical CMOS structure adopted in the 50n-40nm technology node is shown as an example. Three features to be noticed are ;
  * adoption of the metal gate
  * stresse layer(capping layer for NMOSFET) and SiGe implantation for PMOSFET and
  * adoption of HfO2 as the gate dielectric (to reduce the gate leakage for same T# : equivalent oxide thickness)

B-1. Un-conventional MOSFET structure

- Most of the structures different from the conventional MOSFET structures have been introduced mainly for better 'electrostatic' control of the drain field. The situations may be best understood from following two figures.

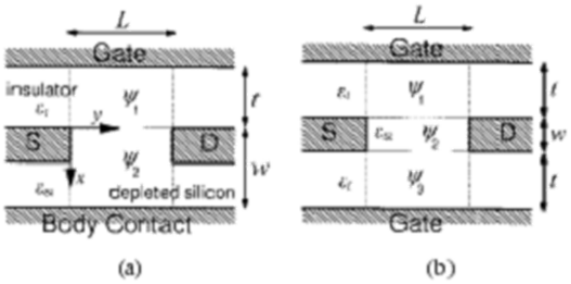
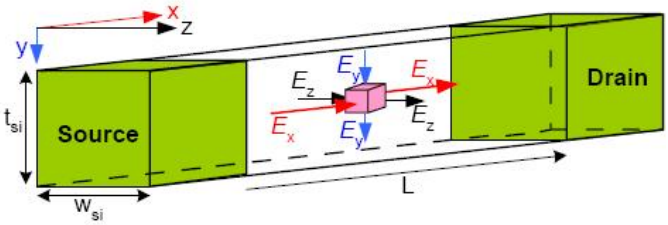


Fig. 1. Schematic cross section diagram of (a) a bulk MOSFET and (b) double-gate MOSFET.

Fig 1 from Frank, et.al., Generalized scaling length of for two dimensional effects in MOSFET's, IEEE EDL, Oct. 1998



$$Electrostatic\ Control \propto \sqrt{\frac{n\varepsilon_{ox}}{\varepsilon_{si}}\frac{1}{t_{si}t_{ox}}}$$

n=number of gates; t_{si} is assumed equal to W_{si}

Fig. Electrostatic controllablity from the gate(s) is the function of silicon and oxide thickness, number of gates etc.(form Collinge, INC03, 2007, Belgium)

B-1. SOI(silicon on Insulator)

ref.

- Transistors are built on the Thin silicon film on the BOX(Buried Oxide Layer, ~ 2000-3000Å Basic motivations are better isolations and reductions in the depletion capacitances. According to the magnitudes of W_d and T_{ob}, transistors are classified as the FD(fully depleted) and PD(partially depleted) devices.

PD Device operations are same as the bulk MOSFET except the junction capacitance and the short channel characteristics due to the junction overlap region.

- The operation of the FD can be best described by the following sketch on the vertical field profile.

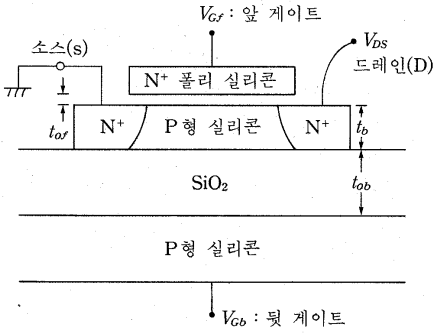
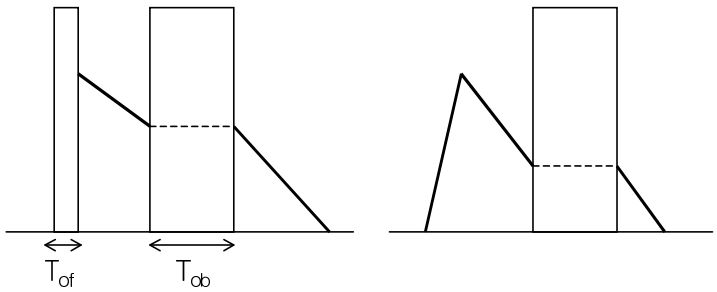


그림 8-1 SOI MOSFET의 단면



(a) channel (b) drain section

- FD(Fully depleted) vs. PD(Partially Depleted) SOI

  - 'artially Depleted structure
    - * Kink effect
    - * Body contact is needed
    - * better V_T control than FD
    - * Body control is possible(various circuit technique)

  - ully Depleted structure
    - * Better body instability problem
    - * V_T process control is difficult since Tsi determines the V_T

- Pros and Cons of SOI Devices

Pros(Compared with bulk CMOS)

- ınction related
  - * Smaller junction capacitance; 4-7 times less in modern VLSI
  - * Smaller junction related leakage current(3-4 orders of magnitudes smaller)
  - * smaller SEU(Single Event Upset) events

- ubthreshold characteristics
  - * Larger subthreshold slope due to weak coupling of channel to substrate $1/nk_BT$ (n=1.05 whereas 1.3 to 1.5 in bulk)
    (see fig. 1 and 5 and table 1 of IEDM 94, p 819)
  - * leakage current is 3-4 orders of magnitude smaller at 300C

- Jo BJT latch up due to perfect isolation between N and PMOS

- Disadvantages
    - nstabilities caused by the floating body effect
      * Kink in PD,
      * single transistor latch up
    - 'oor thermal conductivity of buried oxide
      * negative i_D-V_D characteristics
      * Poor ESD characteristics
    - 'oor gate oxide integrity and possible hot carrier effects
    - -5 times higher cost

- Scaling properties
    - 'hinning of silicon thickness
      * Mobility degradation concern(IEDM 95 pp847-850, IEDM94 p645)
        (Mobility degrades from T_{si} of 200Å
    - V reduction ; better back bias control
    - Jo degradation of subthrehold slope with channel doping concentration

B-2. Double gate MOSFET and Gate All Around structure

ref. 2 of chapter 1(Wong et. al, pp.550-553)
ref. Good modeling paper from Baccarani, TED, 1998

a) Double Gate MOSFET structure

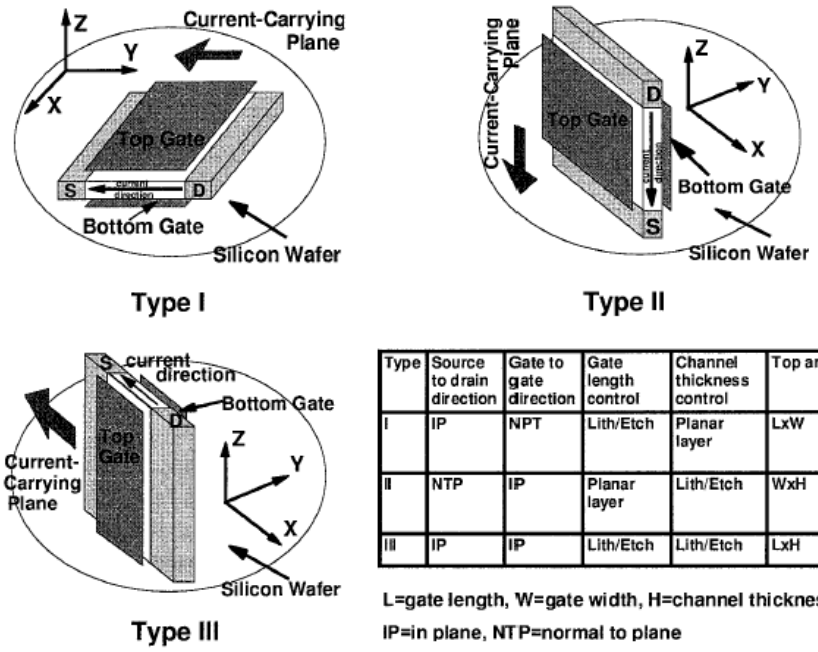
As the substrate of the conventional MOSFET(single gated MOSFET) plays the "electrostatic shield", there is the tradeoff between the degree of the shielding and the substrate slope.

DG MOSFET does not have the above problem and advantage solver the conventional MOSFET in

* high transconductance
* low channel doping and
* high mobility due to low effective electric field.

- Three types adopting the double gate structures be classified according to their arrangement;

Table 5
DG FET—Topological Considerations (Adapted from Wong *et al.* [113])



Type	Source to drain direction	Gate to gate direction	Gate length control	Channel thickness control	Top area
I	IP	NPT	Lith/Etch	Planar layer	LxW
II	NTP	IP	Planar layer	Lith/Etch	WxH
III	IP	IP	Lith/Etch	Lith/Etch	LxH

L=gate length, W=gate width, H=channel thickness,
IP=in plane, NTP=normal to plane

b). FINFET

ref. D. Hisamoto, et. al., " FinFET - A Self Aligned Double Gate MOSFET scalable to 20nm", TED, pp2320-2325
Other followers, IEDM 01, p 421
IEDM 02 HO # 3

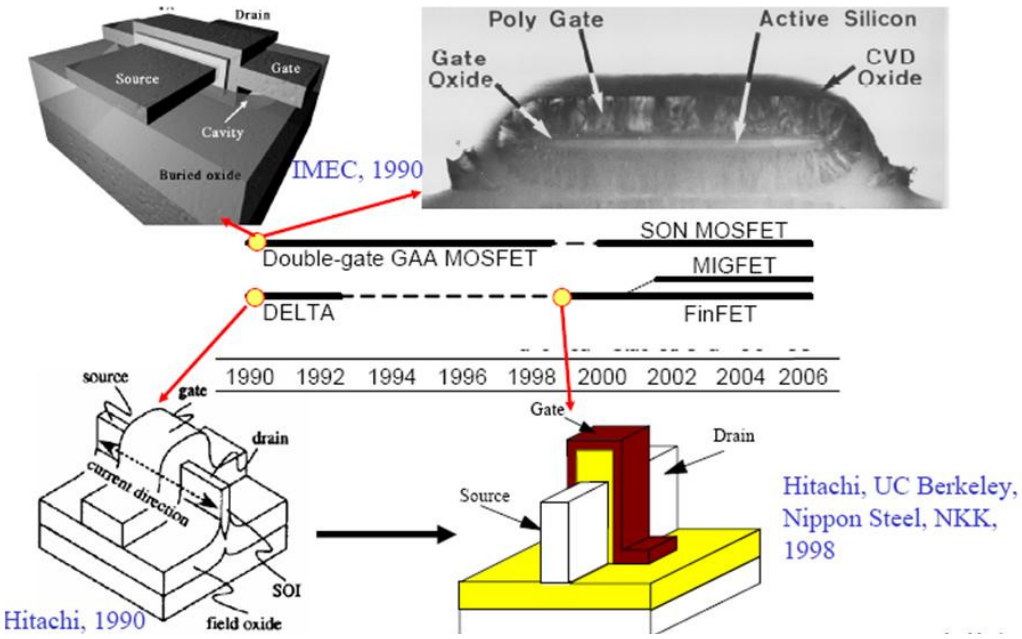


Fig. Summary of the evolution of the DG FET structures(From Collinge, INC3, 2007, Belgium)

- The electronic states in the thin silicon of the DG FET can be best understood by 'bulk' quantization shown in the following figure.
Baccarani could obtain the analytical solution for the energy states(so the inversion layer charges) assuming constant Ec in the silicon (constant Vp in the Schrodinger equation).

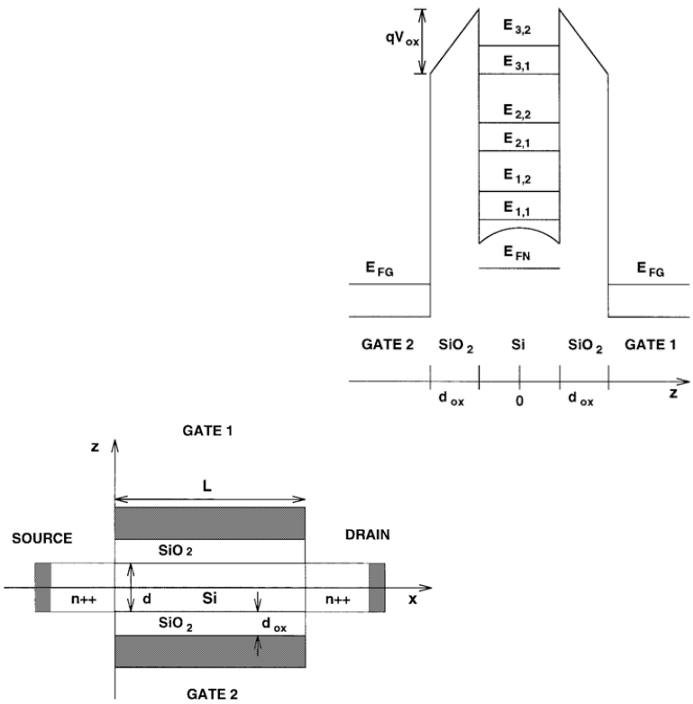


Fig. The situation in the DGFET. Notice that energies in the thin silicon are quantized, called the 'bulk quantization'.

- Advantages in scaling of DGFET due to good gate control(electrostatic) gives
  * lower doping (even no doping) so no fluctuation in Vt associated with the nonuniformity associated with doping,
  * mitigation of the oxide thickness scaling so better mobility
  * etc.

B-3. Silicon Nanowire transistor

ref. for modeling of nanowire transistor,

Bipul C, et. al., An Analytical Compact Circuit Model for Nanowire FET IEEE TED, VOL. 54, NO. 7, JULY 2007 1637