High-Speed Digital System Design
4190.309
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Traditional demand

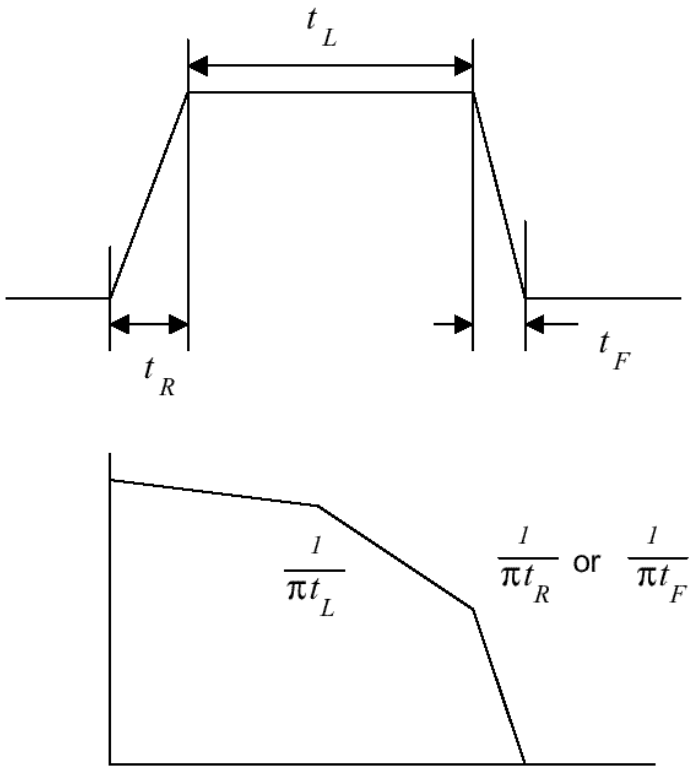
- Speed is one of the most important design factor
  - Hundreds of MHz processors are available
- 2 GHz is high frequency?
- 100 KHz is not so high frequency?
- What about 10 MHz?

High-speed digital systems

- Demand for short propagation delay
  - Fast edge rate is required
  - Results in ringing, reflections, and crosstalk
- Digital systems do not use sine wave!
- Power spectrum of square wave

Frequency of interest

- Knee frequency
- Device speed is important
- Frequency components
  - rise time (t_R)
  - fall time (t_F)
  - pulse width (t_L)
  - Usually t_F is the shortest components



Frequency of interest (contd.)

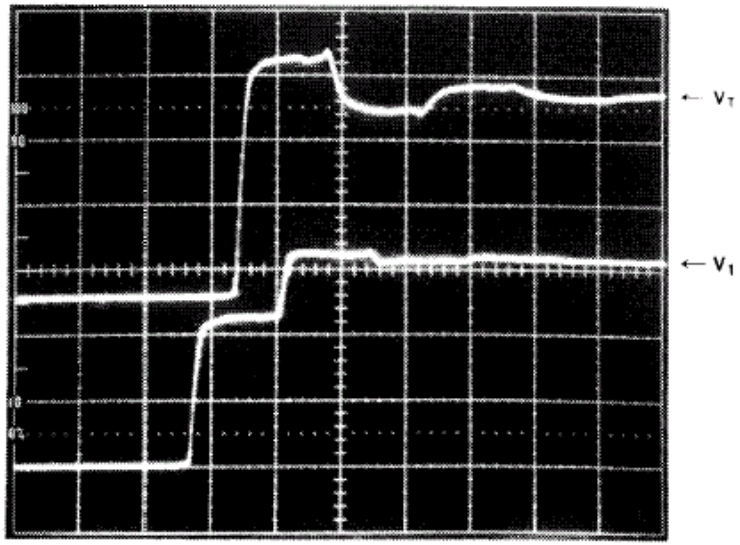
- Example
  - PALCE16V8: t_F = 2 ns
  - f_N =1/(π × 2 ns) = 160 MHz
  - f_N =0.5/(2 ns) = 250 MHz
  - Regardless of the clock frequency

Signal lines as transmission lines

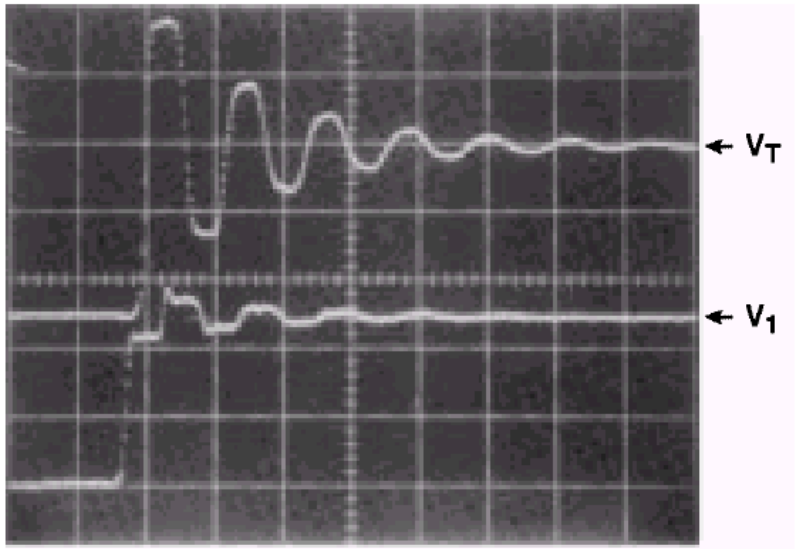
- Return signal's tendency to take the path of the least impedance
- Controlled-impedance lines: constant impedance along the signal line
- Signal delay is greater than a significant portion of the transition time!
  - The signal line must be treated as a transmission line

Signal reflection

- Improperly terminated transmission line is subject to reflections
- Ringing



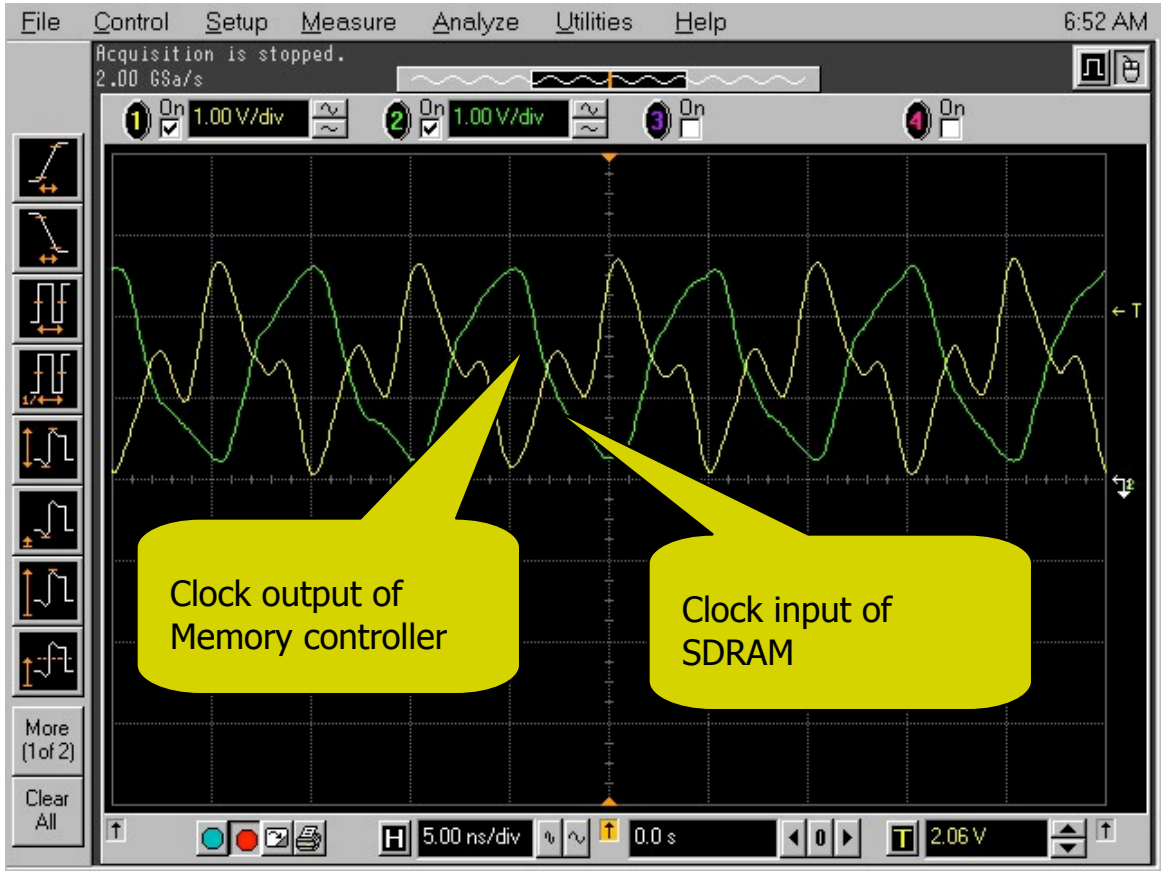
H = 20 ns/div
V = 1.0 V/div



TL/F/12419–7

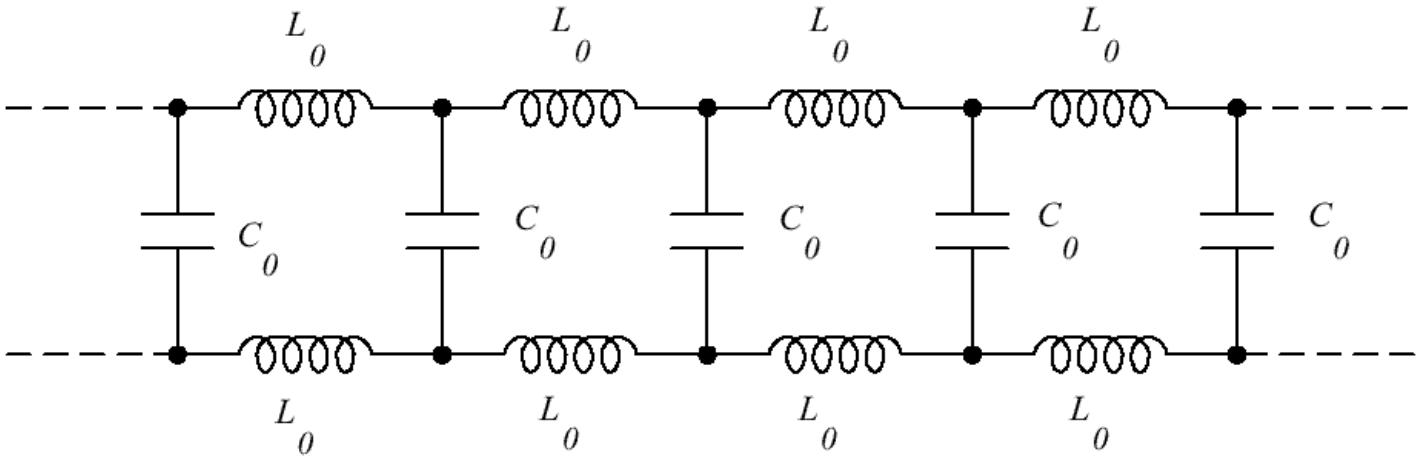
Signal reflection

- SDRAM clock



Controlled impedance line

- Inductance and capacitance are evenly distributed along the length of the line



Controlled impedance line (contd.)

- Characteristics

  - Inductance and capacitance are evenly distributed along the length the line
  - Z_0: AC resistance, unit is Ω

$$Z_0 = \sqrt{\frac{L_0}{C_0}}$$

L_0: Signal line inductance in Henrys per unit length

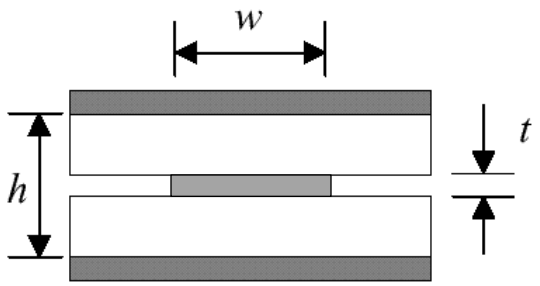
C_0: Signal line capacitance in Farads per unit length

  - t_{PD}: propagation delay

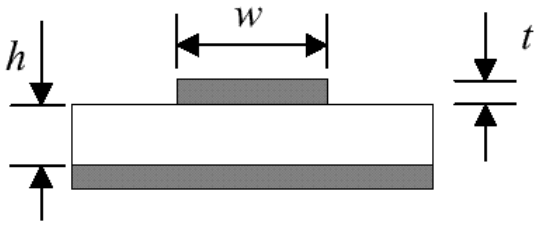
$$t_{PD} = \sqrt{L_0 C_0}$$

Controlled impedance line (contd.)

- Stripline and microstripline



Stripline



Microstripline

Microstripline

- A common material is epoxy-laminated fiberglass, which has an average dielectric constant of 5

$$Z_0 = \frac{87}{\sqrt{\varepsilon_R + 1.41}} ln \frac{5.98h}{0.8w + t} \ \Omega$$

$$t_{PD} = 1.017\sqrt{0.457\varepsilon_R + 0.67} \ ns/ft$$

$$C_0 = 1000\frac{t_{PD}}{Z_0} \ pF/ft$$

$$L_0 = Z_0^2 C_0 \ pH/ft$$

Microstripline (contd.)

- Example
  - Copper thickness is 1 mil
  - Track width is 8 mils (typically 8 to 15 mils)
  - Layer separation is 30 mils

$$Z_0 = \frac{87}{\sqrt{5}+1.41} ln \frac{5.98 \times 0.03}{0.8 \times 0.001 + 0.01} \Omega = 67.05\,\Omega$$

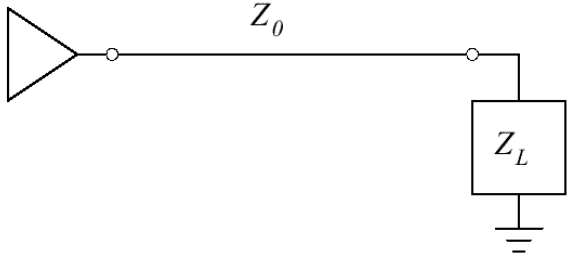
$$t_{PD} = 1.017\sqrt{0.457 \times 5 + 0.67}\, ns/ft = 1.75\, ns/ft$$

$$C_0 = 1000\frac{1.75}{67.05}\, pF/ft = 26.1\, pF/ft$$

$$L_0 = 67.05^2 \times 26.1\, pF/ft = 117\, pH/ft$$

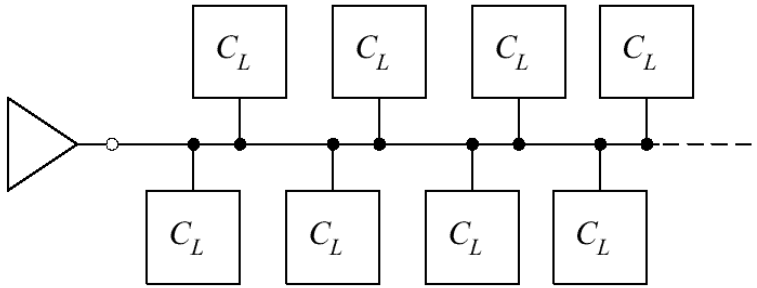
Microstripline (contd.)

- Lumped or distributed load
  - New parameter CL: added capacitance in Farads per unit length
  - DRAM: 4 to 12 pF



$$Z_0 = \frac{Z_0}{\sqrt{1 + \frac{C_L}{C_0}}} \Omega$$

$$t_{PD} = t_{PD}\sqrt{1 + \frac{C_L}{C_0}}\ ns/ft$$



Microstripline (contd.)

- Example
  - Input capacitance is 5 pF, and clearance is 200 mil

$$C_L = \frac{5\,pF}{0.5\,in\frac{1\,ft}{12\,in}} = 120\,pF/ft$$

$$Z_0 = \frac{67.05}{\sqrt{1+\frac{120\,pF/ft}{26.1\,pF/ft}}} = 28.34\,\Omega$$

$$t_{PD} = 1.75\,ns/ft\sqrt{1+\frac{120\,pF/ft}{26.1\,pF/ft}} = 4.14\,ns/ft$$

Reflection

- Maximum transfer of energy
  - The load impedance is equal the source impedance
    - $Z_0 = Z_L$
- The waveform at the load
  - Sum of originally generated signal and the reflection from the load

Reflection (contd.)

- Appearance of the waveform depends on
  - Mismatch of the load
  - Line impedance Z_0
  - The ratio of the signal-transition time, tR to the propagation delay of the line, τ: t_R/τ
- The amount of overshoot usually varies proportionally with the signal-line length until $t_R=\tau$

Reflection (contd.)

- The overshoot is as much as the original transition
- A signal line is considered as a transmission line when $\tau \geq t_R/4$
- More conservative rule is $\tau \geq t_R/8$
- t_R ranges from 1 (0.5) ns to 5 ns
- Think distributed load

Reflection (contd.)

- Example
- t_R (ns), line length (in) with the condition of $\tau = t_R/4$

t_R (ns)	Line length (in)	
	Lumped load	Distributed load
5	8.5	3.6
3	5.1	2.17
2	3.4	1.4
1	1.7	0.75

Reflection (contd.)

- Qualifying reflection
  - $K_R = (Z_L - Z_0) / (Z_L + Z_0)$
  - Open load: $(\infty - Z_0) / (\infty + Z_0) = 1$
  - Short load: $(Z_L - 0) / (Z_L + 0) = -1$

Reflection (contd.)

- Example: CMOS GAL PALCE16V8 and micropipeline
  - Z_0 ranges from 30 to 150 Ω
  - Input impedances range from 10 K to 100 KΩ
  - Driver's output impedance

  - Since input impedance 100K Ω, K_R at load = 1

$$Z_S = \frac{V_{OL}}{I_{OL}} = \frac{0.2\,V}{24\,mA} = 8.3\,\Omega$$

Reflection (contd.)

- Since Z_0 = 67 Ω, K_R at source:

$$K_R = \frac{8.3 - 67}{8.3 + 67} = -0.78$$

- Driver generates 3.5 V ⇒ 0.2 V

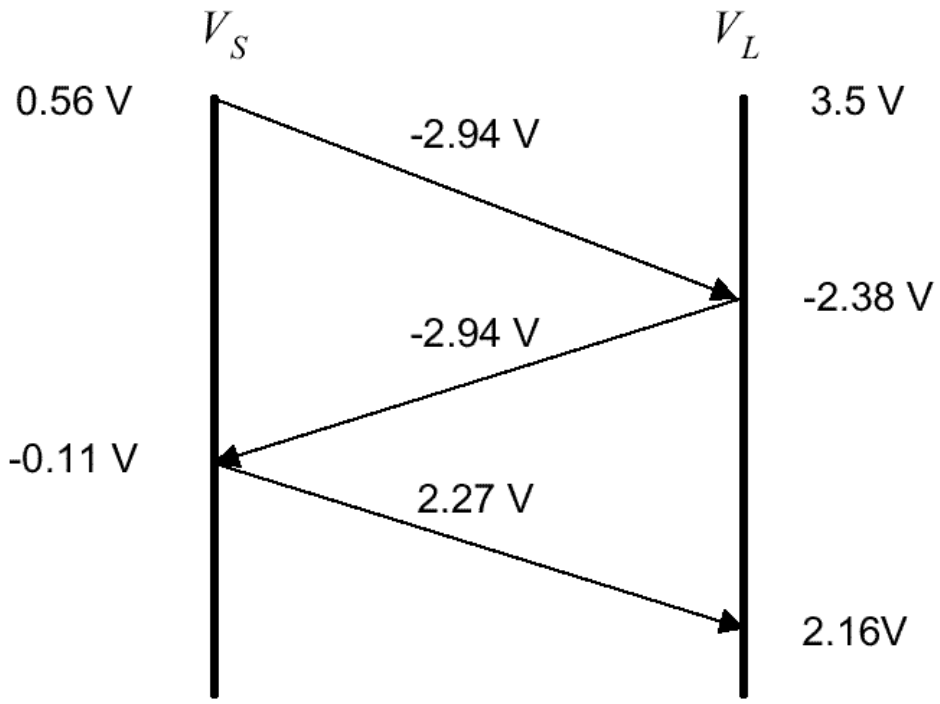
$$\Delta_V = \frac{(0.2\,V - 3.5\,V)Z_0}{Z0 + Z_s} = \frac{-3.3\,V \times 67\,\Omega}{67\,\Omega + 8.3\,\Omega} = -2.94\,V$$

- Resultant signal, V_S:

$$V_S = 3.5\,V + \Delta_V = 0.56V$$

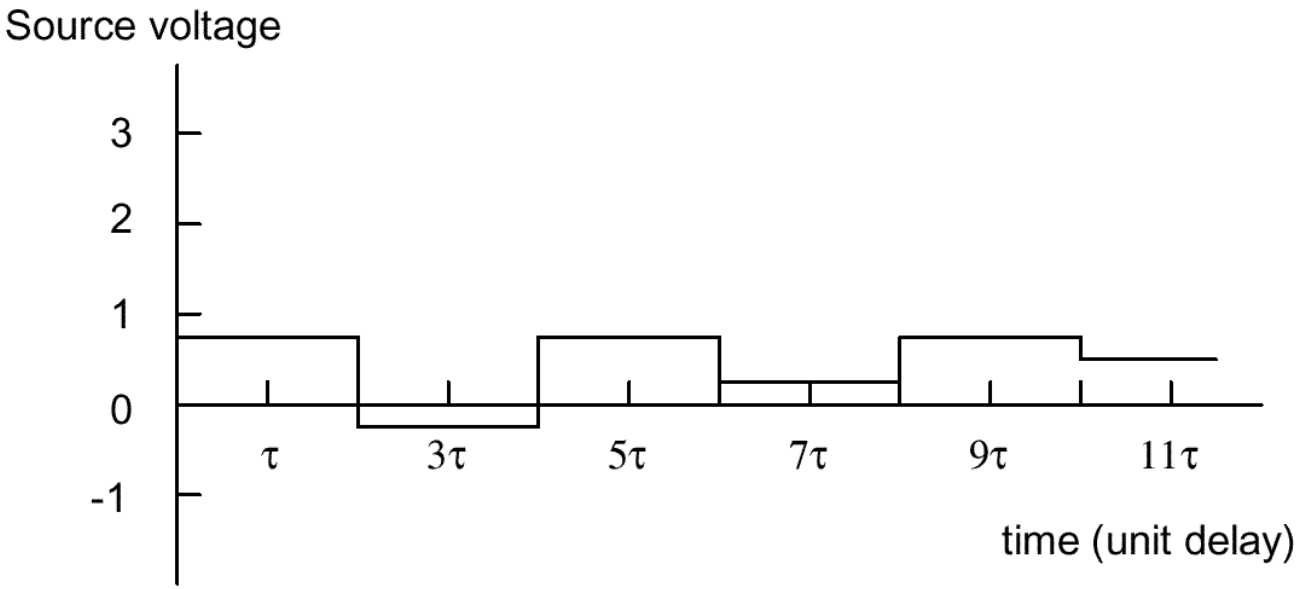
Reflection (contd.)

- Lattice diagram with superposition theory



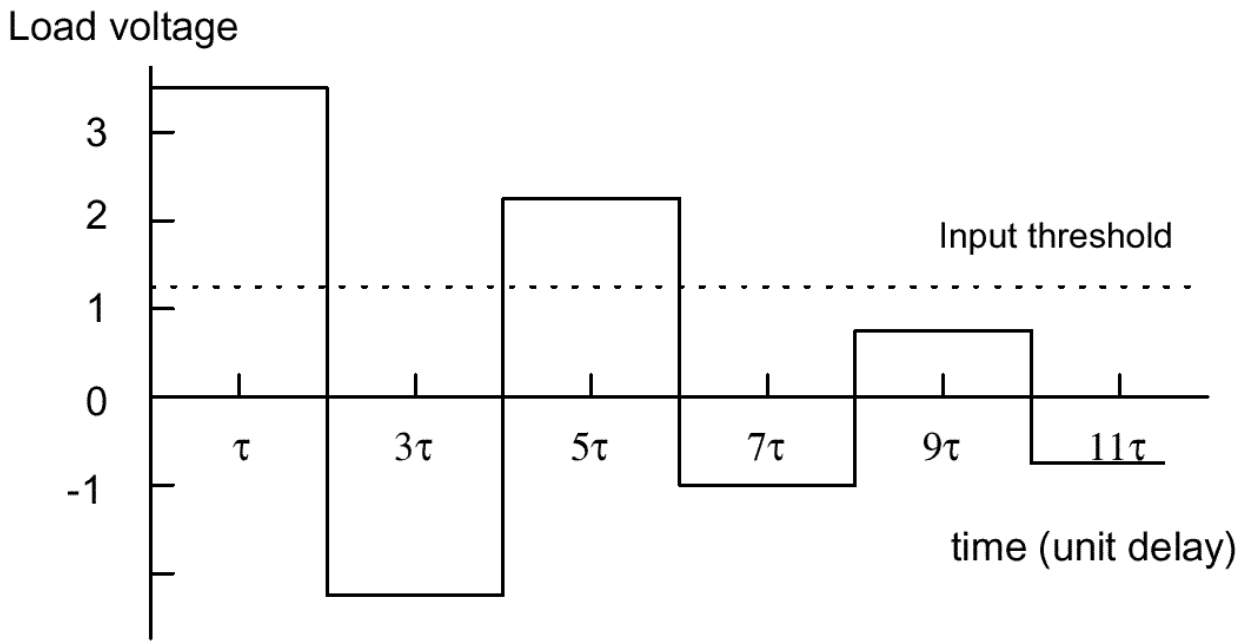
Reflection (contd.)

- Settling time and delay: source voltage



Reflection (contd.)

- Settling time and delay: source voltage



Termination

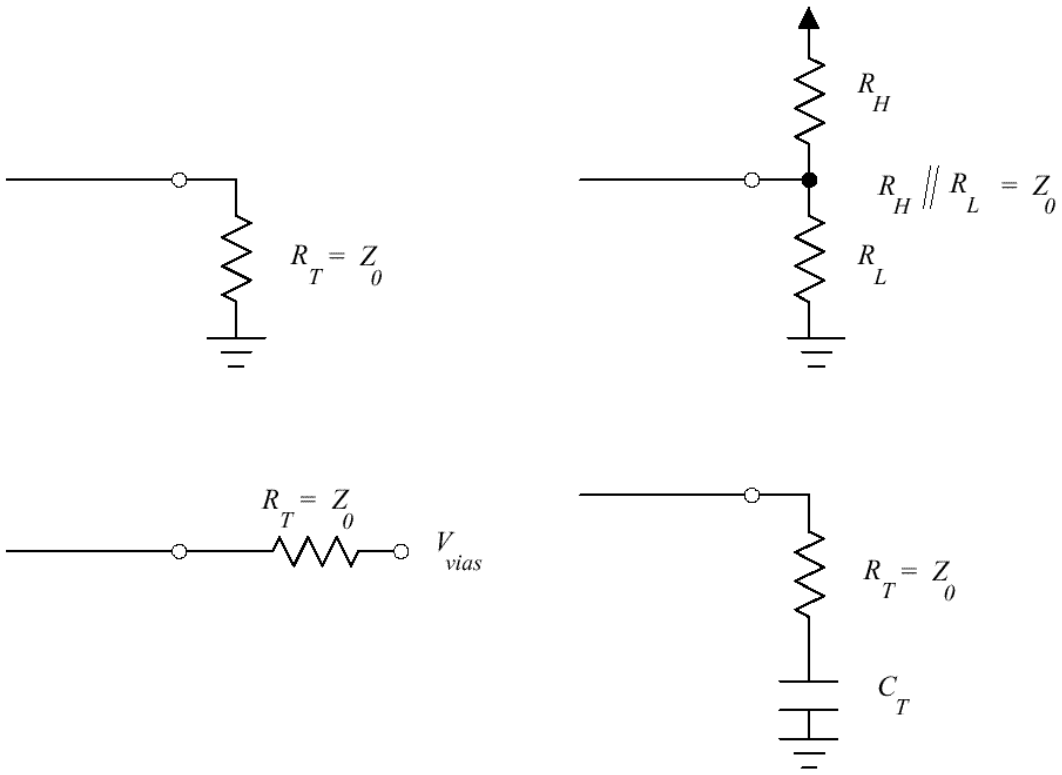
- Reflections are eliminated when $Z_L = Z_0$
- How to make $Z_L = Z_0$?
  - Reduce Z_L to Z_0 : eliminate the first reflection
    - Placing parallel register with the load current drain is high for the HIGH-output state
    - Terminating to Vcc helps since I_{OL} is usually high than I_{OH}, but normally not enough
    - Termination to a DC reference voltage: 50 register to 3 V reference

Termination (contd.)

- DC voltage is AC ground but difficult to find DC reference that can switch from sinking current to sourcing current fast
- Enough to respond to the transition.
- RC-series termination: AC termination

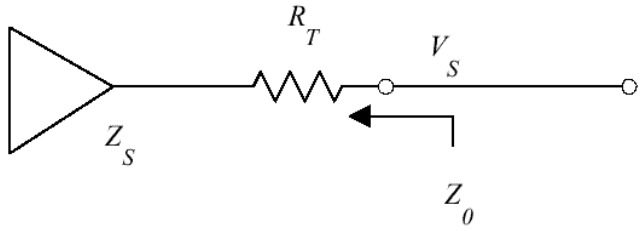
Termination (contd.)

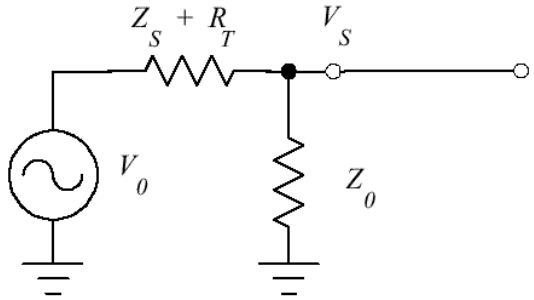
- Source termination methods: $Z_L = Z_0$



Termination (contd.)

- How to make $Z_S = Z_0$?
  - Increase Z_S to Z_0 : eliminate the second reflection
    - placing a series register with the source: best for a lumped load



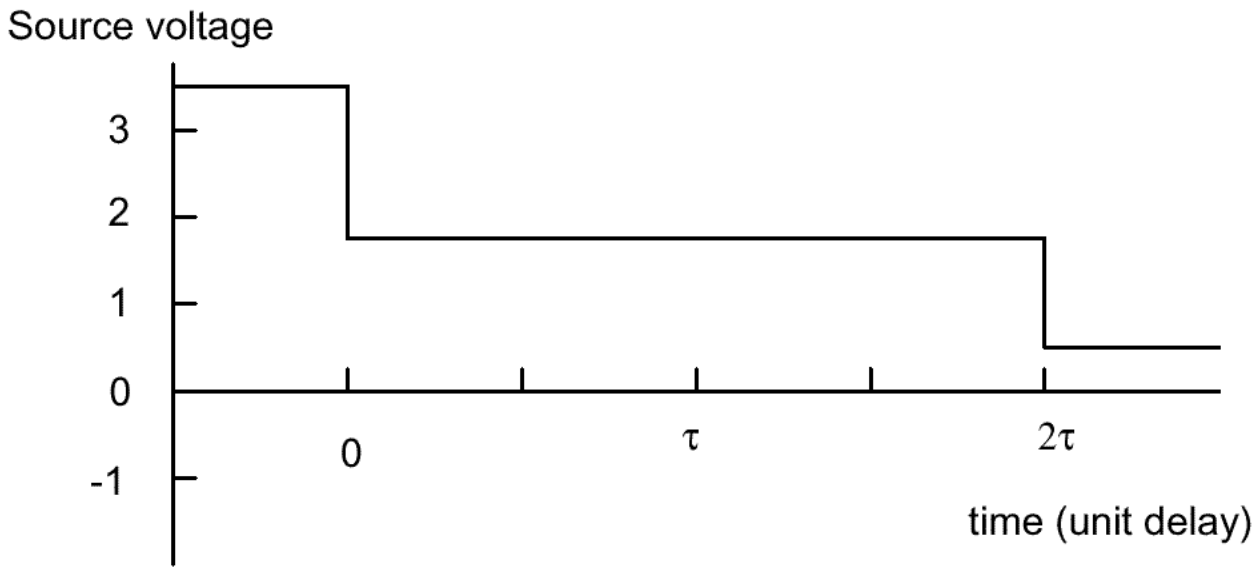


Termination (contd.)

- Since the load is open, ΔV reflects from the load to the source
- There is no second reflection
- Risky approach for a distributed load because of the intermediate voltage
- The device close to the driver has a valid input after a return trip. However, it is popular for a DRAM array

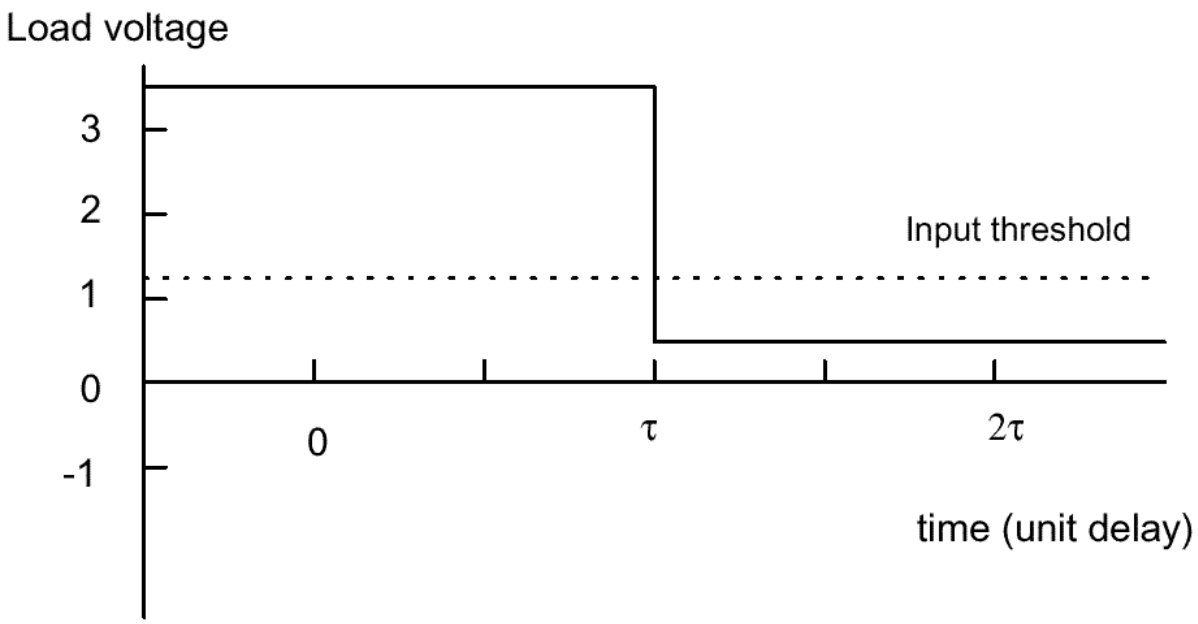
Termination (contd.)

- Settling time and delay: source voltage



Termination (contd.)

- Settling time and delay: load voltage

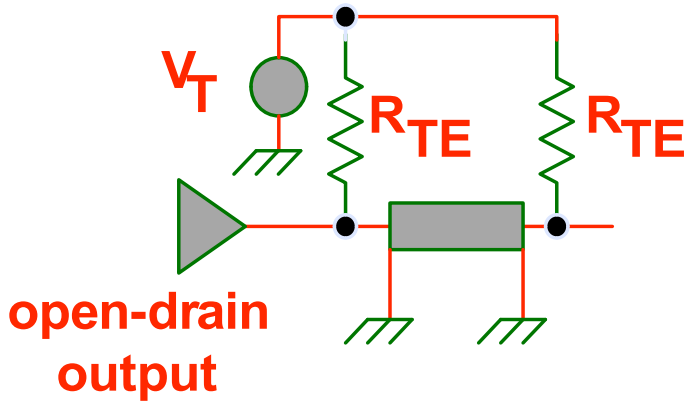


Termination (contd.)

- Choose R_T such that $R_T + Z_S < Z_0$
  - reduce the additional delay by making the intermediate voltage below the threshold level
  - This is not an exact match, thus inducing ringing, but tolerable
  - Generally, exact match is difficult, because HIGH-impedance and LOW-impedance are different: for PALCE16V8, 50 Ω and 8 Ω, respectively

Termination (contd.)

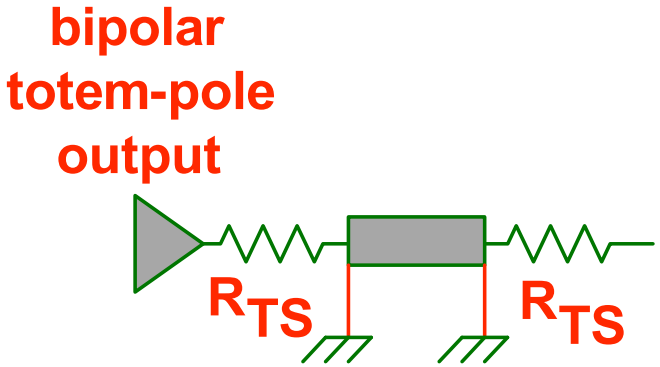
- GTL+



  - processors to memory controllers
  - Intel Pentium™ processor
  - 3.3V supply
  - open-drain output end-terminated to 1.5V
  - CMOS and BiCMOS versions

Termination (contd.)

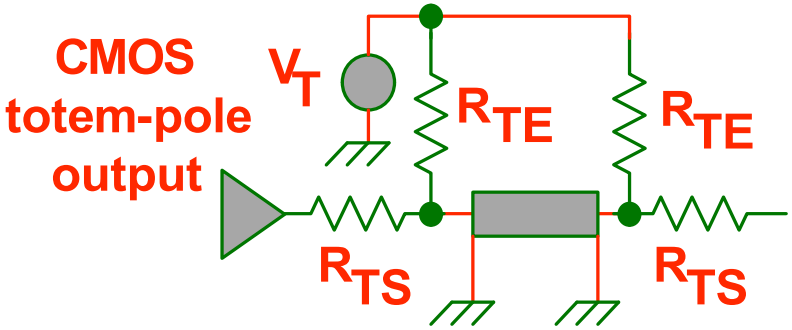
- LVT (ABT)



  - general purpose interconnection
  - TTL (ABT) or low-voltage TTL (LVT) compatible
  - BiCMOS technology
  - bipolar totem-pole output

Termination (contd.)

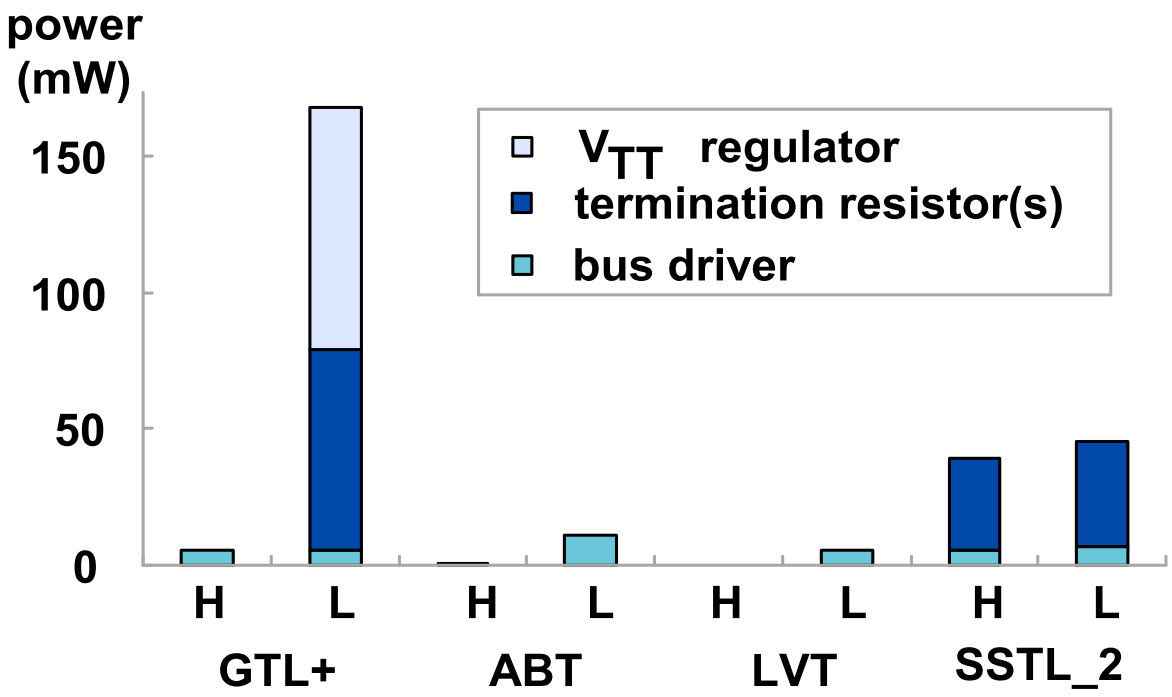
- SSTL_2



  - memory controllers to DDR SDRAM arrays
  - 2.5V CMOS totem-pole terminated to 1.25V
  - CMOS technology
  - CMOS totem-pole

Power consumption model

- Static power consumption



Layout rules for transmission lines

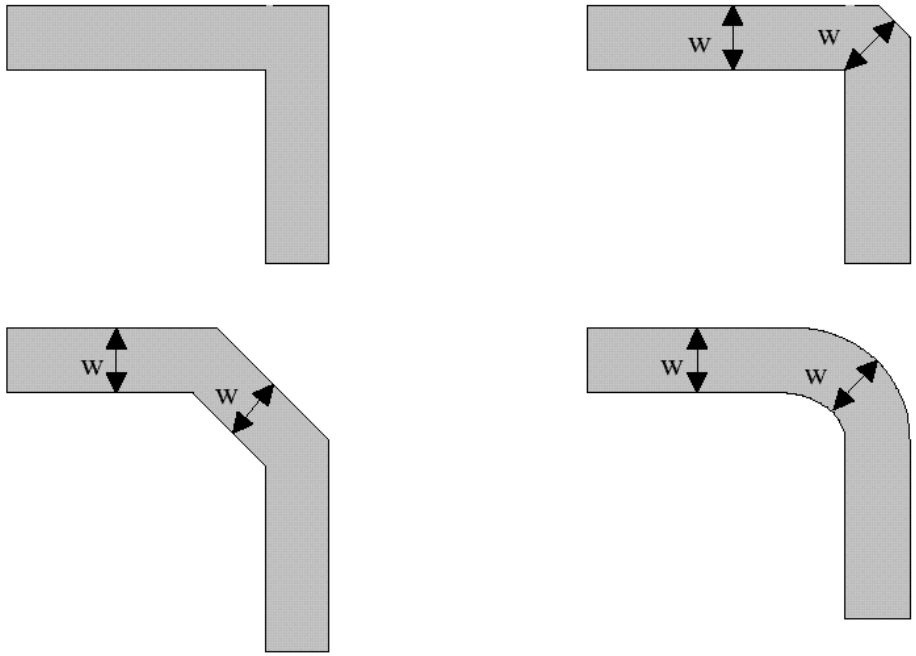
- Do not make discontinuity
  - Discontinuities are points where the impedance of the signal line changes abruptly
  - The formula of KR is valid as well for the discontinuities
  - Avoid bend of tracks and vias
  - Smoothing the bends
  - Reduce excessive vias

Layout rules for transmission lines (contd.)

- Do not use stubs or Ts
  - Stub or Ts can be noise sources
  - Terminate individually long stubs
  - Do not make stubs

Layout rules for transmission lines (contd.)

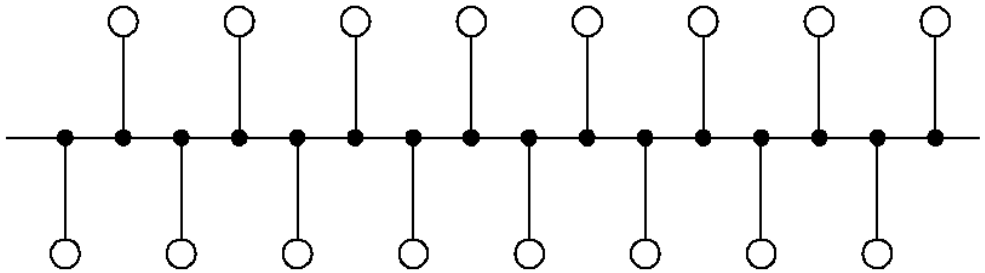
- Soothing the bends

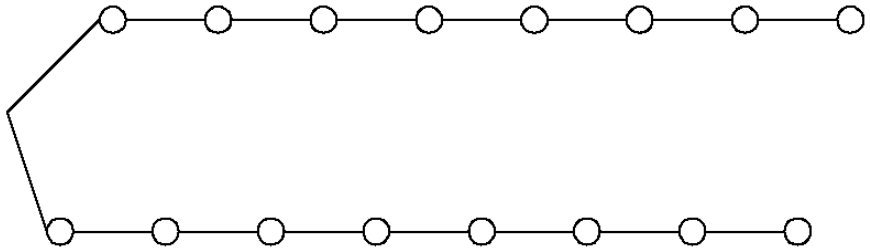


Layout rules for transmission lines (contd.)

- Stub off of a transmission line

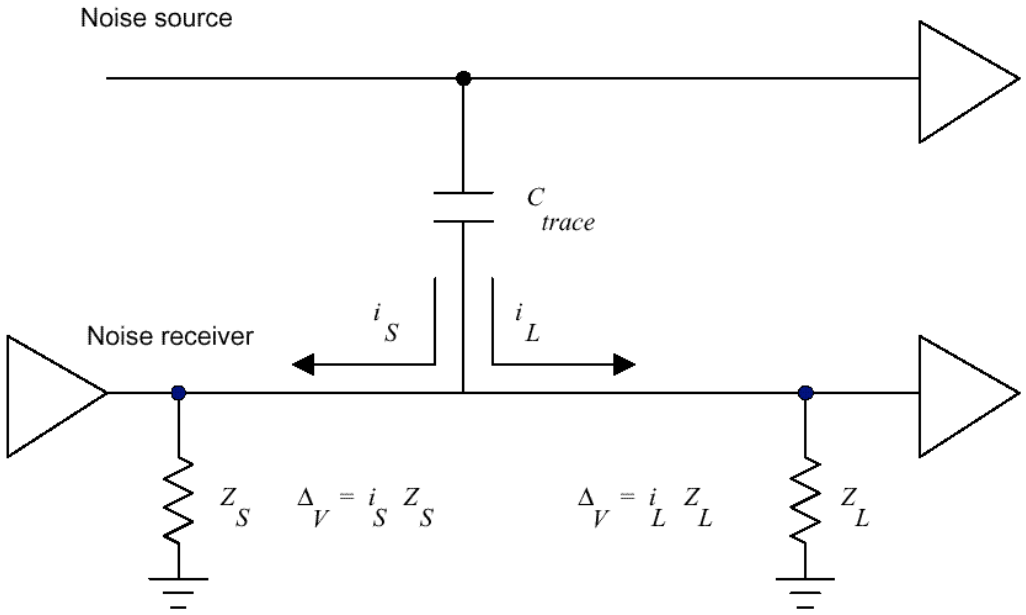
- Correctic





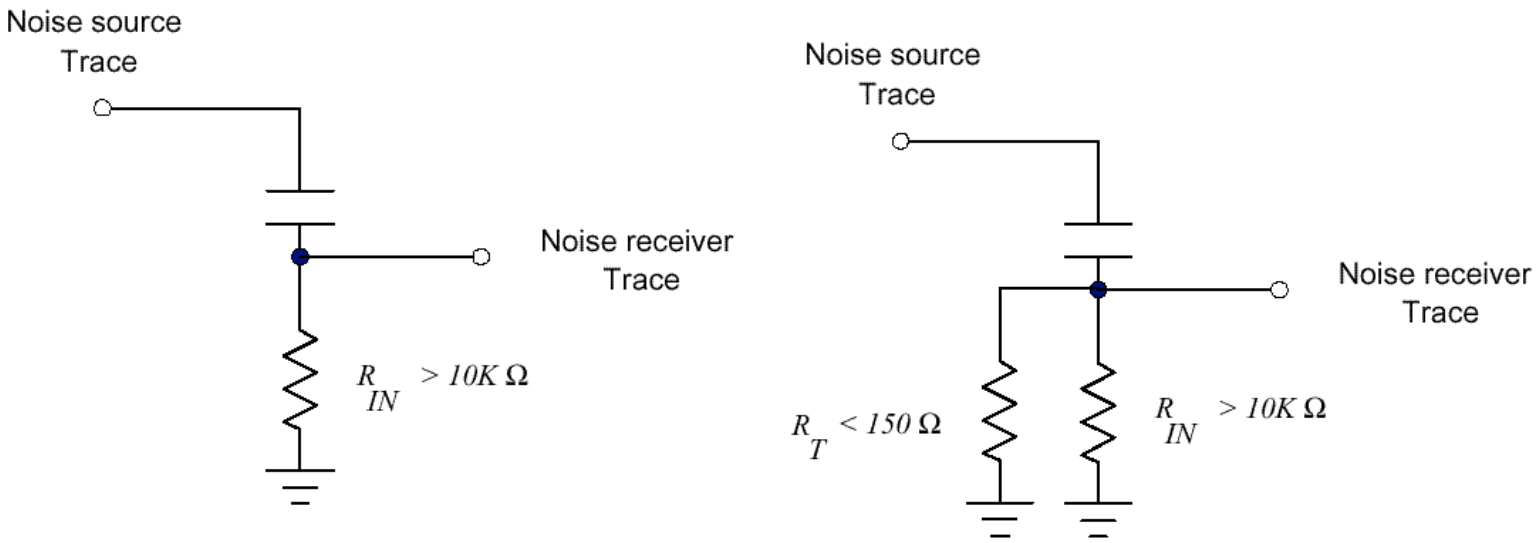
Capacitive crosstalk

- Capacitive coupling induced by closely located lines
  - Current injection to a transmission line



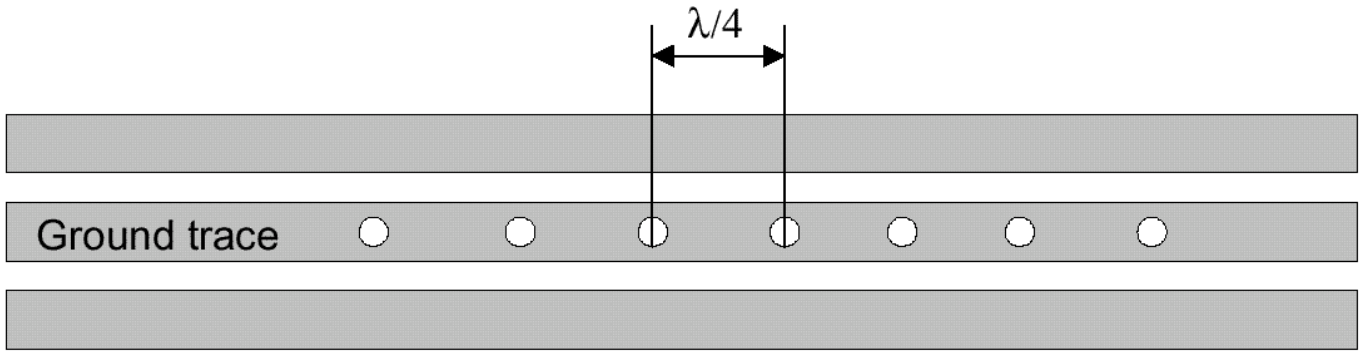
Capacitive Crosstalk (contd.)

- Termination reduces the noise



Capacitive Crosstalk (contd.)

- Separation helps to reduce the crosstalk
- Isolation: put a ground trace between the coupled traces should be a solid ground



Capacitive Crosstalk (contd.)

- Example
  - wavelength
  - max. frequency of interest
  - distance

$$\lambda = \text{velocity} \times \text{period} = \frac{1}{t_{PD}} \frac{1}{\text{freq}}$$

$$\frac{1}{\pi t_R} \qquad f_{MAX} = \frac{1}{1.25\ ns \times \pi} = 255\ MHz$$

$$\lambda = \frac{1}{255\ MHz} \frac{1}{4.14\ ns/ft} \frac{12\ in}{ft} = 11.4\ in$$

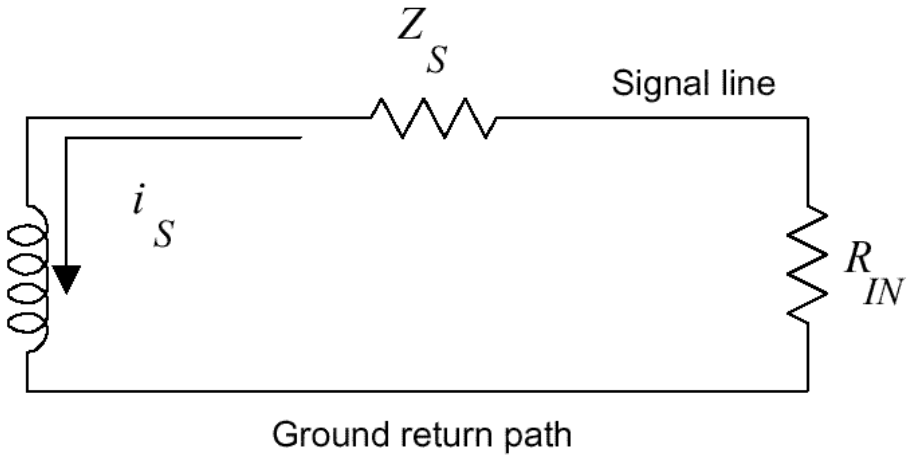
$$\lambda/4 = \frac{11.4\ in}{4} = 2.8\ in$$

Inductive crosstalk

- Coupling of signals between the primary and secondary coils
  - Natural loops by signals and their return paths
  - Artificial loops
  - Amount of the coupled signal depends on
    - size of the loops and their proximity
  - The size of the signal at the load, increases with the load impedance

Inductive crosstalk (contd.)

- Series inductive loop



Inductive crosstalk (contd.)

- Solution
  - Artificial loop: open it
  - Natural Loop: Keeping the load impedance low
  - RT is usually 30 Ω to 150 Ω; this reduce the voltage at least two orders of magnitude

Summary of crosstalk

- Both capacitive and inductive crosstalk increase with load impedance
  - should be terminated
- Keeping the signal separated reduces capacitive coupling
- Capacitive coupling can be reduced by isolation with ground trace

Summary of crosstalk (contd.)

- Inductive crosstalk can be reduced by minimizing loop size
- Inductive crosstalk is induced by shared common path