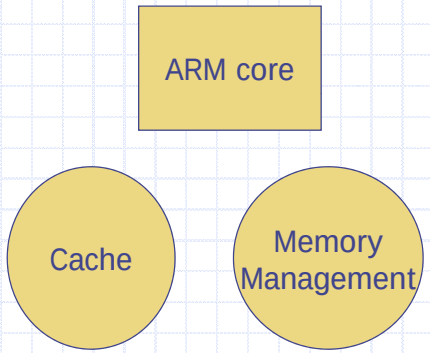
ARM Memory Management Units

ARM Processor Organization



MPU & MMU

- MPU == hardware protection over software-designated regions
- MMU == hardware protection + virtual memory support
- E.g., ARM920T vs. ARM940T

MMU Overview

- Support for private memory space for each task
  - Virtual memory system
  - Address relocation

Virtual to Physical Mapping

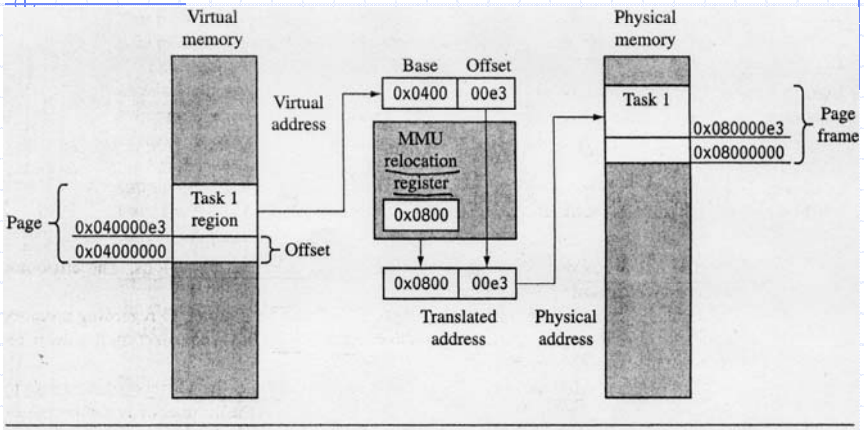


Figure 14.1 Mapping a task in virtual memory to physical memory using a relocation register.

TLB

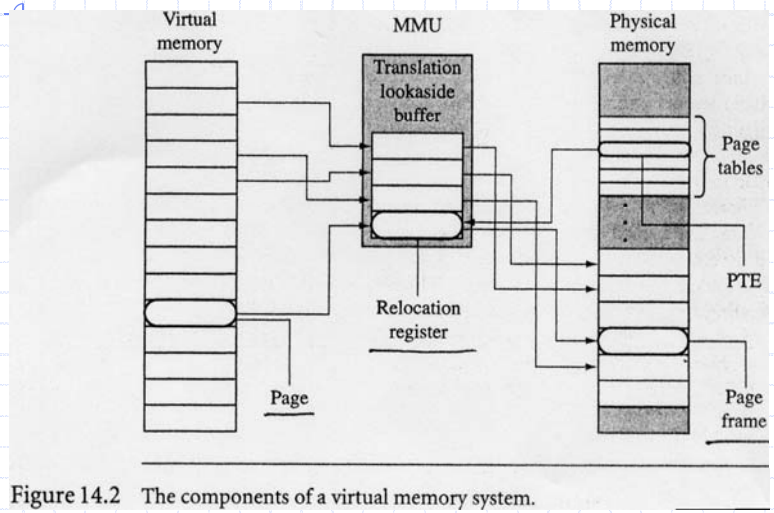


Figure 14.2 The components of a virtual memory system.

Regions

- Sequential set of page table entries (S/W)
  - c.f., H/W components in MPU
- Most page tables represent 1 MB areas of virtual memory

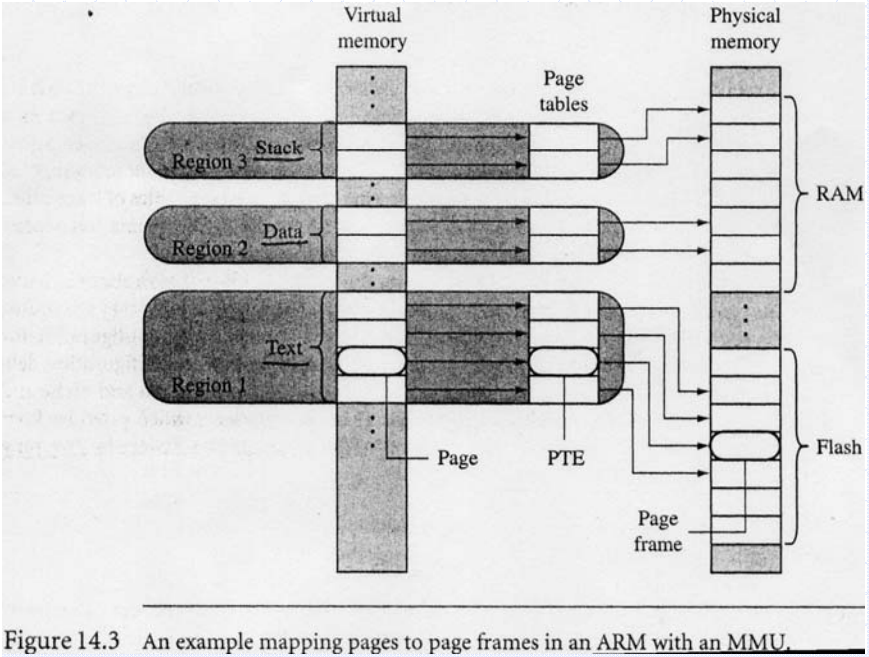


Figure 14.3 An example mapping pages to page frames in an ARM with an MMU.

Multitasking under MMU

- For context switch:
  1. Save the active task context & put it in a dormant state
  2. Flush caches & TLB
  3. Configure MMU to use new page tables
  4. Restore the context of new task
  5. Resume the execution
- Why flush caches?

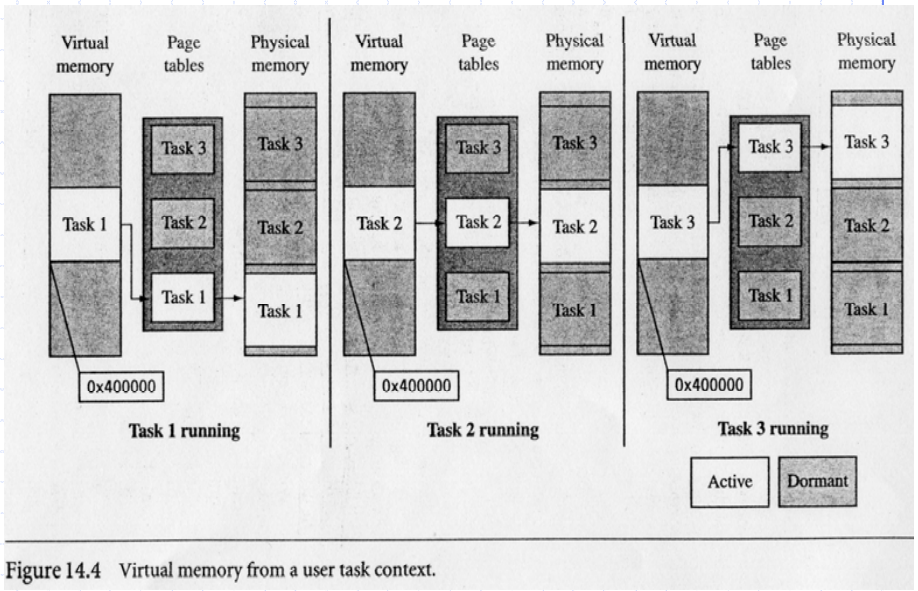


Figure 14.4 Virtual memory from a user task context.

Three tasks with the same virtual addresses

General Memory Organization

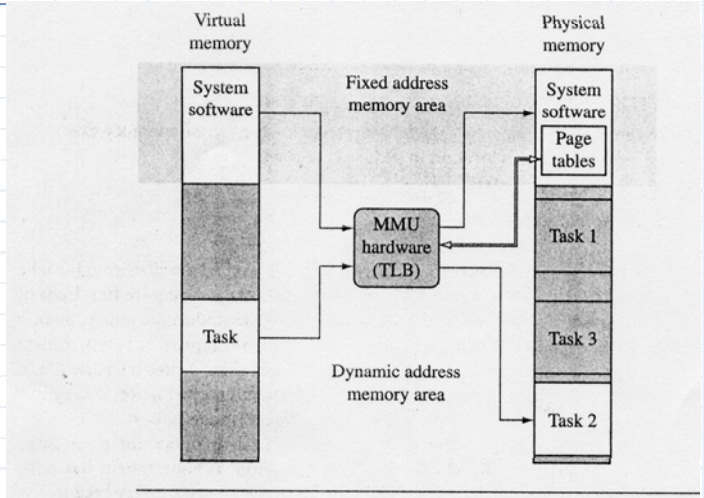


Figure 14.5 . A general view of memory organization in a system using an MMU.

MMU Functions

- Virtual to physical translation
- Memory access permission
- Cache & WB configuration for each page
- Generate abort exceptions for
  - Translation, permission, domain faults

ARM MMU Overview

- Two levels of page tables:
  - L1 page table
  - L2 page table
- L1 page table divides 4 GB address space into 1 MB sections:
  - 4096 entries

L1 Page Tables

- L1 master page table (base addr: CP15:c2)
  - Types 1 & 2: Base address of L2 page tables
    - Fine L2 page table
    - Coarse L2 page table
  - Type 3: Page table entry for 1 MB section
  - Type 4: Fault entry (will generate an abort exception)

L1 PTEs

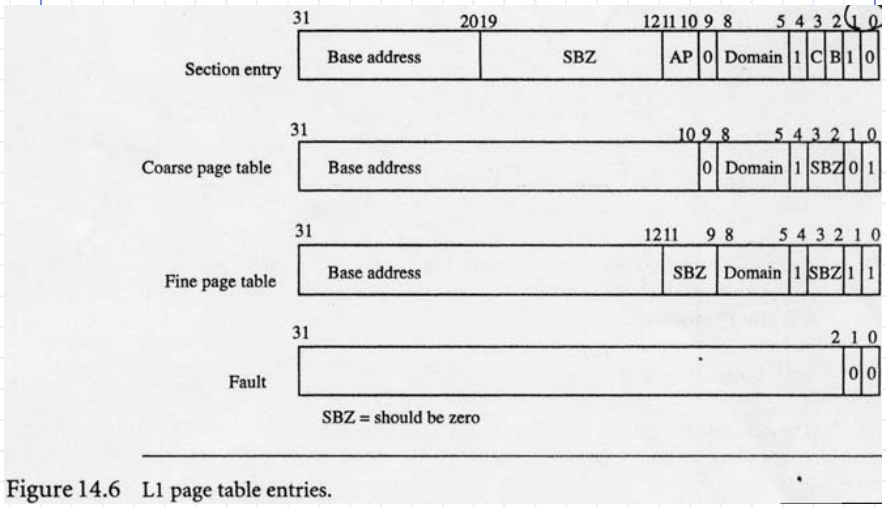


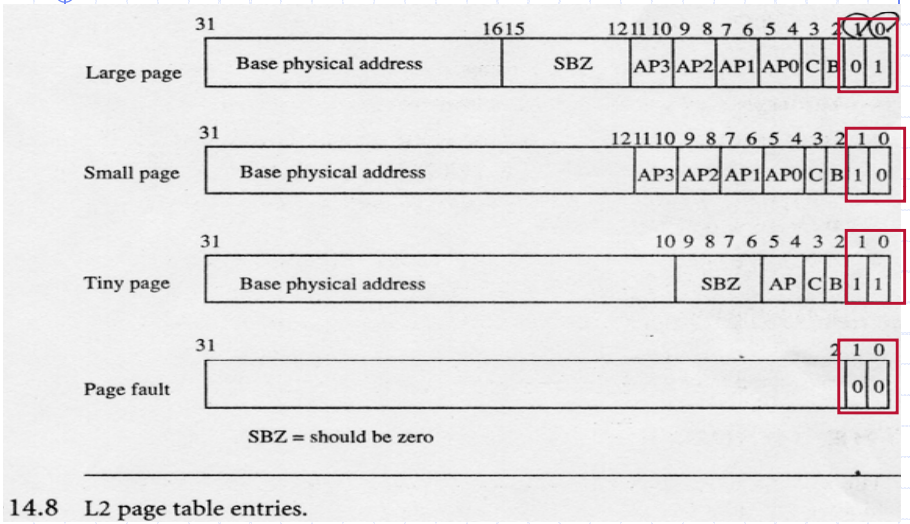
Figure 14.6 L1 page table entries.

L2 Page Tables

- Large page (64 KB)
- Small page (4 KB)
- Tiny page (1KB)
- Fault page entry

L2 PTEs

APs for four subpages



14.8 L2 page table entries.

Single-Step Page Table Walk

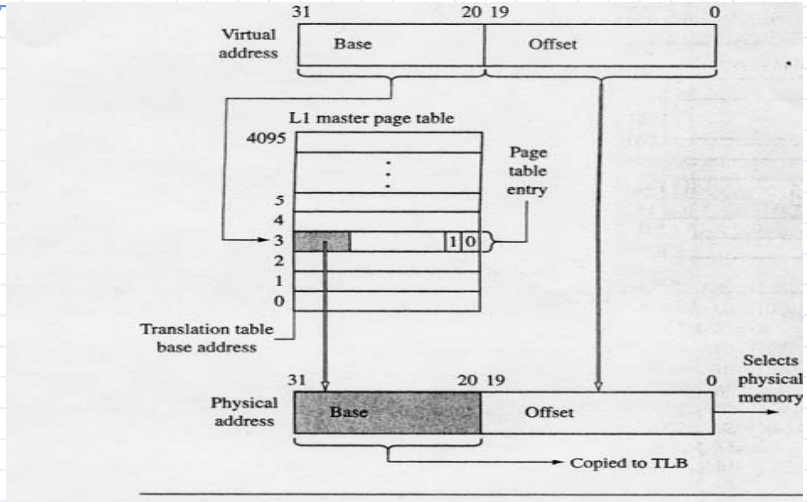


Figure 14.9 L1 Page table virtual-to-physical memory translation using 1 MB sections.

Two-Step Page Table Walk

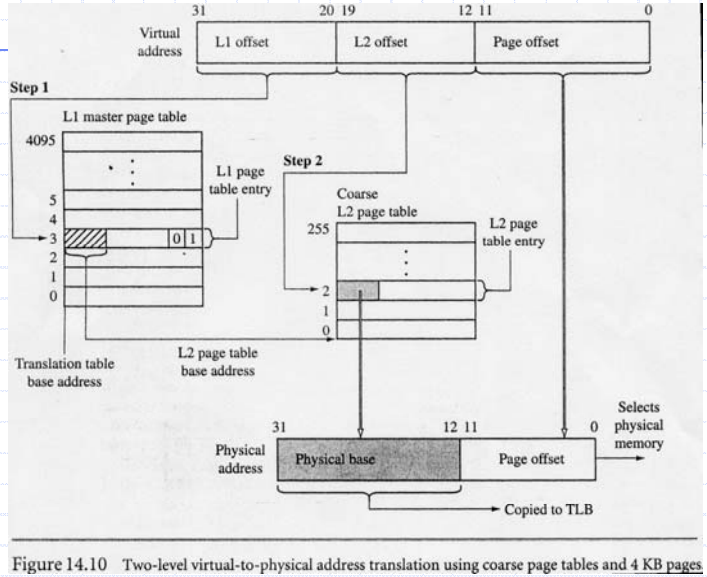


Figure 14.10 Two-level virtual-to-physical address translation using coarse page tables and 4 KB pages.

Domains

- 16 different domains
  - Assigned to a section by setting the domain field in L1 PTE

Value	Status	Description
00	No access	Any access will generate a domain fault
01	Client	Page and section permission bits are checked
10	Reserved	Do not use
11	Manager	Page and section permission bits are not checked

Fast Context Switch Extension

- Avoid cache & TBL flushes during context switch
  - Virtual Address (VA)
  - Modified Virtual Address (MVA)
- MVA = VA + (0x2000000 * process ID)

CP15 register 13

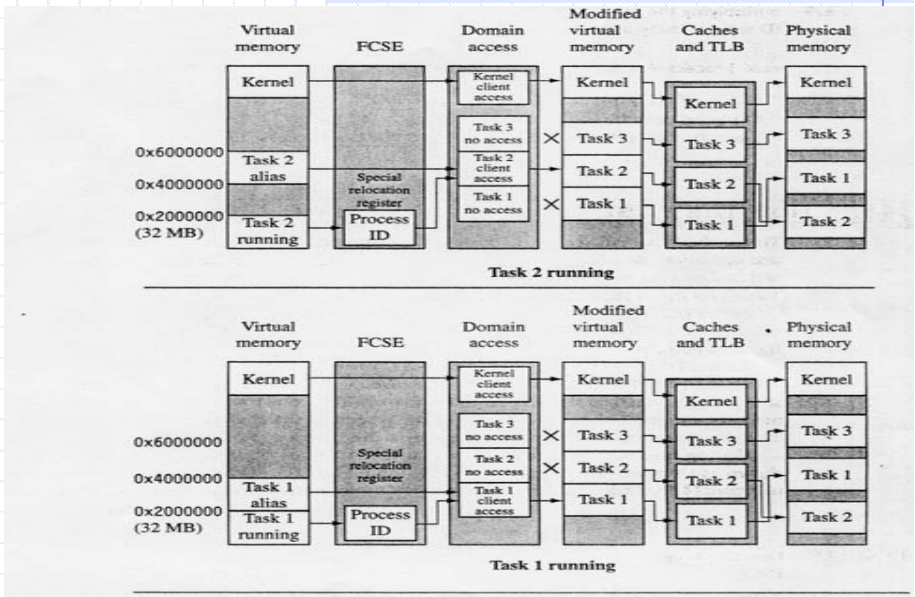


Figure 14.14 Fast Context Switch Extension example showing task 1 before a context switch and task 2 running after a context switch in a three-task multitasking environment.