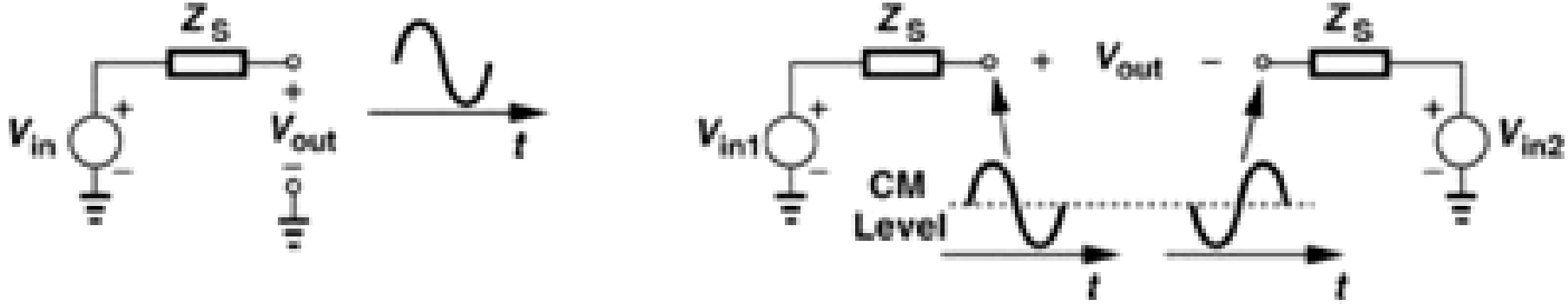
Chapter 4
Differential Amplifiers

CMOS Differential Amplifiers

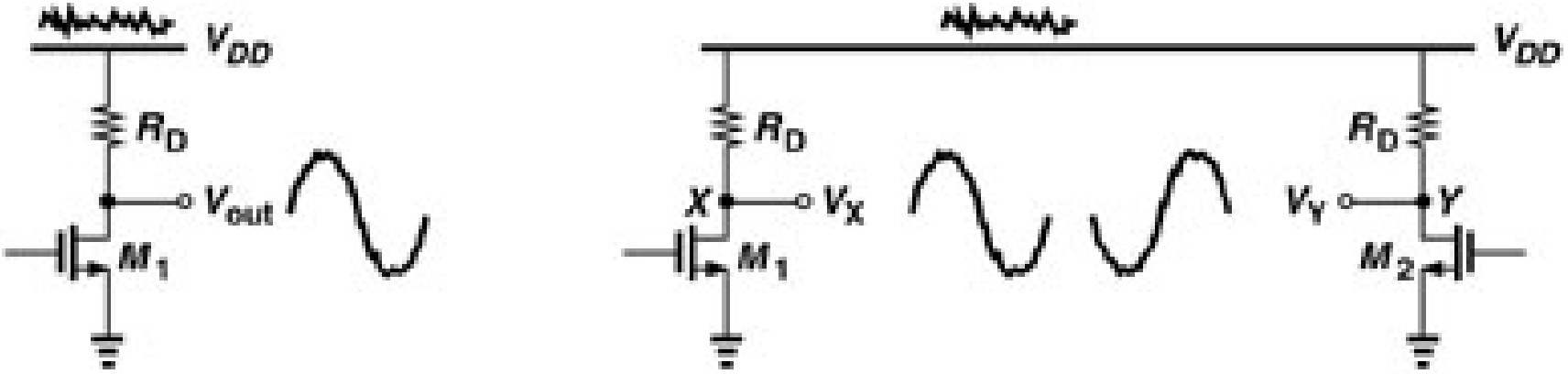
Basic Concepts-L15

Single-ended vs. Differential Signals



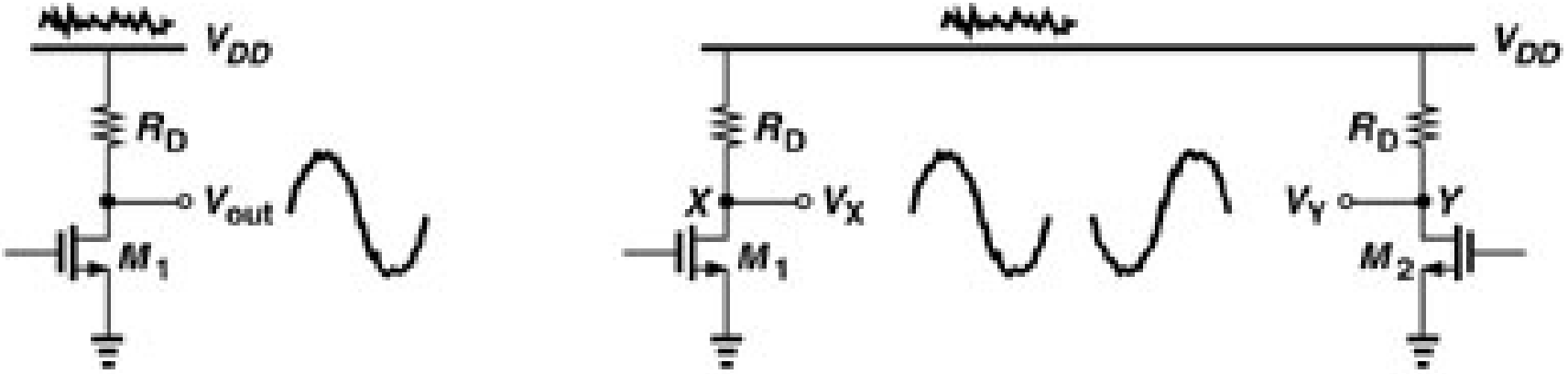
- Single-ended signal: Measured with respect to a fixed potential, typically ground.
- Differential signal: Measured between two symmetric nodes (nodes have equal and opposite signal excursions around a fixed potential, called a “common-mode” level)

Why Differential?



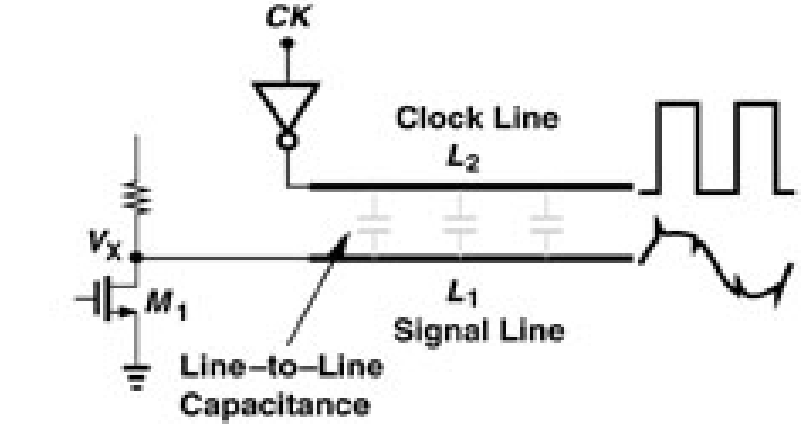
- In a single amplifier V_{DD} fluctuations appear directly on the amplified signal.
- In a differential pair, if we measure V_X-V_Y the fluctuations cancel out.

Why Differential?



- In a single CS amplifier, the maximum swing is V_{DD}-(V_{GS}-V_{TH})
- In a differential pair it can be shown that the swing of V_X-V_Y can reach 2[V_{DD}-(V_{GS}-V_{TH})].

Clock Noise Reduction



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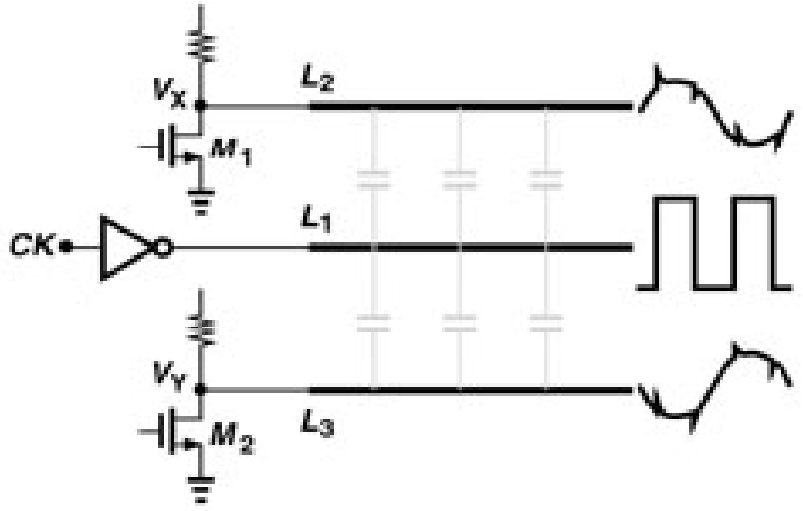
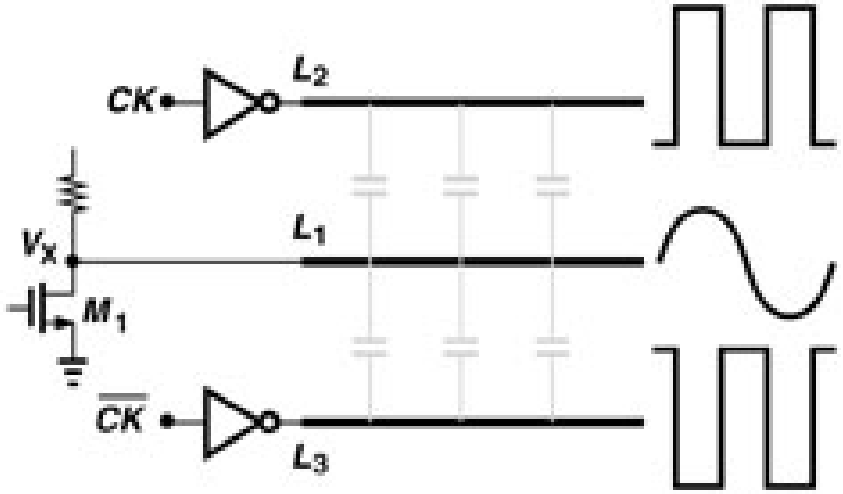




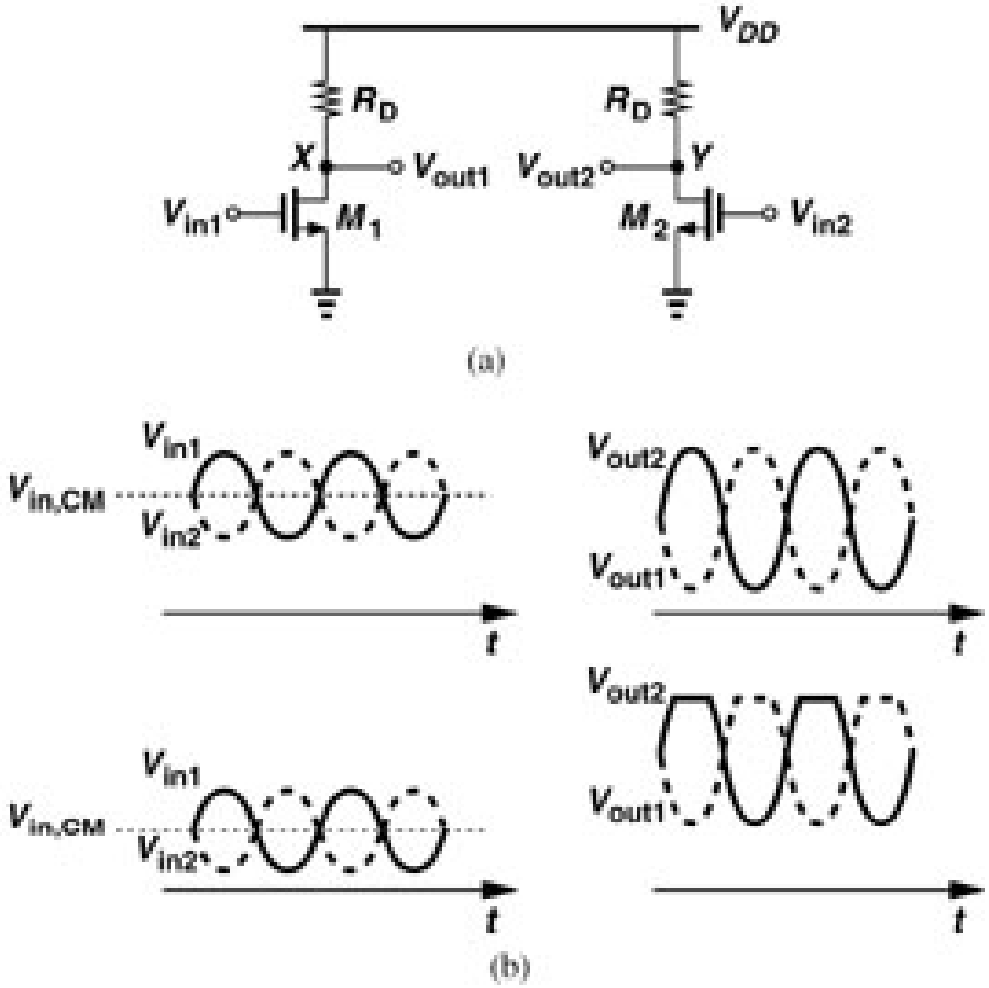
Other advantages of differential amplifying

- Simpler biasing
- Higher linearity

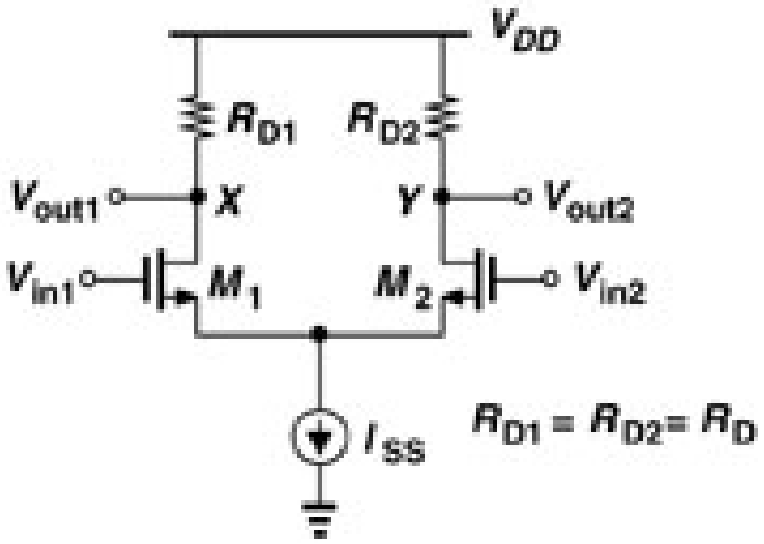
Simple Symmetric Differential Pair won't do!

Good features: Rejection of VDD fluctuations, Larger swing.

Key problem: Input signal common-mode affects bias conditions, and differential amplification.



Solution: Source-coupled (“long-tailed”) Pair, biasing with a current source



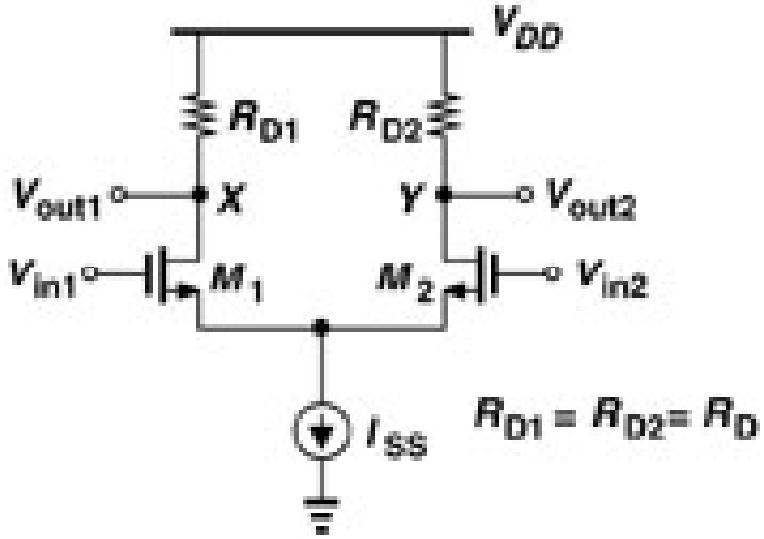
If $V_{in1}=V_{in2}$ then $I_{D1}=I_{D2}=I_{SS}/2$

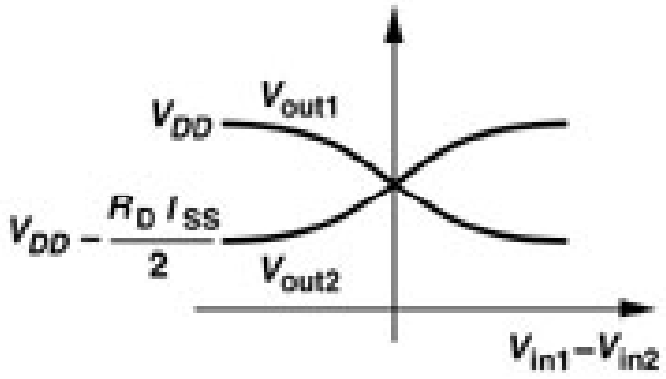
Then $V_{out1}=V_{out2}=V_{DD}-R_DI_{SS}/2$

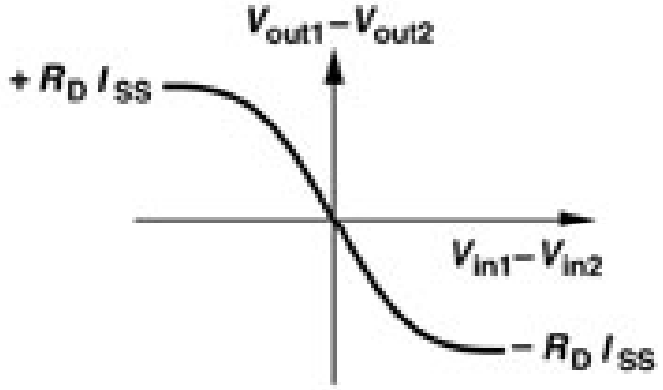
“Current stealing “ phenomenon

If $V_{in1}>>V_{in2}$, then M_2 turns off and M_1 steals all the current.

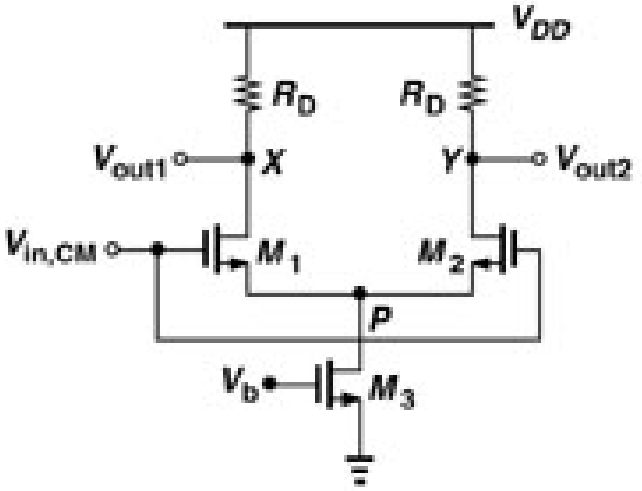
If $V_{in1}<<V_{in2}$ then M_2 takes all the current.







Common-Mode Response



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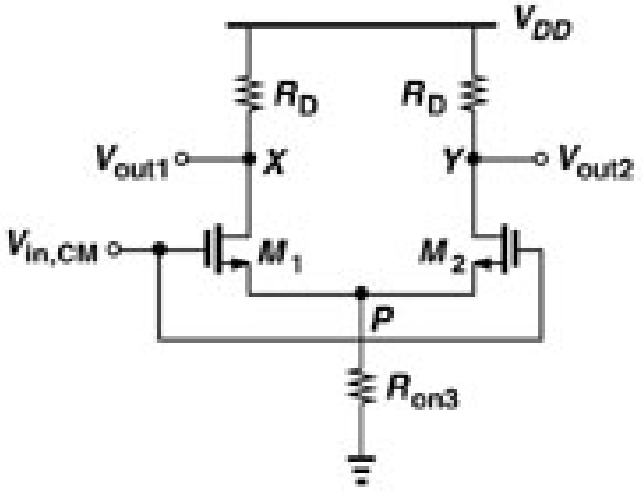

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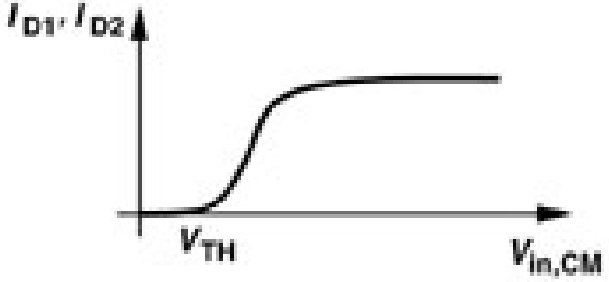
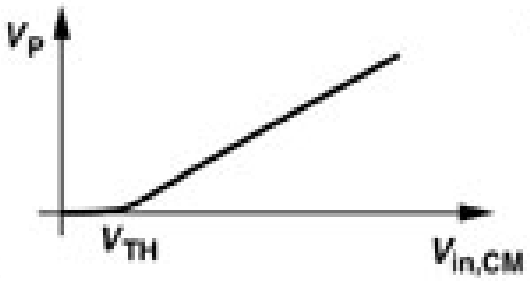
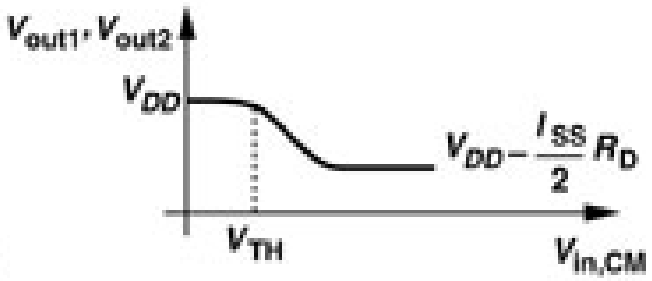
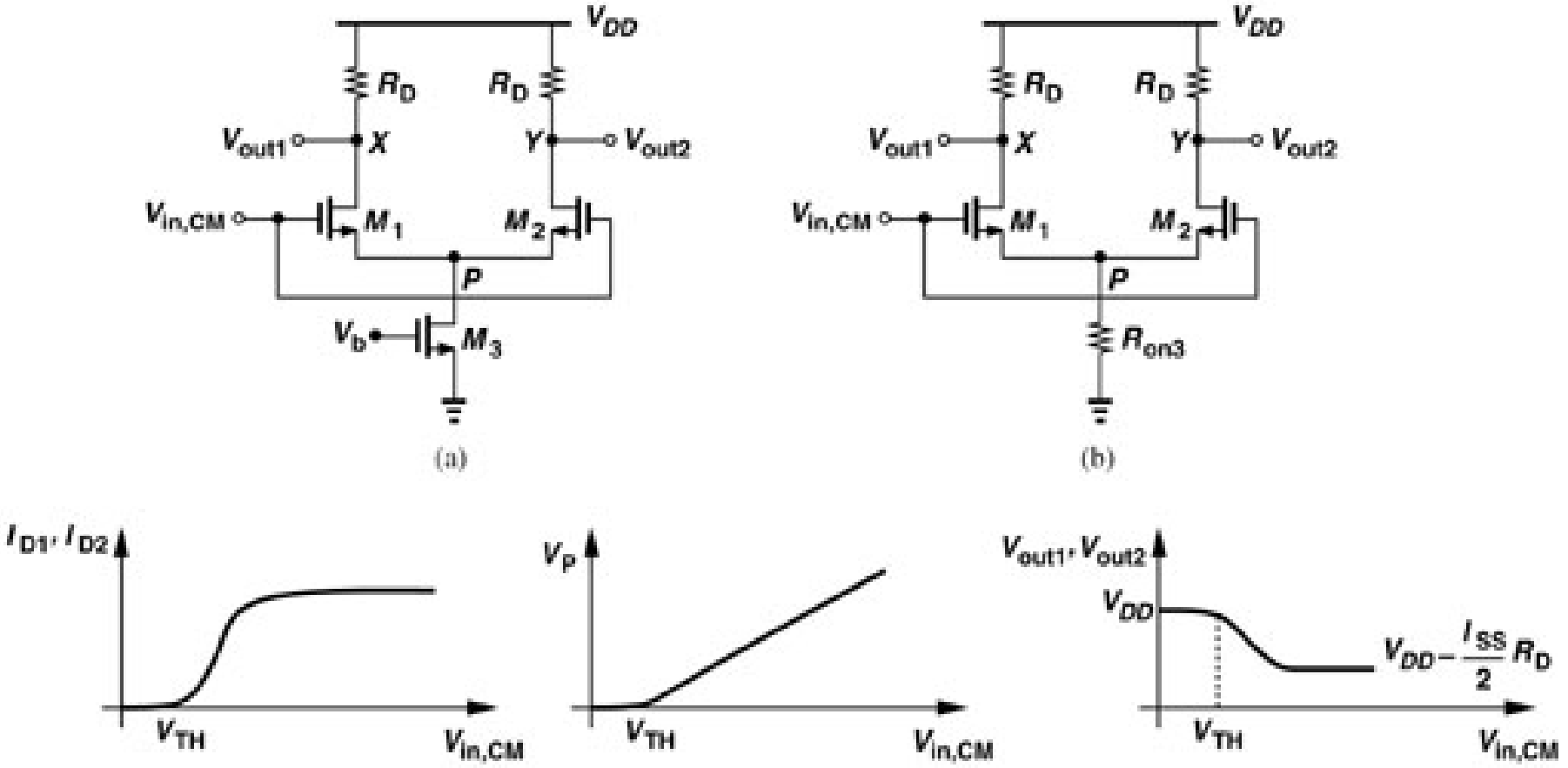






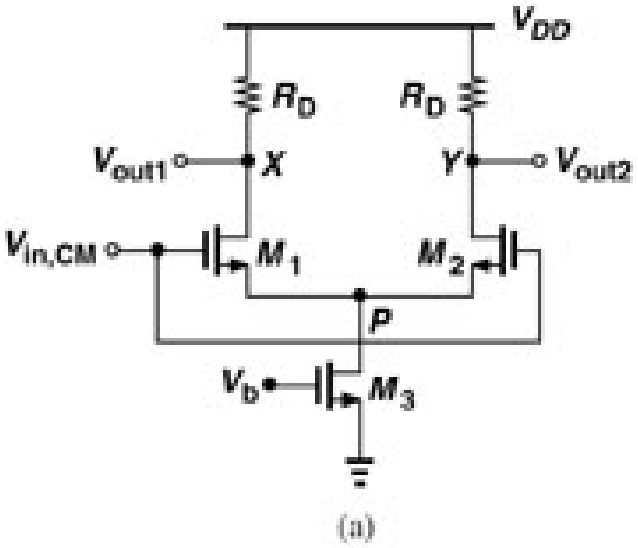
Can $V_{in,CM}$ be arbitrarily large or small?

$V_{in,CM}$ must be large enough for M_3 to be in saturation



M_1,M_2 operate like Source Followers: V_P increases as $V_{in,CM}$ increases – must be larger than V_b-V_{TH3}

$V_{in,CM}$ must not be too large to keep M_1 and M_2 from entering Triode Mode



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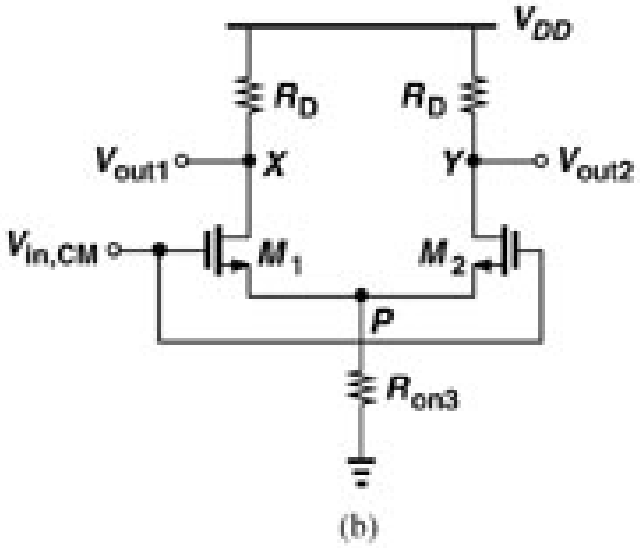

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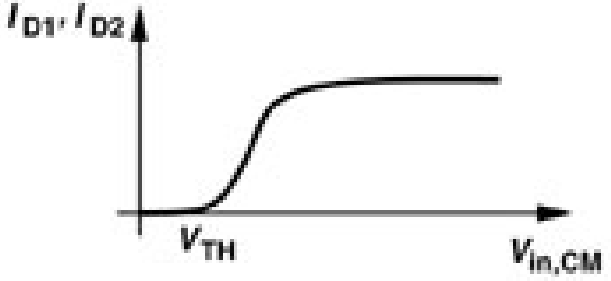
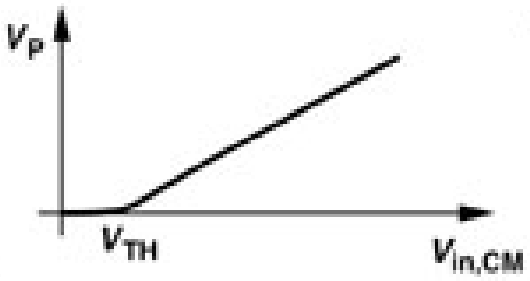
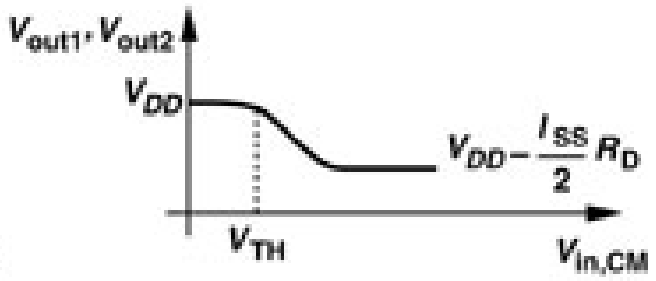
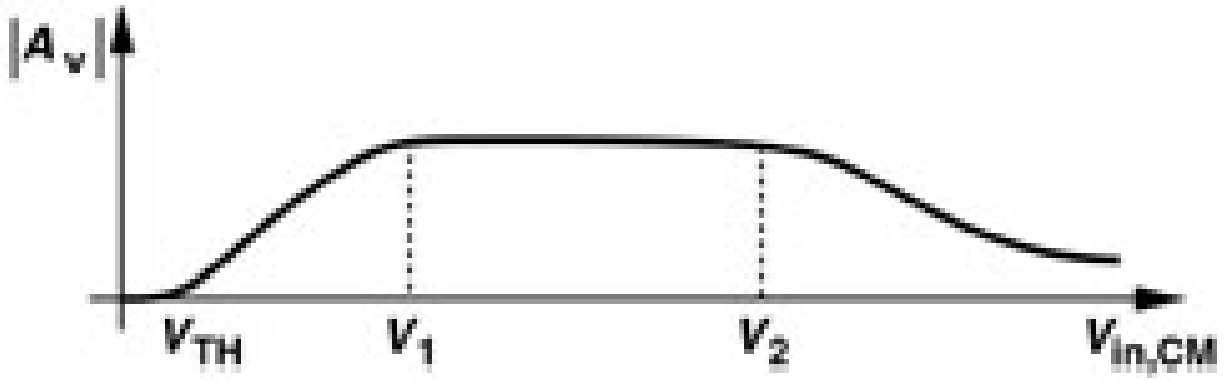






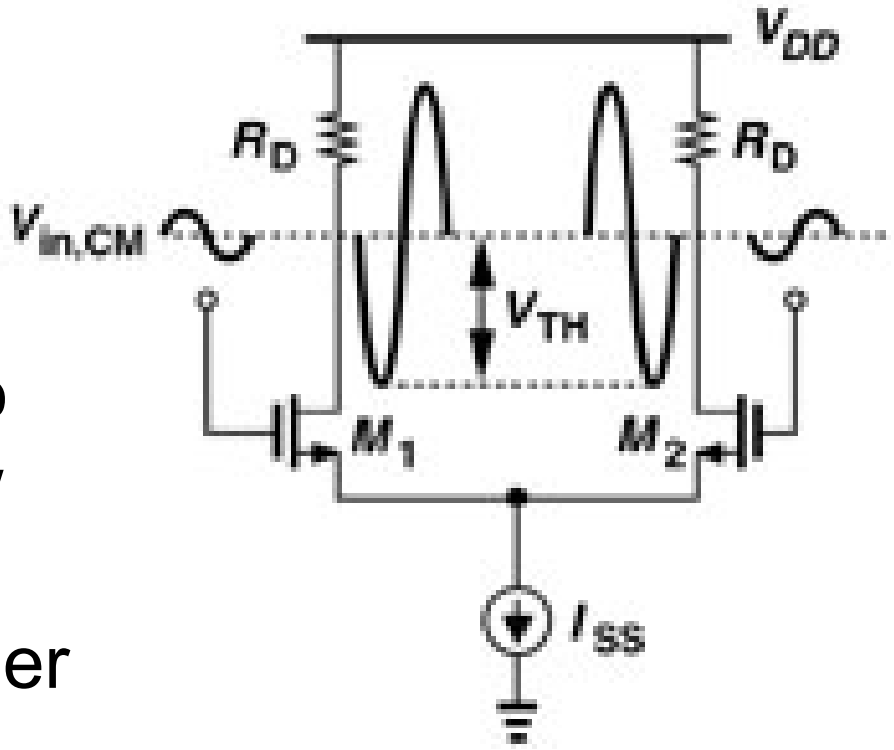
$$V_{GS1} + (V_{GS3} - V_{TH3}) \le V_{in,CM} \le \min[V_{DD} - R_D \frac{I_{SS}}{2} + V_{TH1}, V_{DD}]$$

Consequences of $V_{in,CM}$ going "off range"



- As long as common mode voltage is within the permitted range, differential gain is almost insensitive to it.
- Once too small or too large – gain falls off.

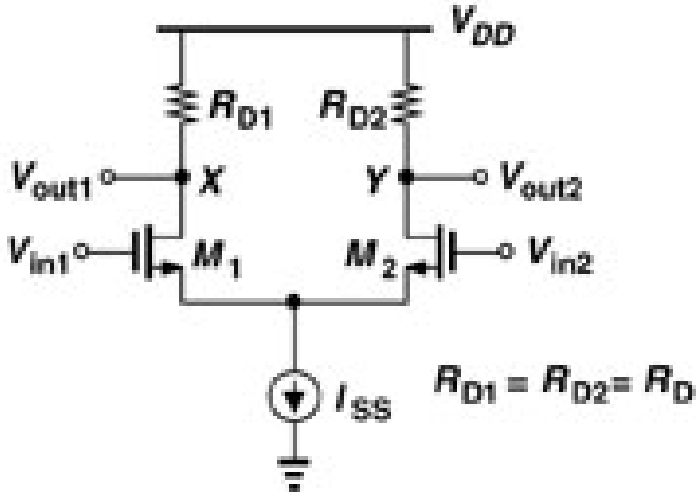
Common-Mode Input vs. Output Swing Tradeoff



Each drain voltage can go as high as V_{DD} and as low as $V_{in,CM}$-V_{TH}.
The larger $V_{in,CM}$ the smaller the swing.

Two types of Differential Gains

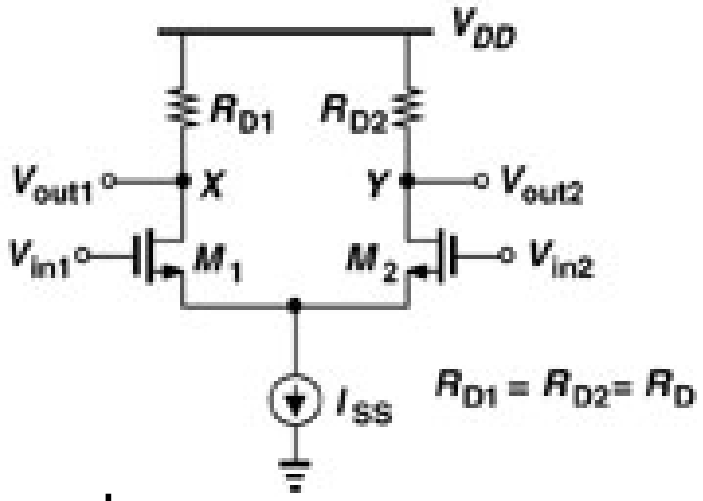
"Single-ended": V_{out1} (or V_{out2}) with respect to ground.



$$A_v(diff) = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} = ?$$

$$A_v(S.E.) = \frac{V_{out1}}{V_{in1} - V_{in2}} = ?$$

Current Division Mechanism



Calculate I_{D1} and I_{D2} in terms of V_{in1} and V_{in2}, assuming the circuit is symmetric, M_1 and M_2 are saturated, and $\lambda=0$.

Since the voltage at node P is equal to

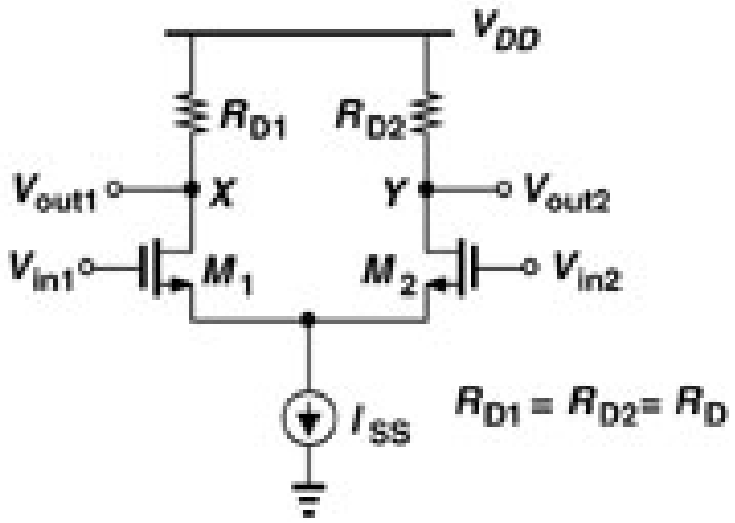
$V_P=V_{in1}-V_{GS1}=V_{in2}-V_{GS2}$,

$V_{in1}-V_{in2}=V_{GS1}-V_{GS2}$

$$V_{GS} = \sqrt{\frac{2I_D}{k_n'\frac{W}{L}}} + V_{TH}$$

Current Division Mechanism

Given the inputs and I_{SS}: Solve two equations with two unknowns for the transistor currents:



$$V_{in1} - V_{in2} = \sqrt{\frac{2I_{D1}}{k_n' \frac{W}{L}}} - \sqrt{\frac{2I_{D2}}{k_n' \frac{W}{L}}}$$

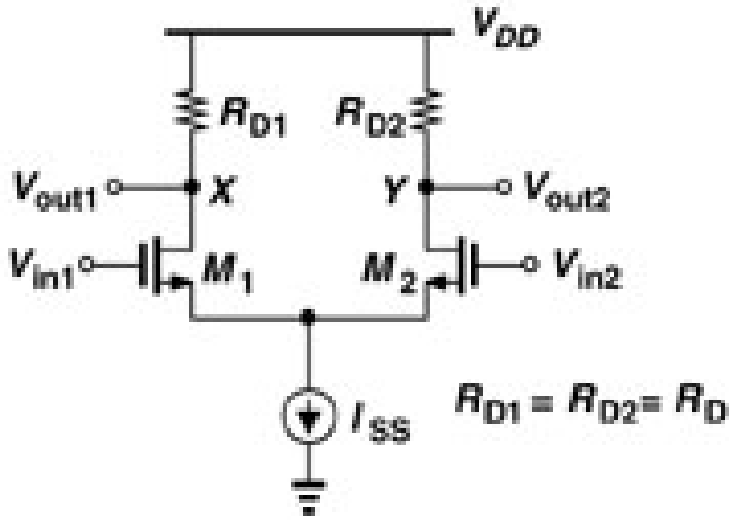
$$I_{SS} = I_{D1} + I_{D2}$$

CMOS Differential Amplifiers

Small-Signal Differential Gain-L16

Current Difference Properties

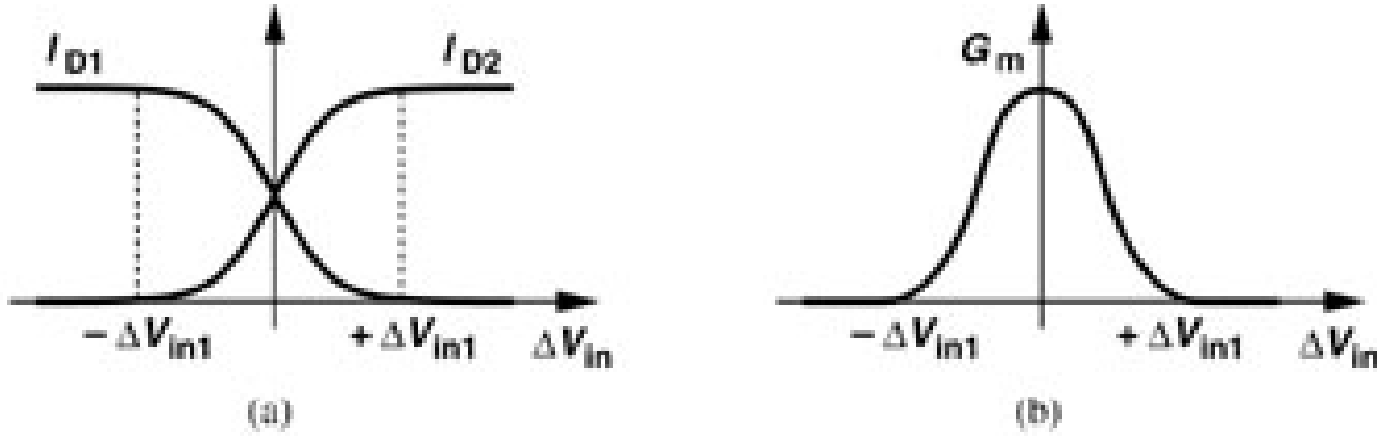
Even though each current is an even function of its respective gate-source voltage, the current difference is an odd function of the input voltage difference



$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{OX}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

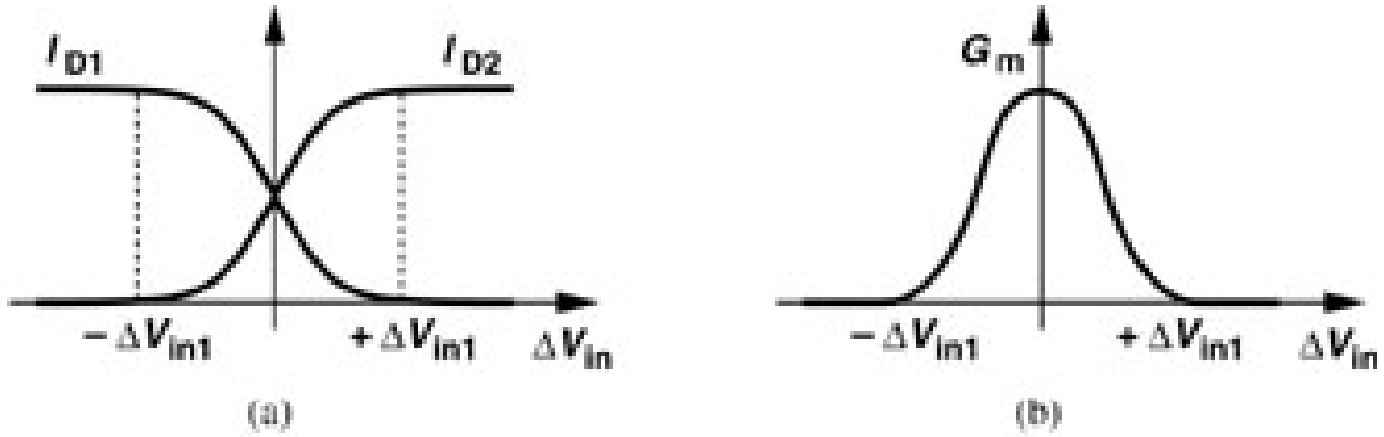
Differential Transconductance Gain vs. Input Voltage

$$\frac{\partial \Delta I_D}{\partial \Delta V_{in}} = G_m = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\frac{\dfrac{4I_{SS}}{\mu_n C_{ox} W/L} - 2(V_{in1}-V_{in2})^2}{\sqrt{\dfrac{4I_{SS}}{\mu_n C_{ox}\dfrac{W}{L}} - (V_{in1}-V_{in2})^2}}$$



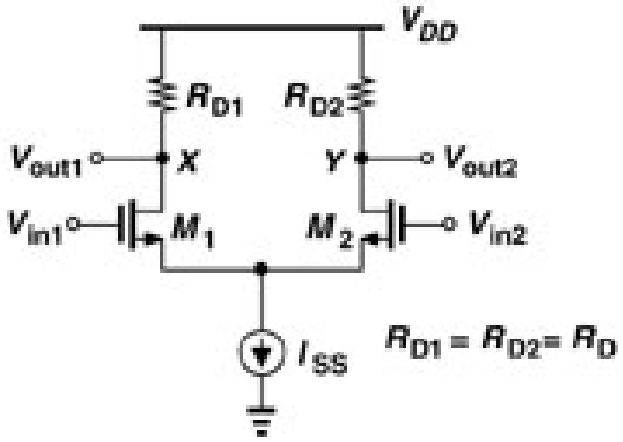
Maximum Differential Transconductance Gain Occurs at $\Delta V_{in}=0$

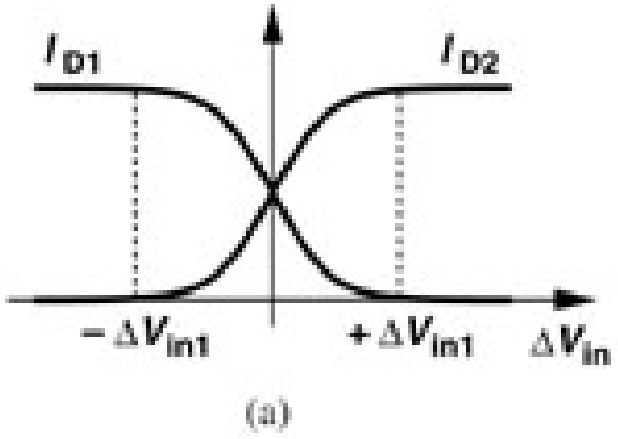
$$G_{m,\max} = \sqrt{\mu_n C_{ox}\left(\frac{W}{L}\right) I_{SS}}$$

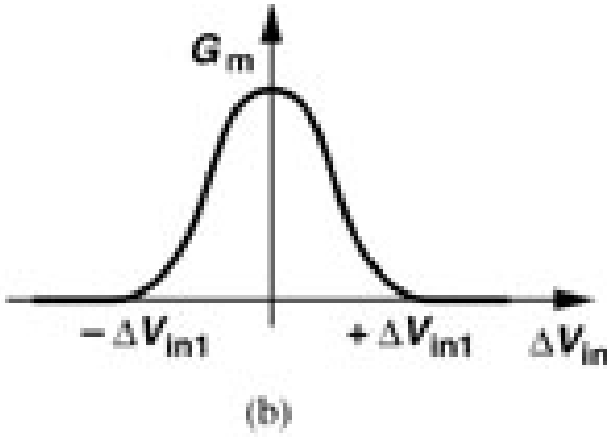


Differential Voltage Gain

$$V_{out1} - V_{out2} = R_D \Delta I_D = R_D G_m \Delta V_{in}$$

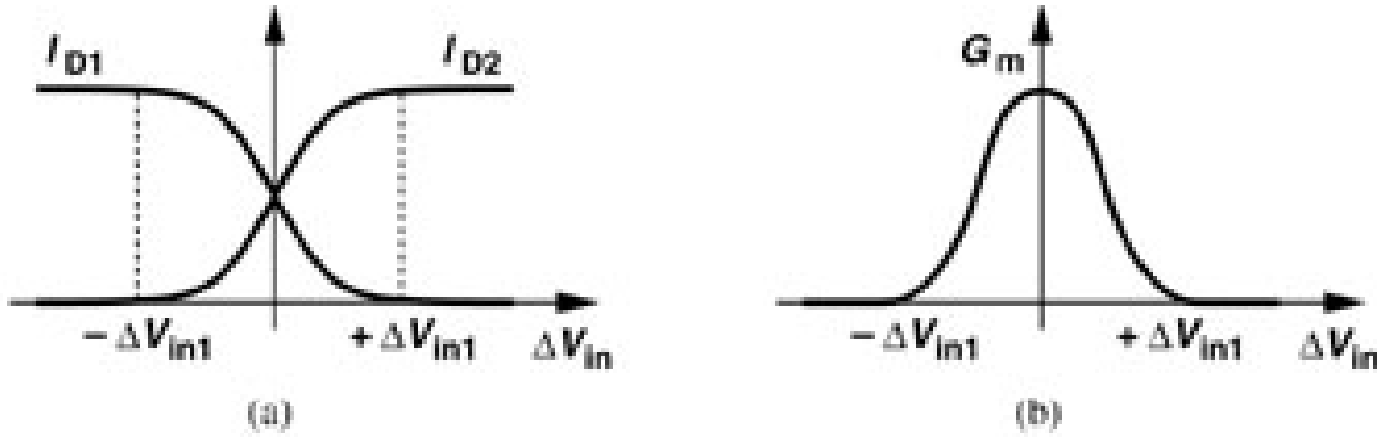






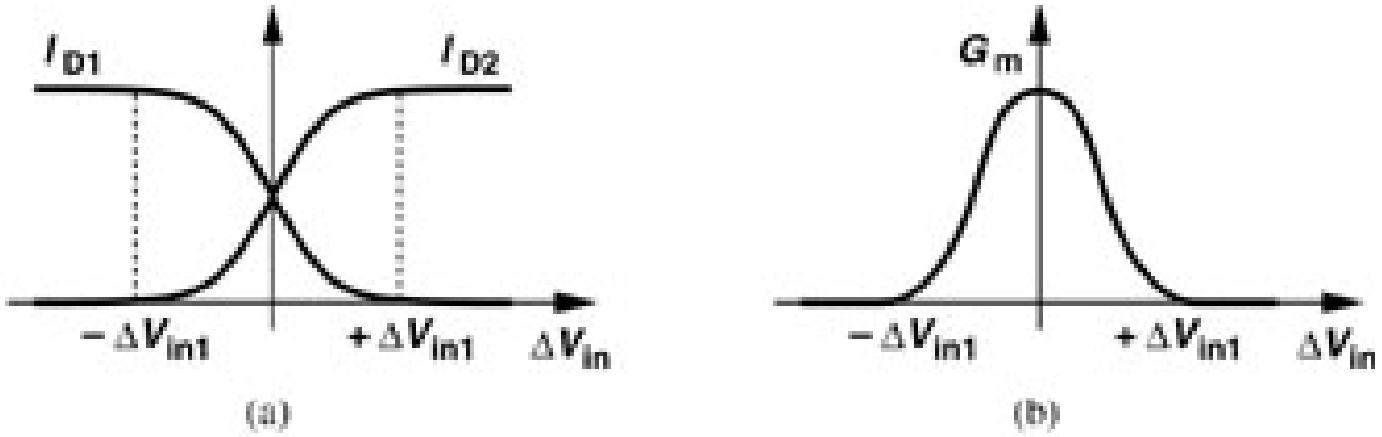
Differential Voltage Gain near $\Delta V_{in} = 0$

$$|A_V| = \frac{\Delta V_{out}}{\Delta V_{in}} = G_{m,\max} R_D = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}} R_D$$



Differential Transconductance Gain Falls to Zero at $\Delta V_{in} = \Delta V_{in1}$

$$\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$

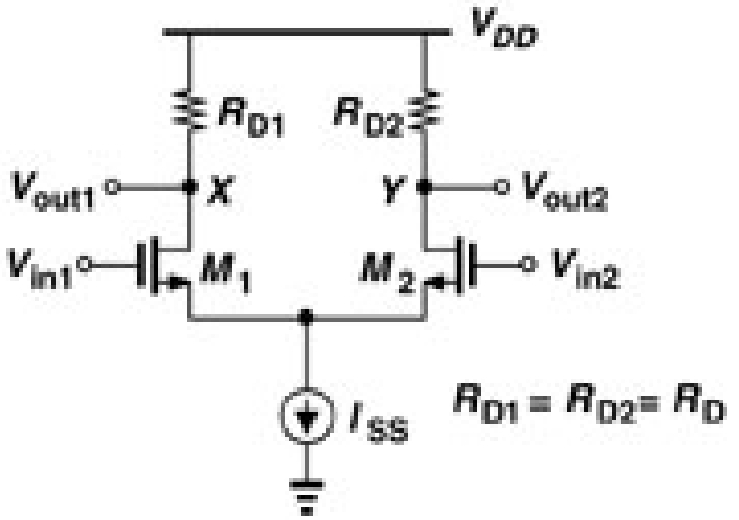


Current Difference Properties

It appears as if ΔI_D also becomes zero at $\Delta V_{in2}=(4I_{SS}/(\mu_n C_{OX} W/L))^{1/2}$

But this is incorrect.

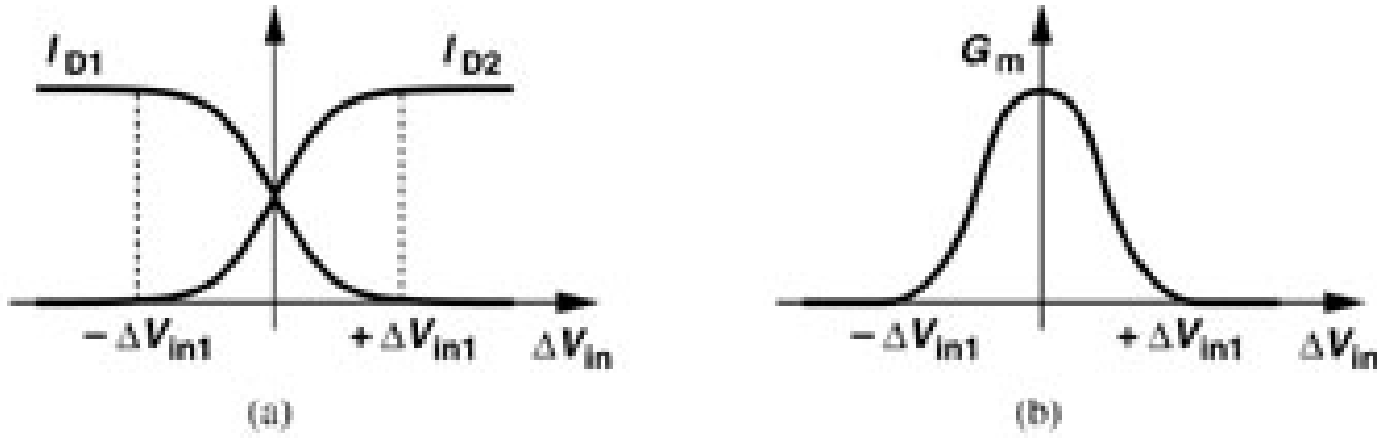
$\Delta V_{in2} > \Delta V_{in1}$ at which a total current stealing occurs.



$$I_{D1} - I_{D2} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L}(V_{in1} - V_{in2})\sqrt{\frac{4I_{SS}}{\mu_n C_{OX}\frac{W}{L}} - (V_{in1} - V_{in2})^2}$$

$\Delta V_{in} = \Delta V_{in1}$ is the maximum differential input that the amplifier can "handle"

$$\Delta V_{in1} = \sqrt{\frac{2I_{SS}}{\mu_n C_{ox} \frac{W}{L}}}$$



Also note that at $\Delta V_{in}=0$ each transistor carries a current of $I_{SS}/2$ and therefore :

$$(V_{GS}-V_{TH})_{1,2}=\sqrt{\frac{I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

Compare this equilibrium overdrive to the maximum differential input permitted:

$$(V_{GS}-V_{TH})_{1,2}=\frac{\Delta V_{in1}}{\sqrt{2}}$$

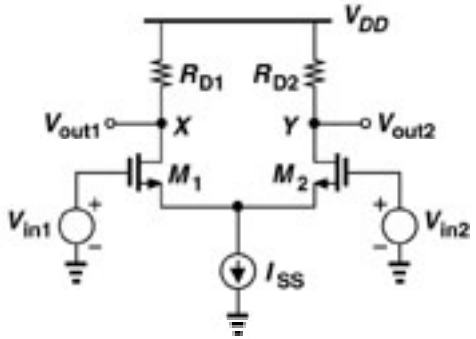
$$\Delta V_{in1}=\sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

It means that if we try to increase ΔV_{in1}, for a given I_{SS}, we need larger overdrive voltage in each transistor, and this is accomplished by reducing W/L

$$(V_{GS}-V_{TH})_{1,2}=\sqrt{\frac{I_{SS}}{\mu_n C_{ox}\frac{W}{L}}} \qquad (V_{GS}-V_{TH})_{1,2}=\frac{\Delta V_{in1}}{\sqrt{2}}$$

$$\Delta V_{in1}=\sqrt{\frac{2I_{SS}}{\mu_n C_{ox}\frac{W}{L}}}$$

Small-Signal Differential Voltage Gain



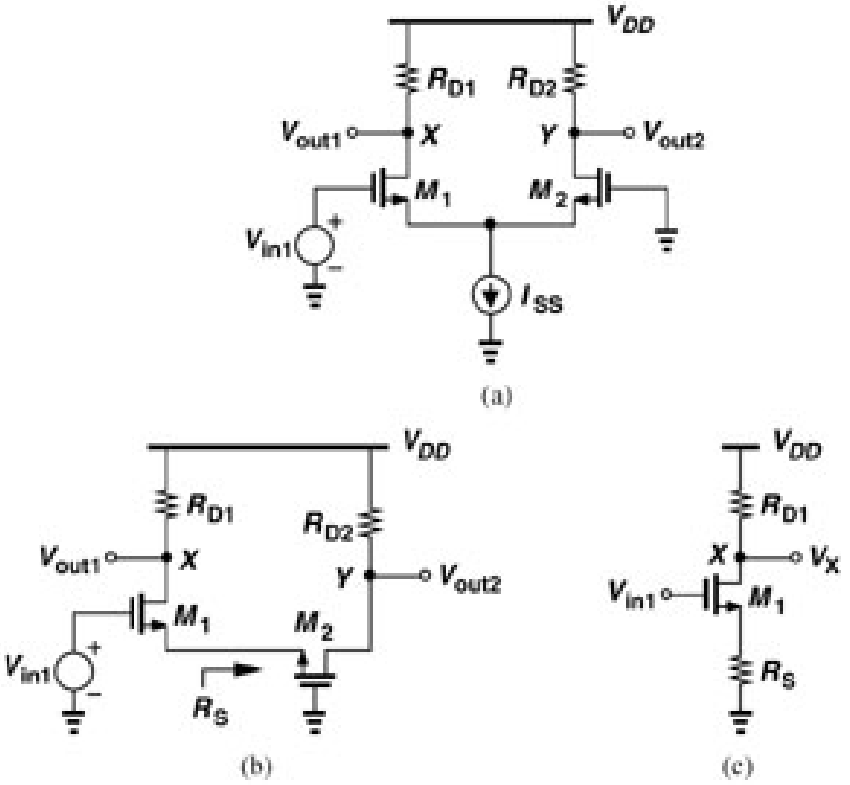
- For $|\Delta V_{in}| \approx 0$ (sufficiently small) we have:

$$|A_V| = \frac{\Delta V_{out}}{\Delta V_{in}} = G_{m,\max} R_D = \sqrt{\mu_n C_{ox} \frac{W}{L} I_{SS}}\, R_D = g_m R_D$$

Where g_m is that of a NMOS with a current of $I_{SS}/2$

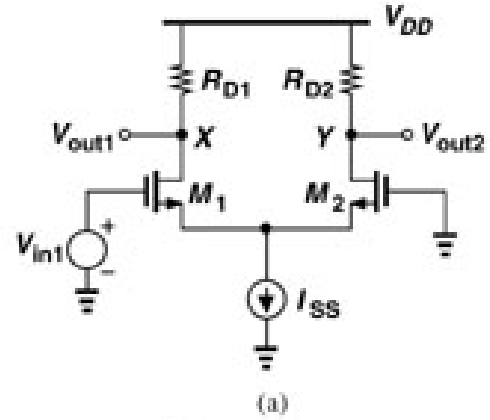
Differential Gain: What does each input "see"?

- By superposition let's short V_{in2} to ground and see the effect of V_{in1}:
- The effect of V_{in1} on V_X is the same as that of a CS amplifier (degenerated by the resistance seen looking into the source of M_2) on V_D



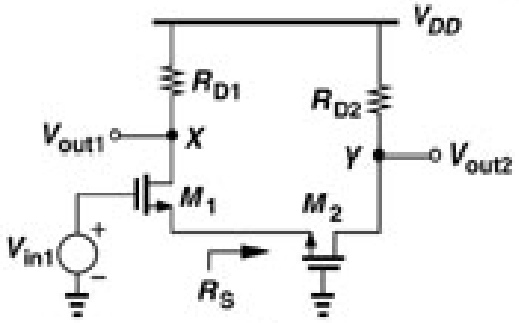
Differential Gain: Effect of V_{in1} on V_X

Neglecting λ_2 and $g_{mb2} R_S \approx 1/g_{m2}$

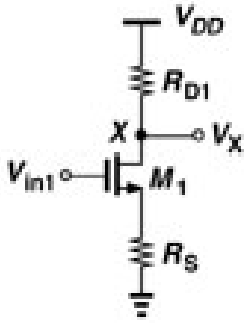


(a)

$$\frac{V_X}{V_{in1}} \approx \frac{-R_D}{\dfrac{1}{g_{m1}} + \dfrac{1}{g_{m2}}}$$

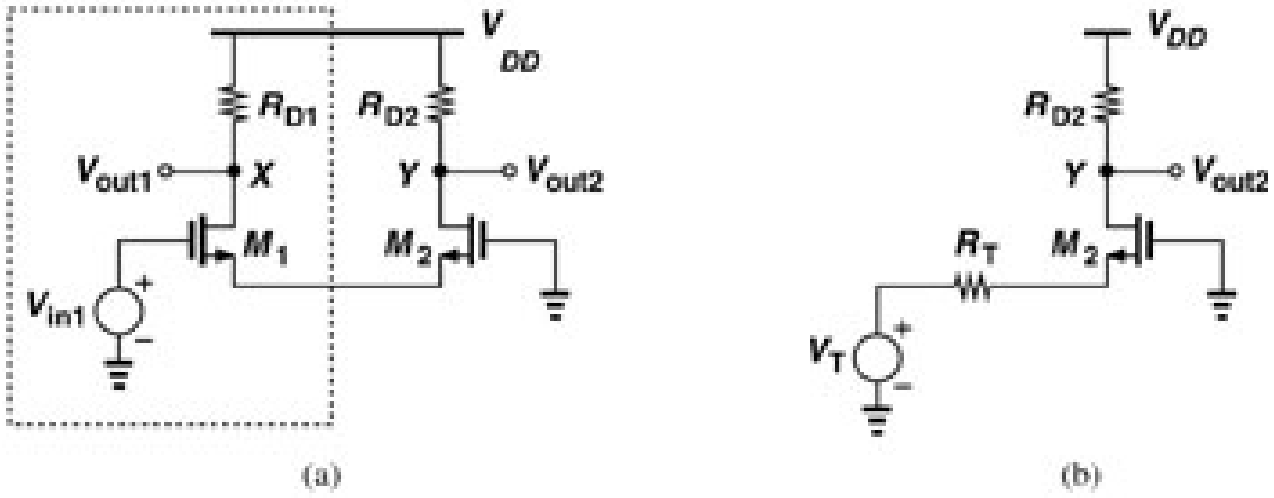


(b)



(c)

Differential Gain: Effect of V_{in1} on V_Y

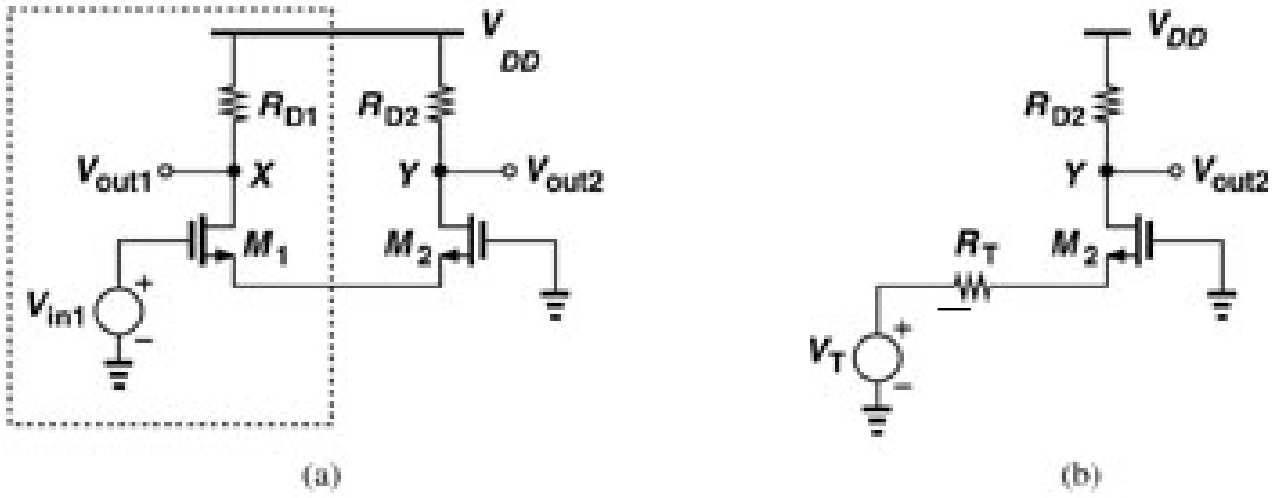


The effect of V_{in1} on V_Y is the same as that of a Source Follower (M_1) amplifier driving a Common-Gate amplifier (M_2)

$$V_T = V_{in1}$$

$$R_T = \frac{1}{g_{m1}}$$

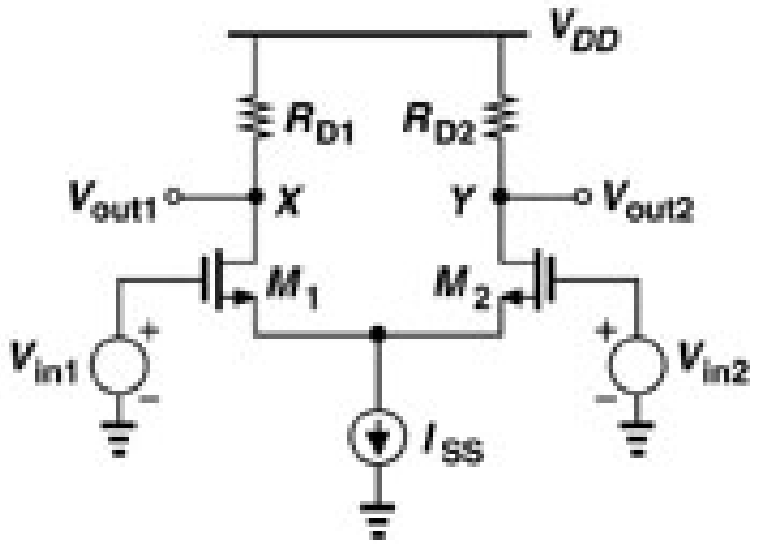
Differential Gain: Effect of V_{in1} on V_Y



The effect of V_{in1} on V_Y is the same as that of a Source Follower (M_1) amplifier driving a Common-Gate amplifier (M_2)

$$\frac{V_Y}{V_{in1}} \approx \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

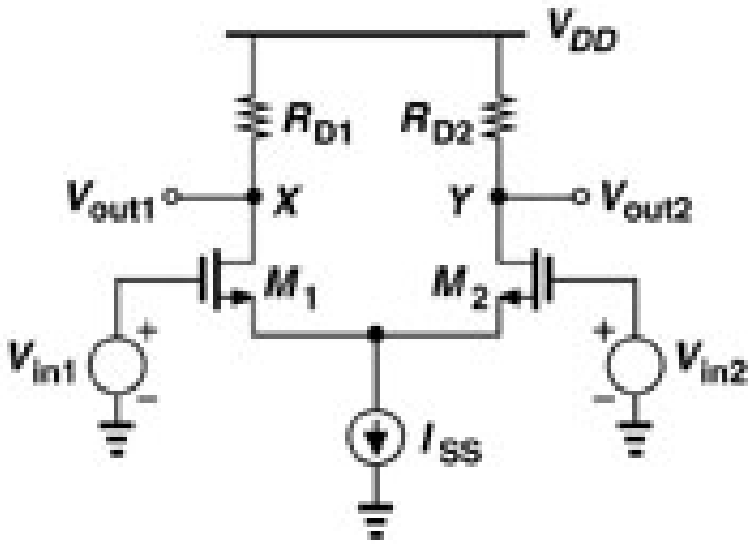
V_X-V_Y as function of V_{in1} if V_{in2}=0



$$(V_X - V_Y)_{due\_to\_V_{in1}} = \frac{-2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in1} = -g_m R_D V_{in1}$$

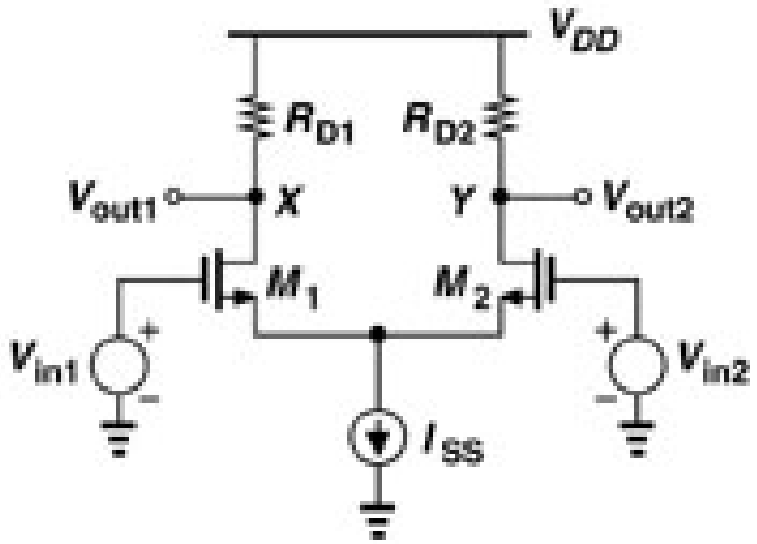
Because g_{m1}=g_{m2}=g_m

By Symmetry: V_X-V_Y as function of V_{in2} if V_{in1}=0



$$(V_X - V_Y)_{due\_to\_V_{in2}} = \frac{2R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}} V_{in2} = g_m R_D V_{in2}$$

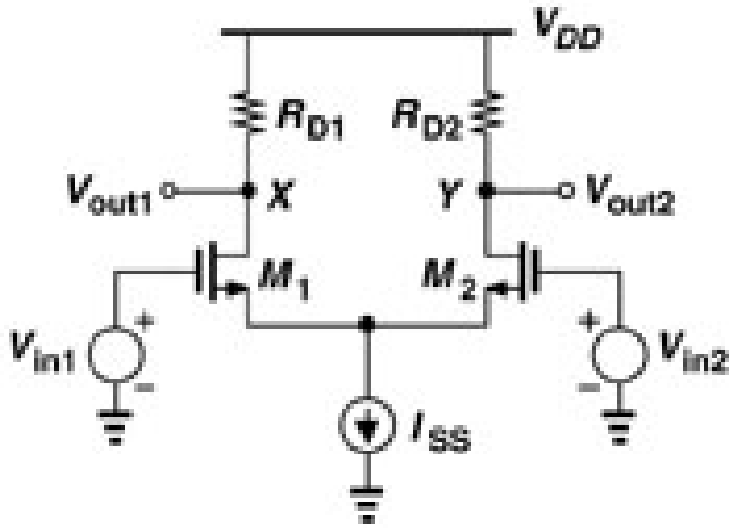
V_X-V_Y as function of V_{in2} and V_{in1}



$$(V_X - V_Y)_{due\_to\_both} = g_m R_D V_{in2} - g_m R_D V_{in1}$$

yielding the gain $g_m R_D$ regardless where and how the inputs are applied

Single-ended Differential Voltage Gain



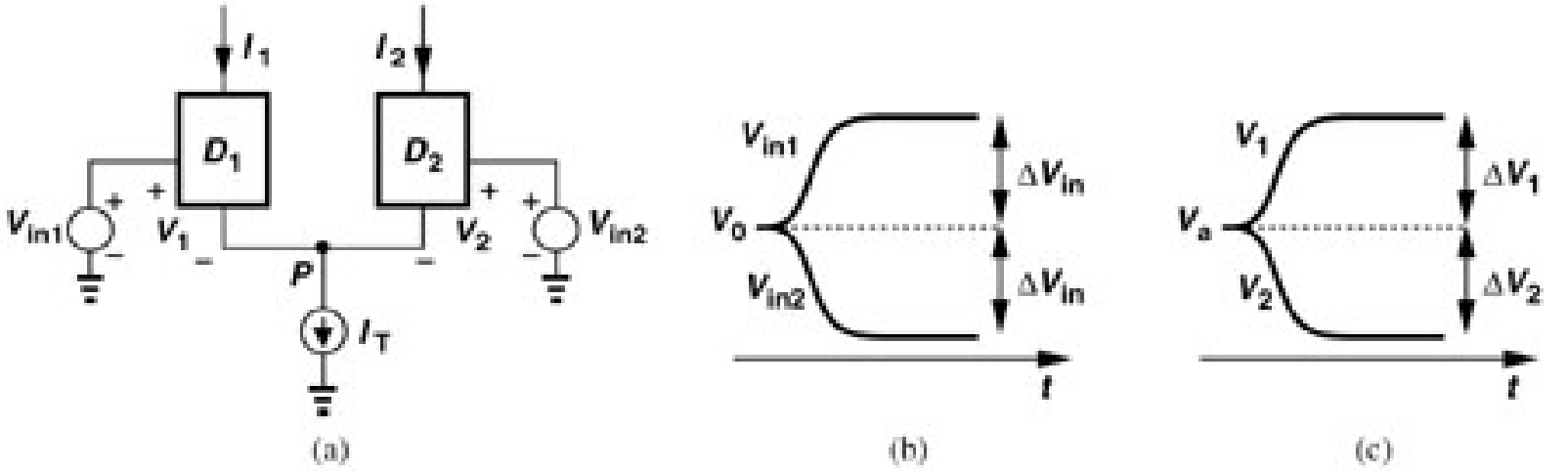
$$A_{V,SE} = \frac{V_X}{V_{in1} - V_{in2}} = -\frac{g_m}{2} R_D$$

$$A_{V,SE} = \frac{V_Y}{V_{in1} - V_{in2}} = \frac{g_m}{2} R_D$$

Comparison: Differential voltage gain of a differential amplifier vs. voltage gain of a CS amplifier

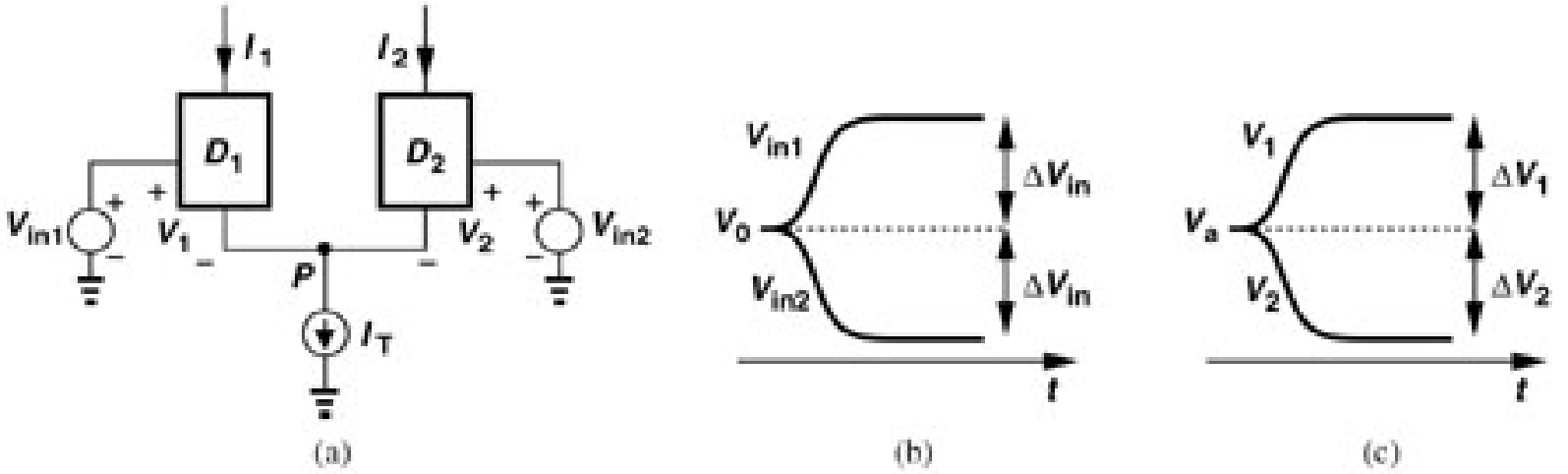
- If the same current source I_{SS} drives the differential amplifier and the CS, each transistor of the differential amplifier has g_m which is $1/\sqrt{2}$ of that of the CS transistor. Differential gain reduces by a factor of $1/\sqrt{2}$.
- If both amplifiers have the same W/L in each transistor and the same load, and we want the gain to be the same, then if we use I_{SS} at CS, we need to use $2I_{SS}$ at the differential amplifier.

The “Virtual Ground” Concept



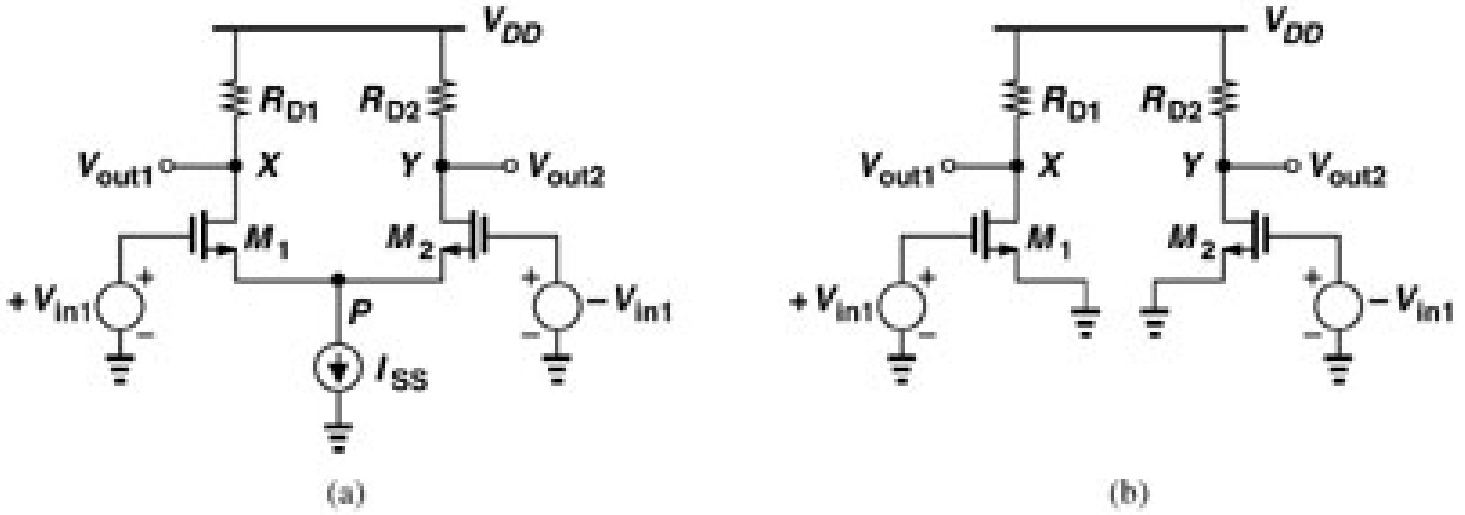
- In a symmetric device (as above), if inputs change anti-symmetrically (one goes up by a certain amount, and the other goes down by the same amount), then V_P does not change.
- For small-signal analysis point P becomes “virtual ground”.

The “Virtual Ground” Concept



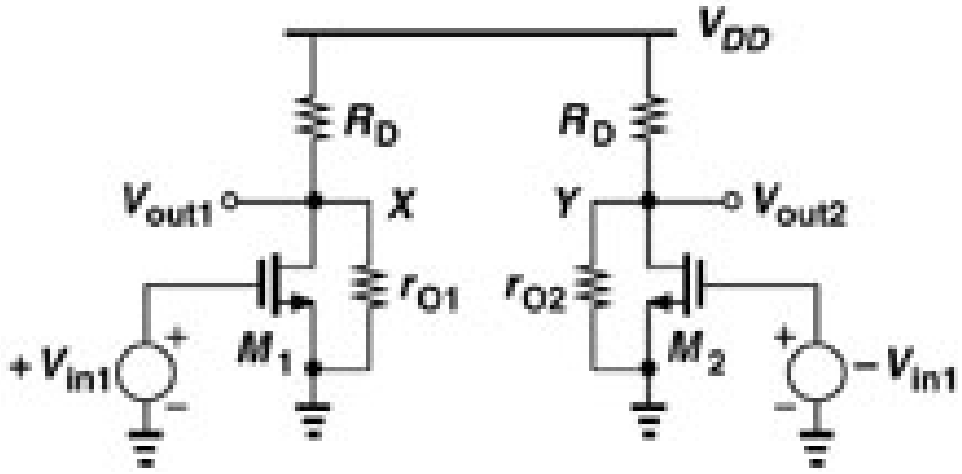
- Explanation: Consider the complete “Kirchhoff path” $V_{in1} \rightarrow D_1 \rightarrow D_2 \rightarrow V_{in2}$.
- By symmetry of the devices, and anti-symmetry of sources, using voltage-division argument, V_P stays constant.
- See book (pp. 114-115) for 2-3 more explanations.

The “Half-Circuit” Concept



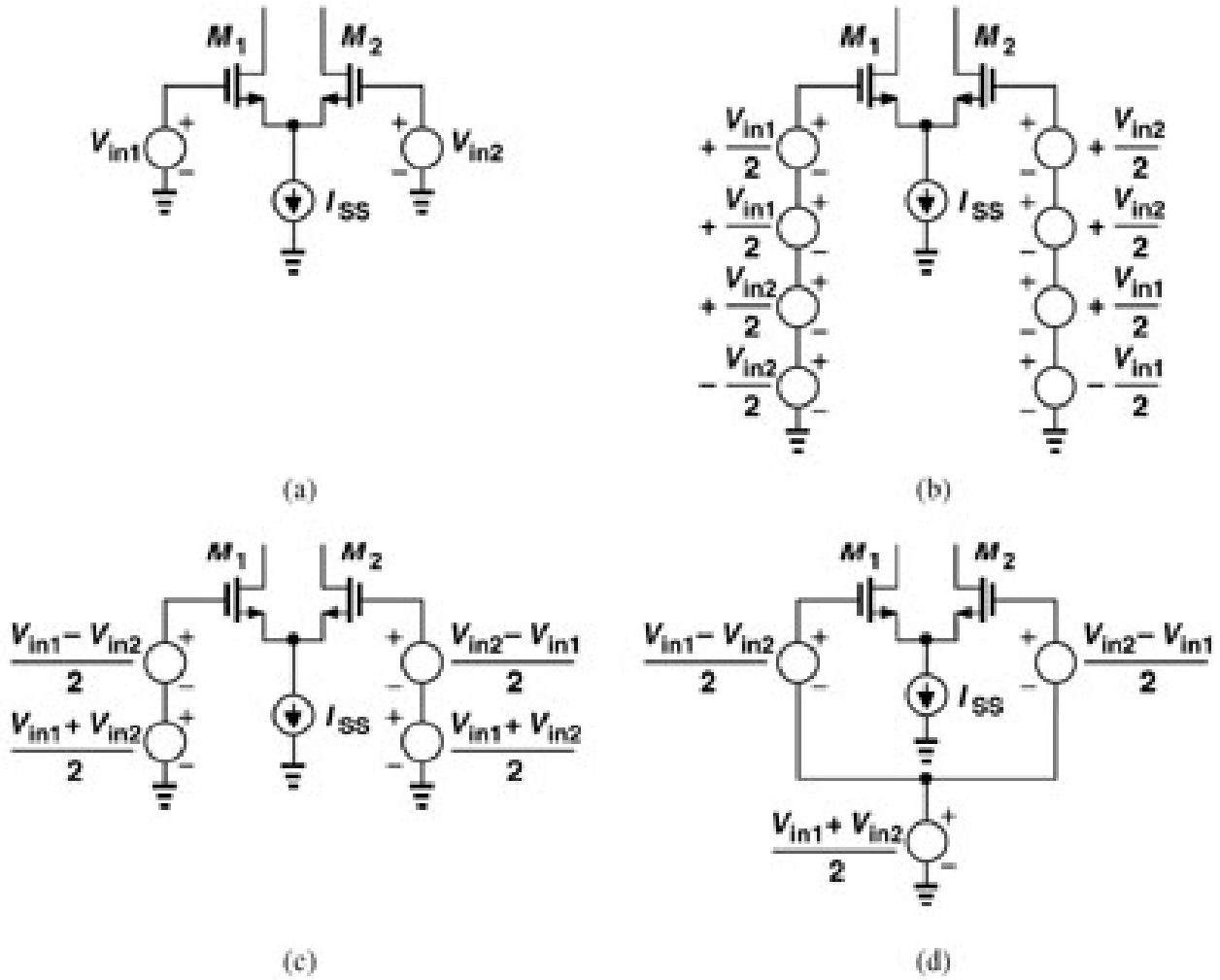
- For small-signal analysis, because point P is “ground” (this is valid only if inputs are anti-symmetric and devices are symmetric!), we can analyze each CS “half-circuit” separately.

Differential Gain with λ effect



- Based on the half-circuit concept, gain calculation is highly simplified. We get:
- $V_X/V_{in1}=-g_m(R_D||r_o)=V_Y/(-V_{in1})$
- $(V_X-V_Y)/2V_{in1}=-g_m(R_D||r_o)$

In general V_{in1} and V_{in2} are arbitrary (not necessarily anti-symmetric): What do we do?



Analysis of Differential Amplifiers for arbitrary inputs

- As long as circuit operates more or less linearly, we use superposition of two analyses:
- Differential input analysis, using anti-symmetric inputs derived from the difference between the inputs.
- Common-mode analysis, where an input equals to the average of both inputs is applied to both transistors.

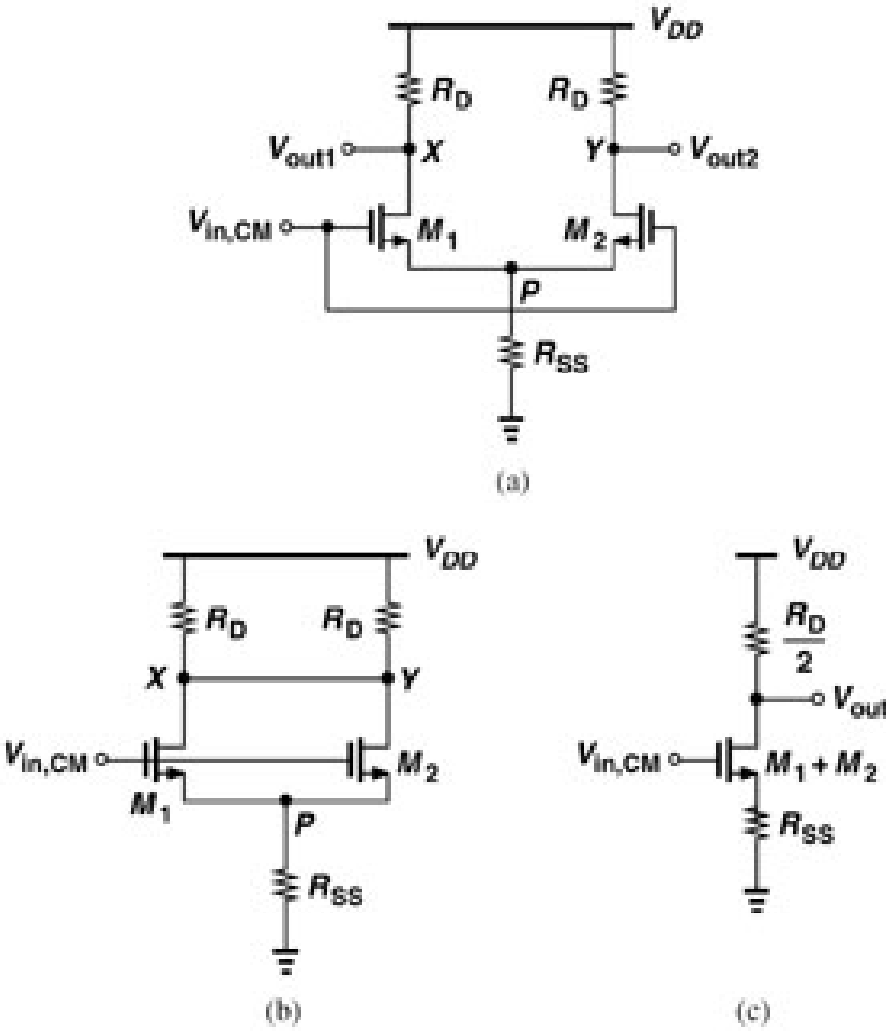
CMOS Differential Amplifiers

Common-Mode Analysis –L17

Goal: No common-mode signal at amplifier's output

- If amplifier is not 100% symmetric, CM signals will not be fully cancelled out.
- If the DC current source (biasing the amplifier) is not ideal (that is, has a finite output resistance) then CM signal appears at each single-ended output.

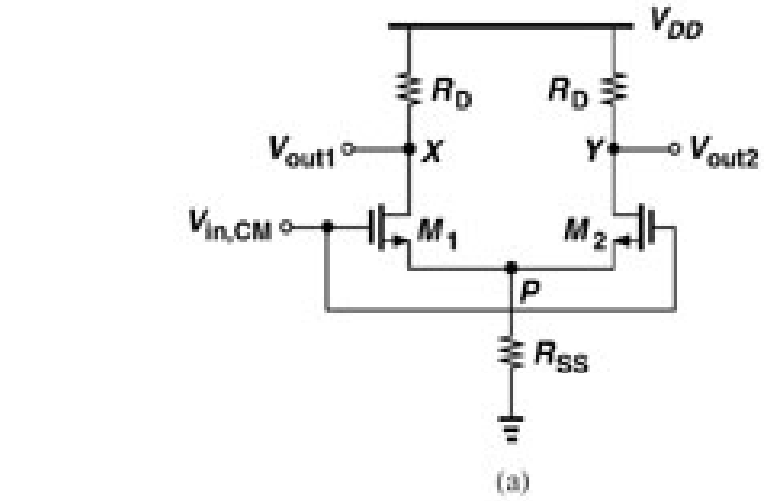
Single-ended Common-Mode Response of a symmetric amplifier



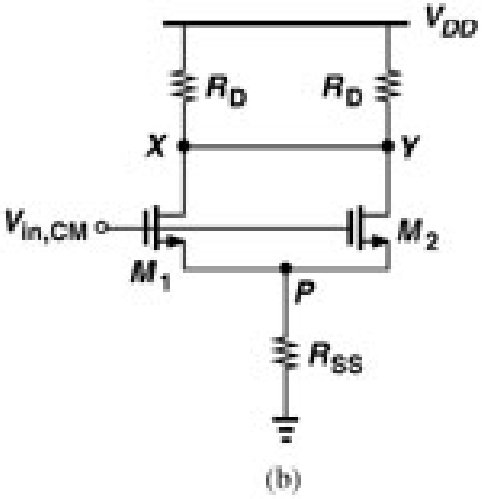
Consider a small-signal analysis for the common-mode signal.

Current source is represented by its output resistance R_{SS}

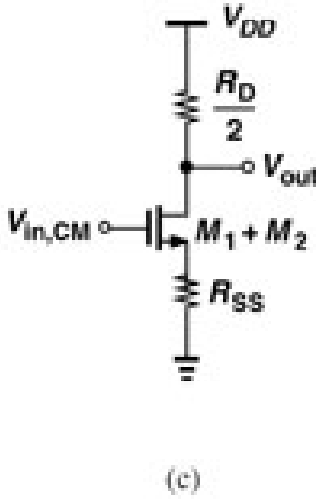
Single-ended Common-Mode Response of a symmetric amplifier



(a)



(b)

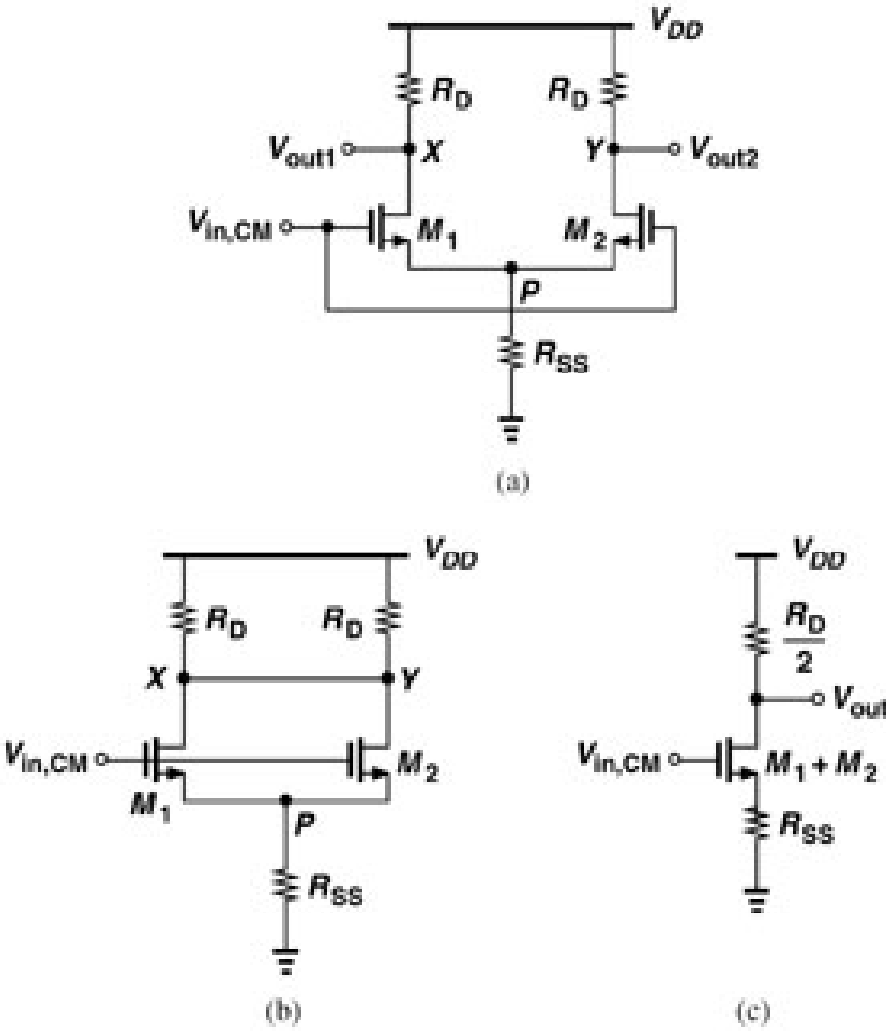


(c)

As $V_{in,CM}$ changes so does V_P. As a result, I_D currents change, and V_X and V_Y change.

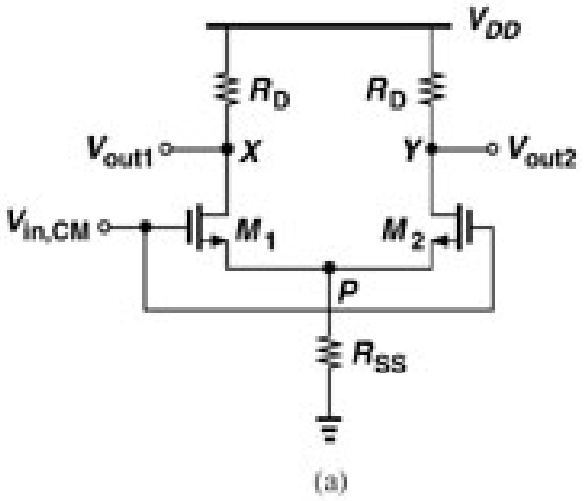
V_X-V_Y continues to be zero.

Single-ended Common-Mode Response of a symmetric amplifier



To find V_X as function of $V_{in,CM}$ we may do a “half circuit analysis”, splitting R_{SS} into two parallel $2R_{SS}$ resistors, or equivalently, connect transistors in parallel (as shown).

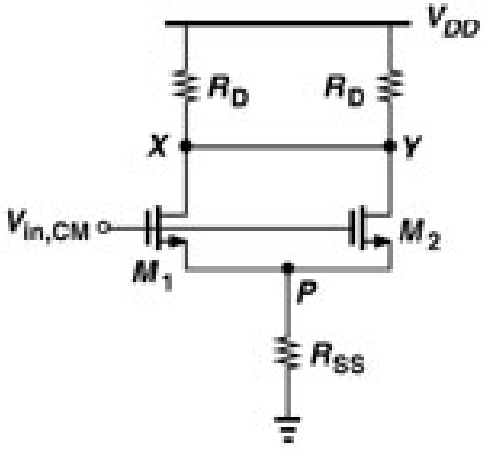
Single-ended Common-Mode Gain of a symmetric amplifier assuming λ=0 and γ=0



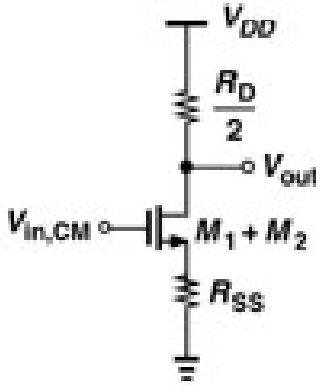
(a)

$$A_{V,CM} = \frac{V_{out}}{V_{in,CM}} = \frac{V_X}{V_{in,CM}} = \frac{V_Y}{V_{in,CM}}$$

$$= -\frac{R_D/2}{1/(2g_m) + R_{SS}}$$



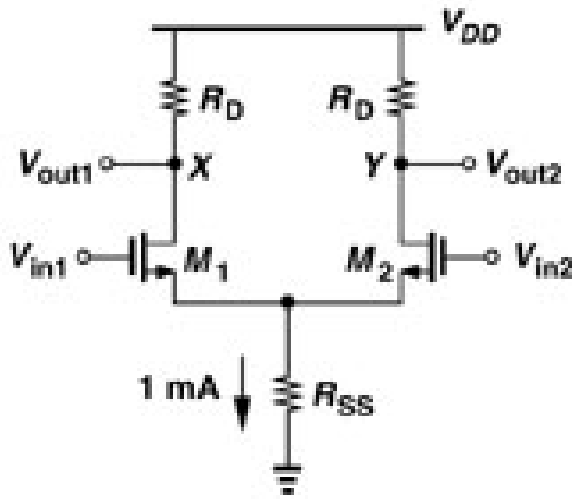
(b)



(c)

M_1+M_2 has twice the width and bias current, therefore g_m is doubled.

Most Primitive Differential Amplifier: Resistor in place of current source

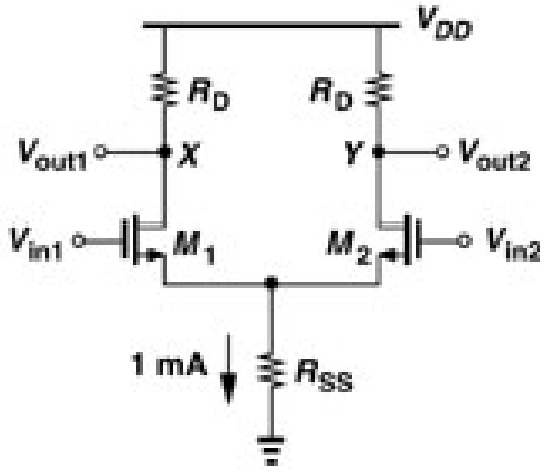


- Example: Let V_{DD}=3V, $(W/L)_1$=$(W/L)_2$=25/0.5
- $\mu_n C_{OX}$=50μA/V^2, V_{TH}=0.6V, λ=0, γ=0, R_{SS}=500Ω
- Because I_{D1}=I_{D2}=0.5mA, we have:

$$V_{GS1} = V_{GS2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{OX}\dfrac{W}{L}}} + V_{TH} = 1.23V$$

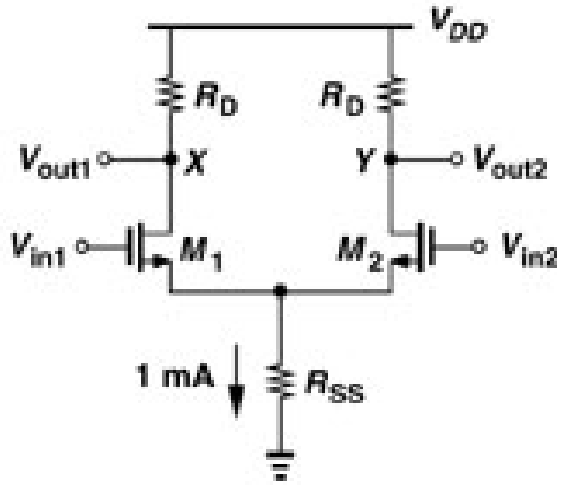
“Resistor current source” example

$$V_{GS1} = V_{GS2} = \sqrt{\frac{2I_{D1}}{\mu_n C_{OX}\frac{W}{L}}} + V_{TH} = 1.23V$$



- Also: $V_S = I_{ss}R_{SS} = 0.5V$
- Bias voltage at gates $V_{in,CM} = V_{GS1} + V_S = 1.73V$
- This voltage creates the necessary 0.5mA current in each of the transistors.

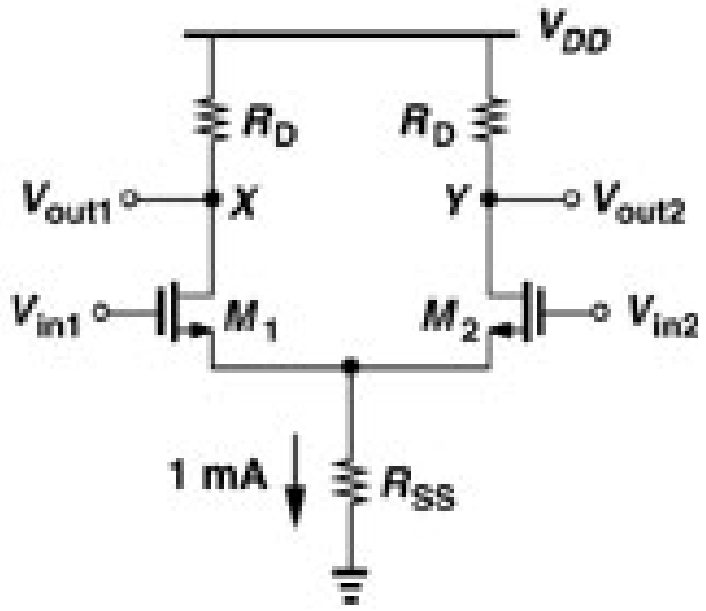
“Resistor current source” example – differential gain design



$$g_m = \sqrt{2\mu_n C_{OX} \frac{W}{L} I_{D1}} = \frac{1}{632\Omega}$$

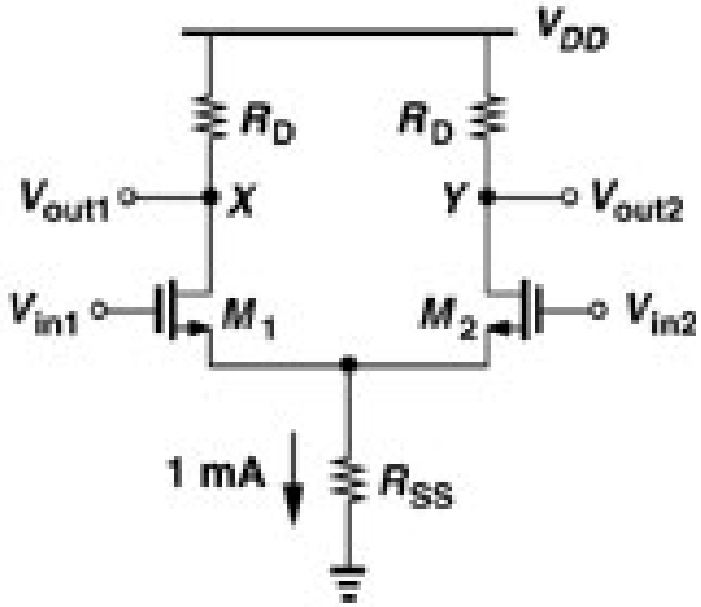
If R_D=3.16KΩ then differential voltage gain = $g_m R_D$=5

“Resistor current source” example – with such R_D are transistors in Saturation?



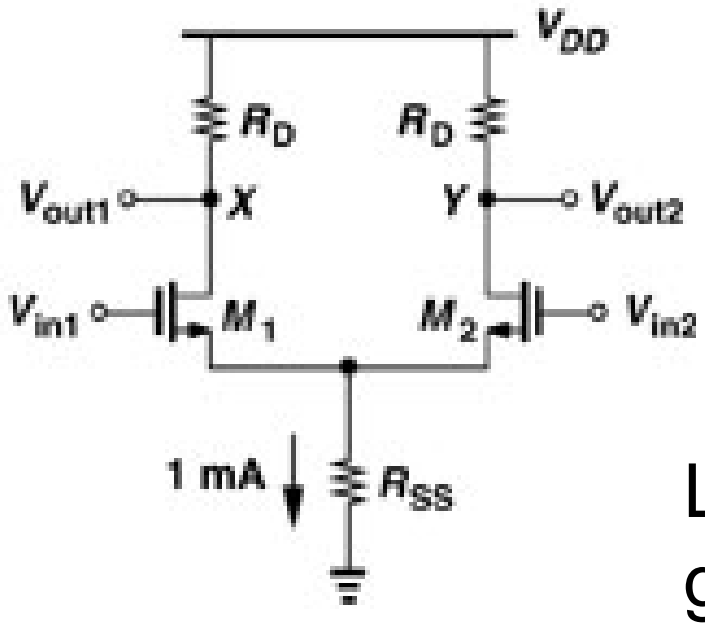
$V_{out1}=V_{out2}=V_{DD}-I_DR_D=1.42V > V_{in,CM} – V_{TH}$ =1.73 – 0.6 = 1.13V by 290mV (the overdrive)

“Resistor current source” example – Common-Mode Response



If $V_{in,CM}$ increases by 50mV, what will happen to each output?

“Resistor current source” example – Common-Mode Response

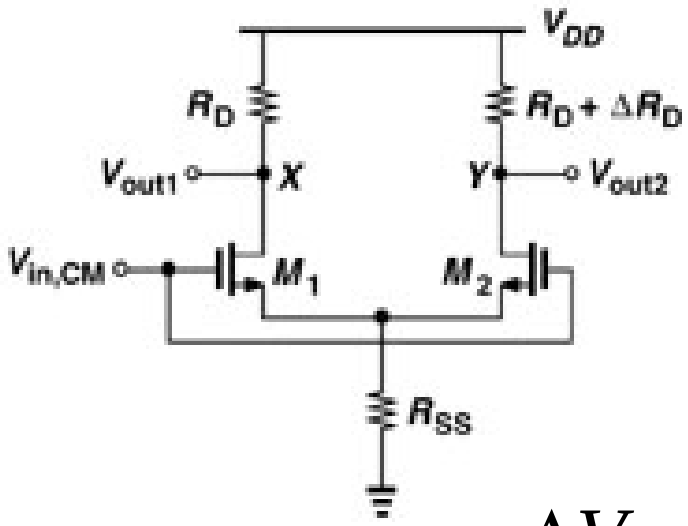


$$A_{V,CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}} = -\frac{R_D/2}{1/(2g_m) + R_{SS}}$$

Large CM gain of 1.94 is due to the small R_{SS}

$$\Rightarrow |\Delta V_X| = \Delta V_{in,CM} \frac{R_D/2}{1/(2g_m) + R_{SS}} = (50mV) \cdot 1.94 = 96.8mV$$

Common-Mode Response with asymmetric R_D assuming λ=0



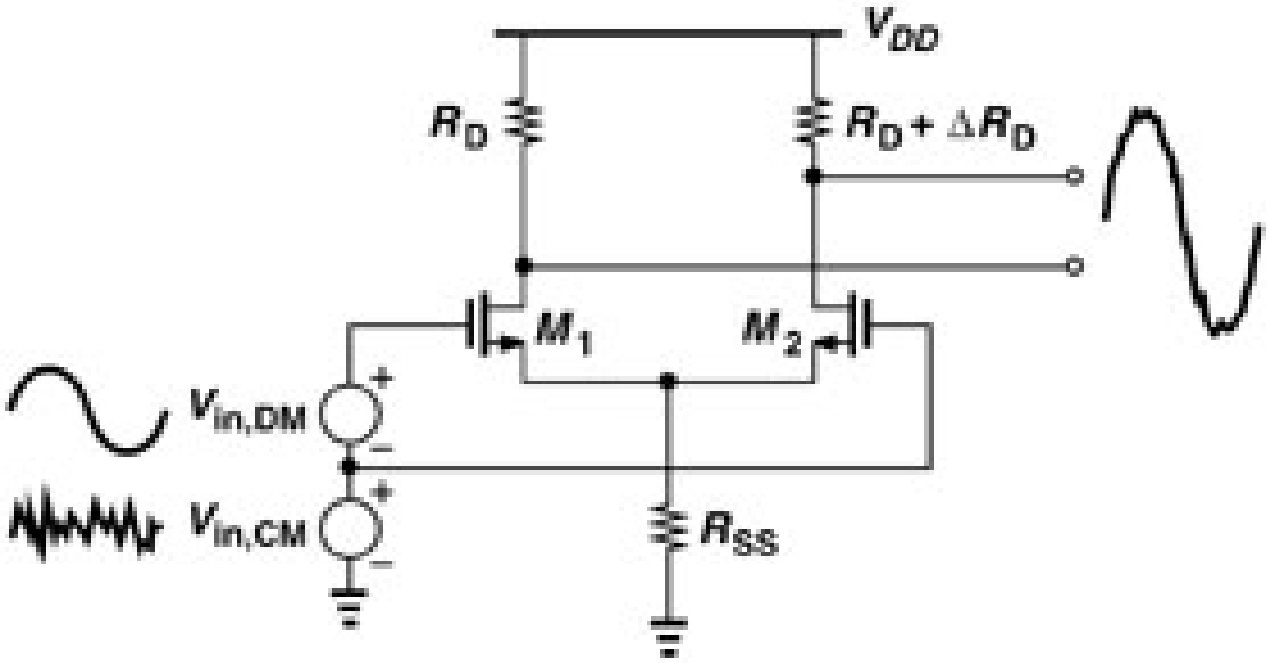
$$\frac{\Delta V_X}{\Delta V_{in,CM}} = -\frac{g_m}{1+2g_m R_{SS}} R_D$$

$$\frac{\Delta V_Y}{\Delta V_{in,CM}} = -\frac{g_m}{1+2g_m R_{SS}} (R_D + \Delta R_D)$$

$$\frac{\Delta V_X - \Delta V_Y}{\Delta V_{in,CM}} = \frac{g_m}{1+2g_m R_{SS}} \Delta R_D$$

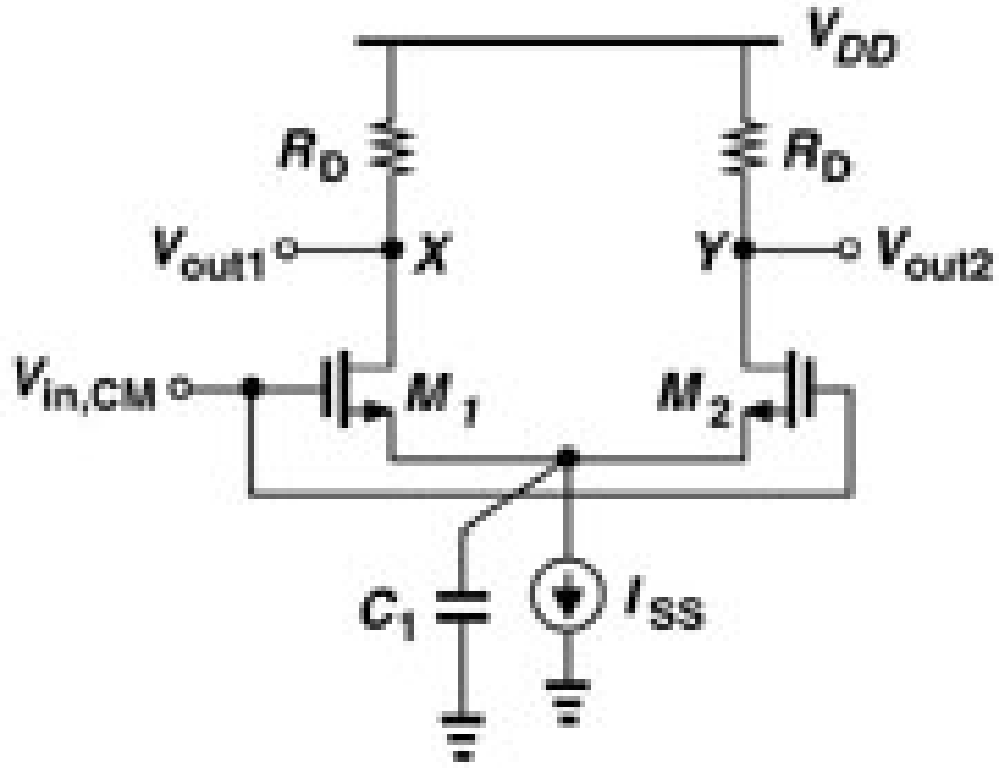
R_{SS} *above represents the current source – need large* R_{SS}

Common-Mode Response with asymmetric R_D

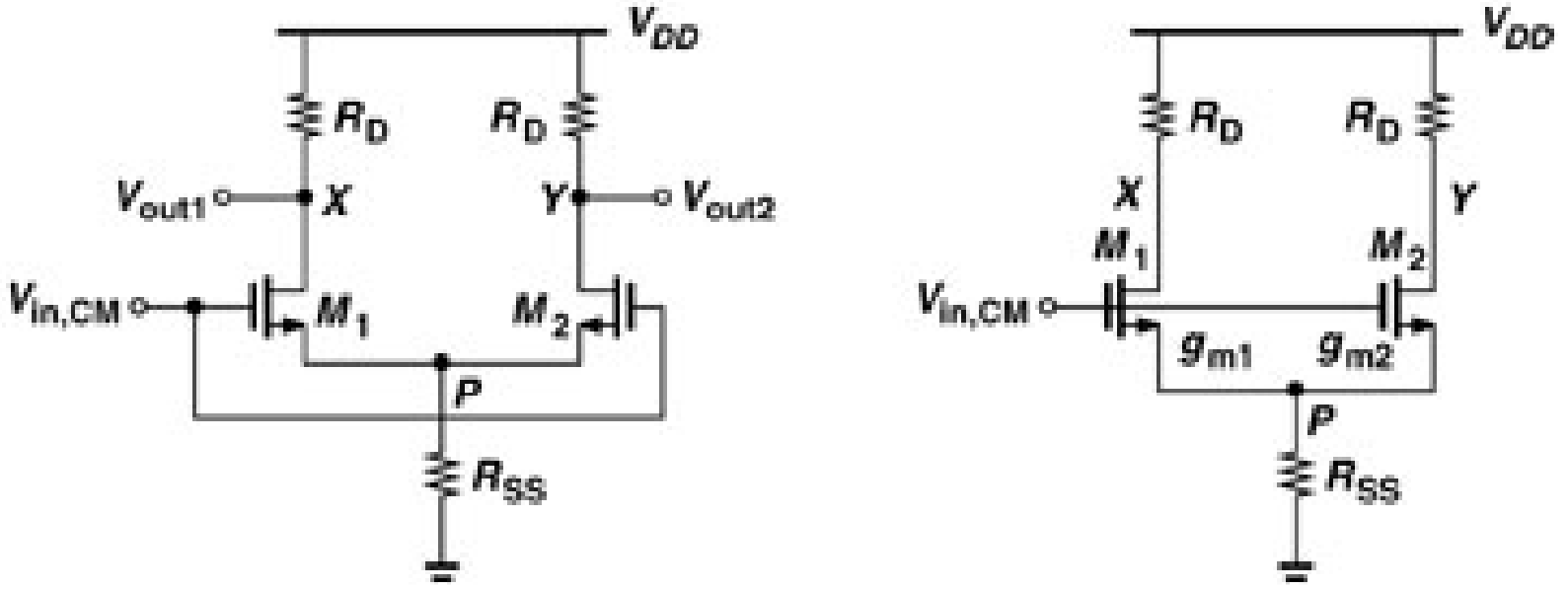


CM input noise corrupts the amplified differential signal, because of the asymmetry

For high-frequency Common-Mode input need to take into account parasitic capacitance effects, even if R_{SS} is large. C_1 is contributed by M_1,M_2 and I_{SS} and contributes to the impedance “seen” by the CM signal.



Mismatches in W/L, V_{TH} and other transistor parameters all translate to mismatches in g_m



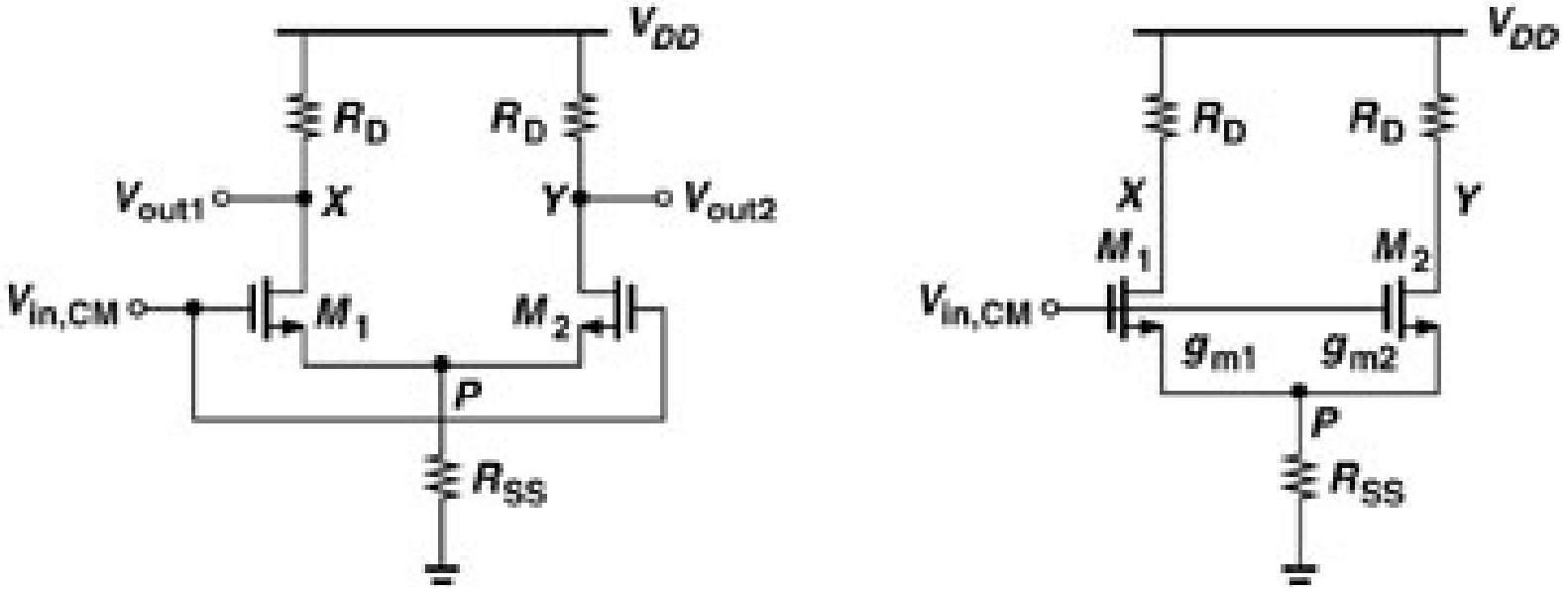
$$I_{D1} = g_{m1}(V_{in,CM} - V_P)$$

$$I_{D2} = g_{m2}(V_{in,CM} - V_P)$$

Small-signal analysis

$$\Rightarrow (g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS} = V_P$$

Mismatches in W/L, V_{TH} and other transistor parameters all translate to mismatches in g_m



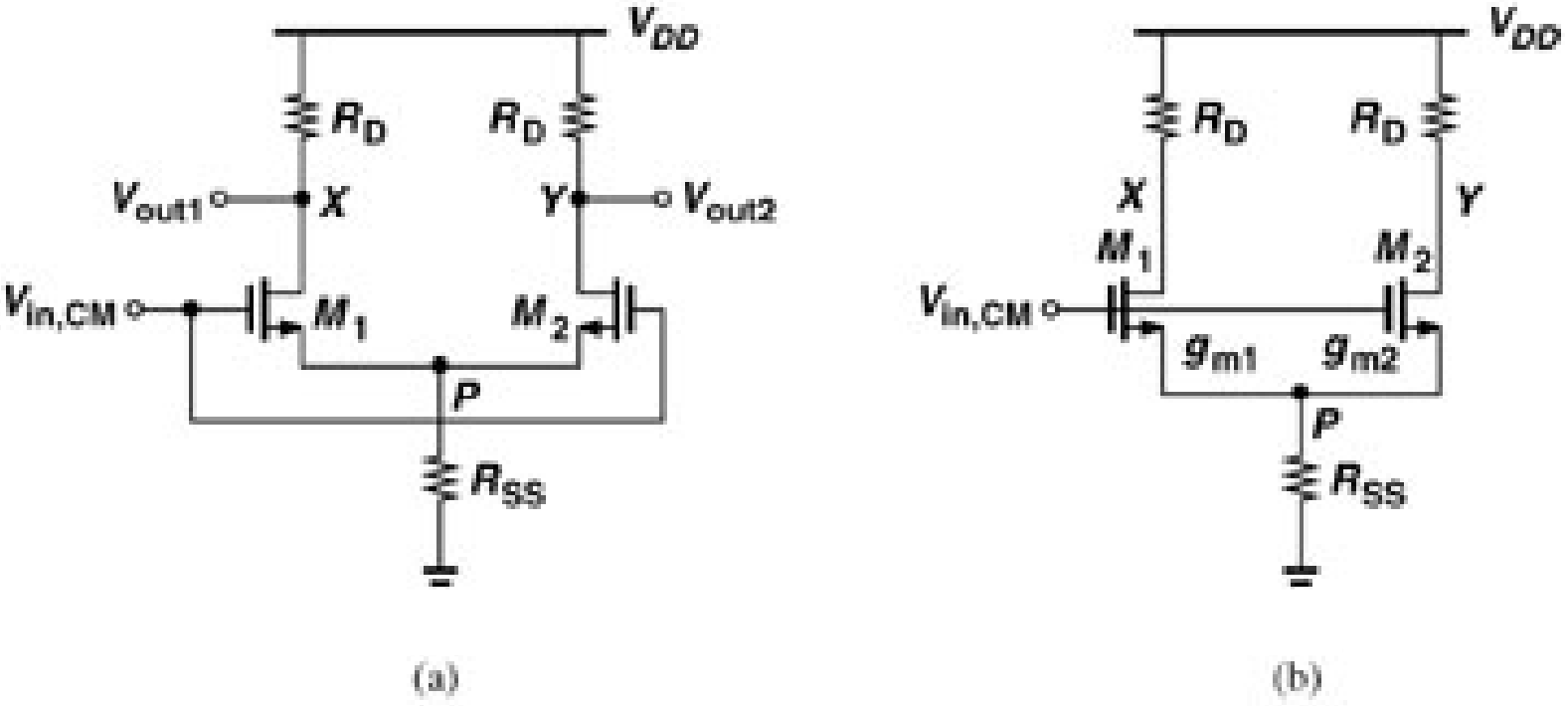
$$(g_{m1} + g_{m2})(V_{in,CM} - V_P)R_{SS} \overset{(a)}{=} \overset{(b)}{V_P}$$

$$\Rightarrow V_P = \frac{(g_{m1} + g_{m2})R_{SS}}{(g_{m1} + g_{m2})R_{SS} + 1} V_{in,CM}$$

$$V_X = -g_{m1}(V_{in,CM} - V_P)R_D$$

$$V_Y = -g_{m2}(V_{in,CM} - V_P)R_D$$

Mismatches in W/L, V_{TH} and other transistor parameters all translate to mismatches in g_m



$$A_{V,CM-DM} = \frac{V_X - V_Y}{V_{in,CM}} = -\frac{g_{m1} - g_{m2}}{(g_{m1} + g_{m2})R_{SS} + 1} R_D$$

Common-Mode Gains

- We have seen two types of common-mode gain:
- $A_{V,CM}$: Single-ended output due to CM signal.
- $A_{V,CM-DM}$: Differential output due to CM signal.

$$A_{V,CM} = \frac{V_X}{V_{in,CM}} = \frac{V_Y}{V_{in,CM}}$$

$$A_{V,CM-DM} = \frac{V_X - V_Y}{V_{in,CM}}$$

Common-Mode Rejection Ratio (CMRR) Definitions

$$CMRR = CMRR_{SE} = \left| \frac{A_{DM}}{A_{CM}} \right|$$

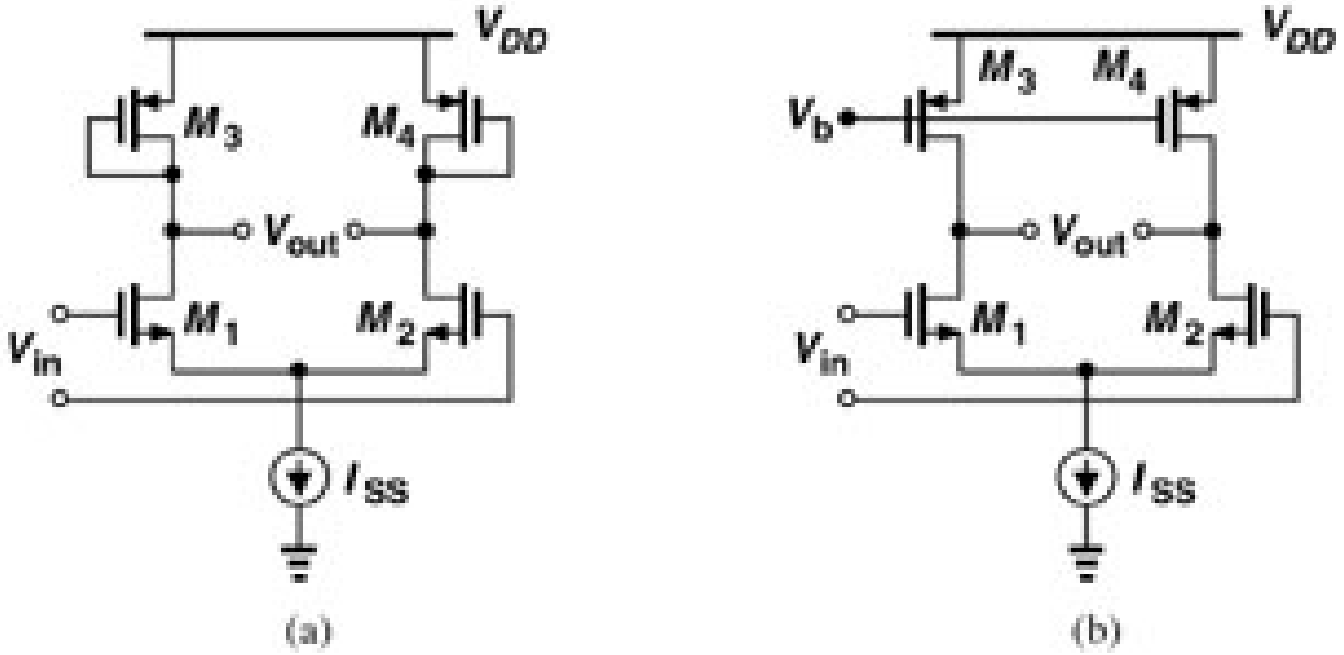
$$CMRR = CMRR_{diff} = \left| \frac{A_{DM}}{A_{CM-DM}} \right|$$

In both cases we want CMRR to be as large as possible, and it translates into small matching errors and R_{SS} as large as possible

CMOS Differential Amplifiers

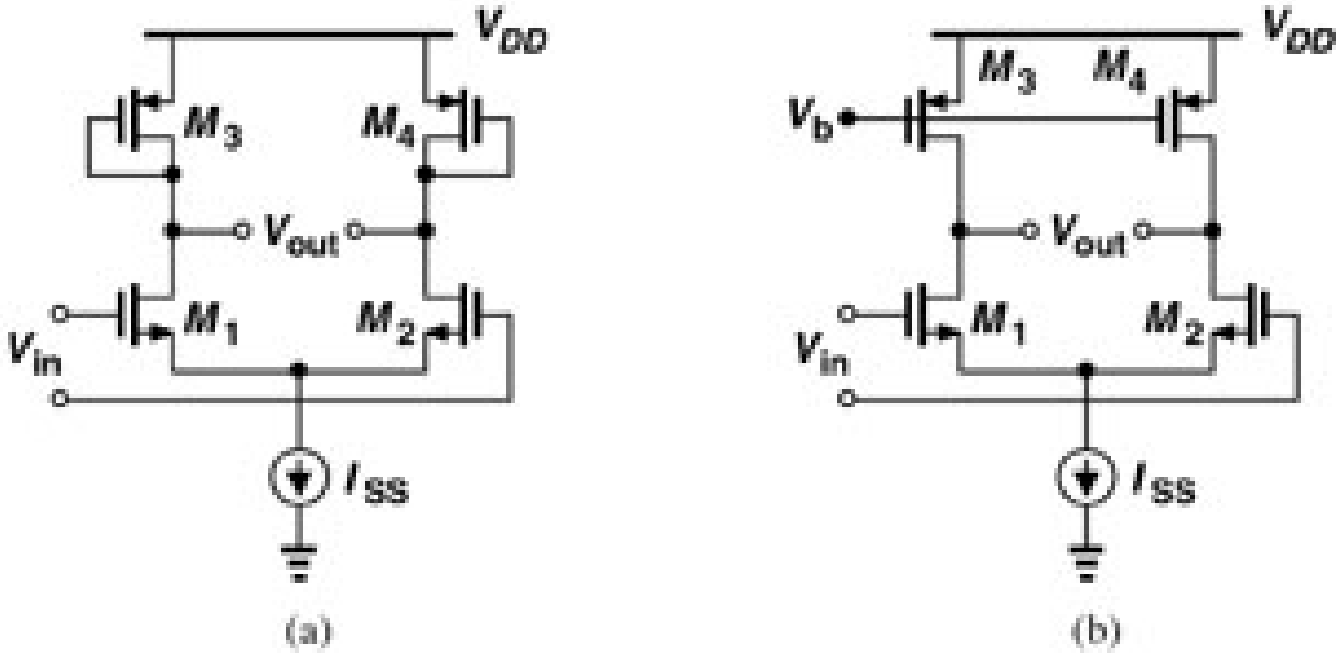
MOS Loads – L18

MOS Loads



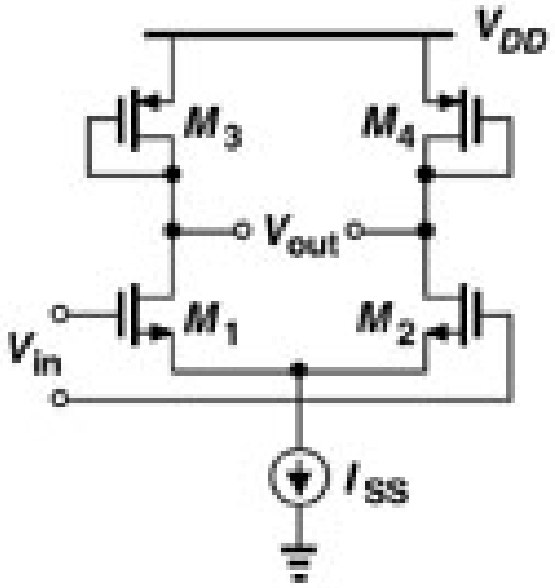
- (a) Diode-connected load
- (b) Current-Source load

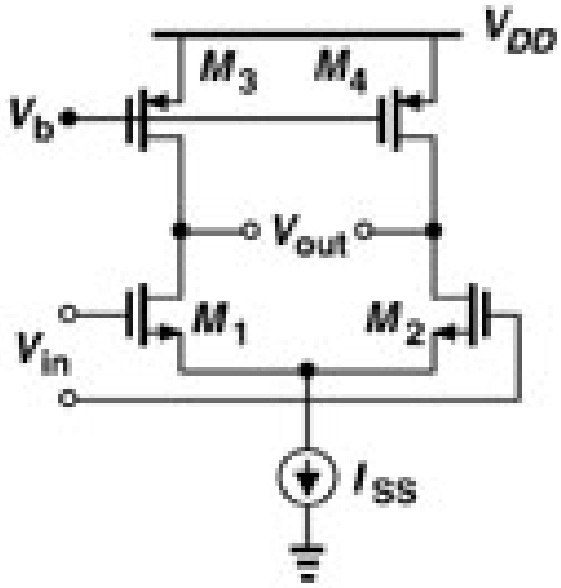
MOS Loads: Analysis Method



- Differential Analysis: Use half-circuit method, with source node at virtual ground.
- Common-Mode Analysis: Again use half-circuit method, with appropriate accommodation for parallel transistors, and for R_{SS}.

MOS Loads: Differential Gain Formulas





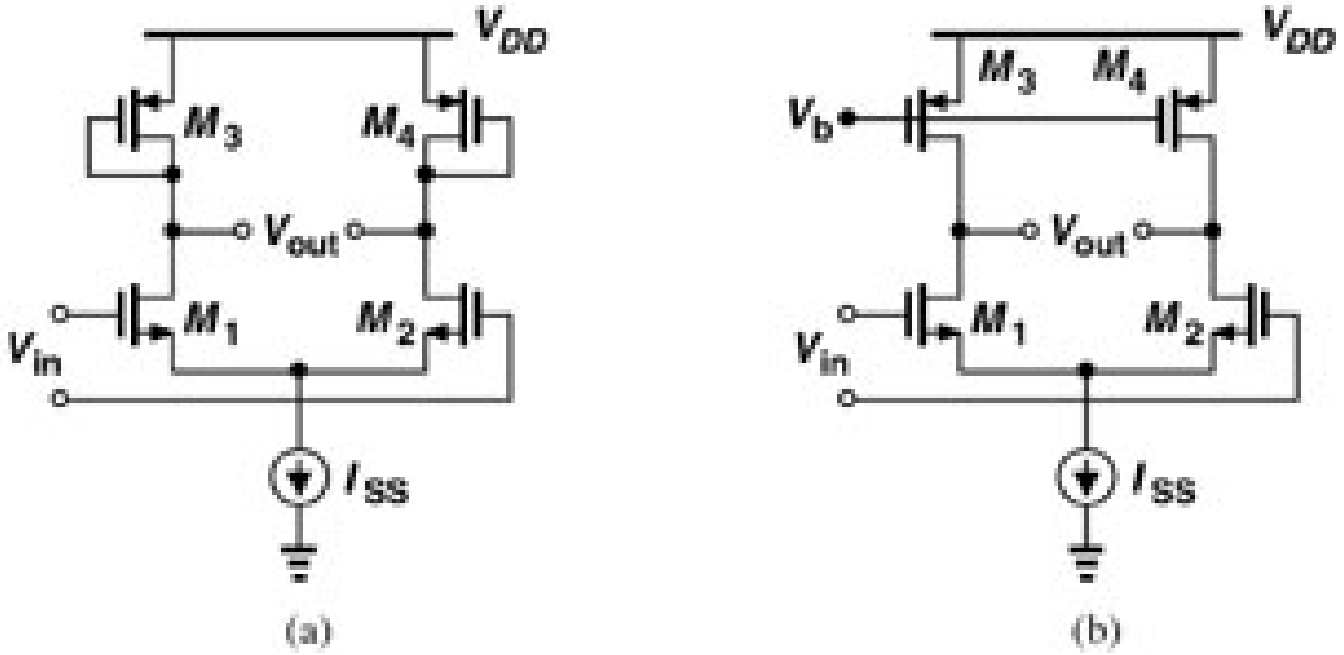
(b)

$$A_{V,diff} = -g_{mN}(g_{mP}^{-1} \parallel r_{oN} \parallel r_{oP})$$

$$\approx -\frac{g_{mN}}{g_{mP}} = -\sqrt{\frac{\mu_n (W/L)_N}{\mu_p (W/L)_P}}$$

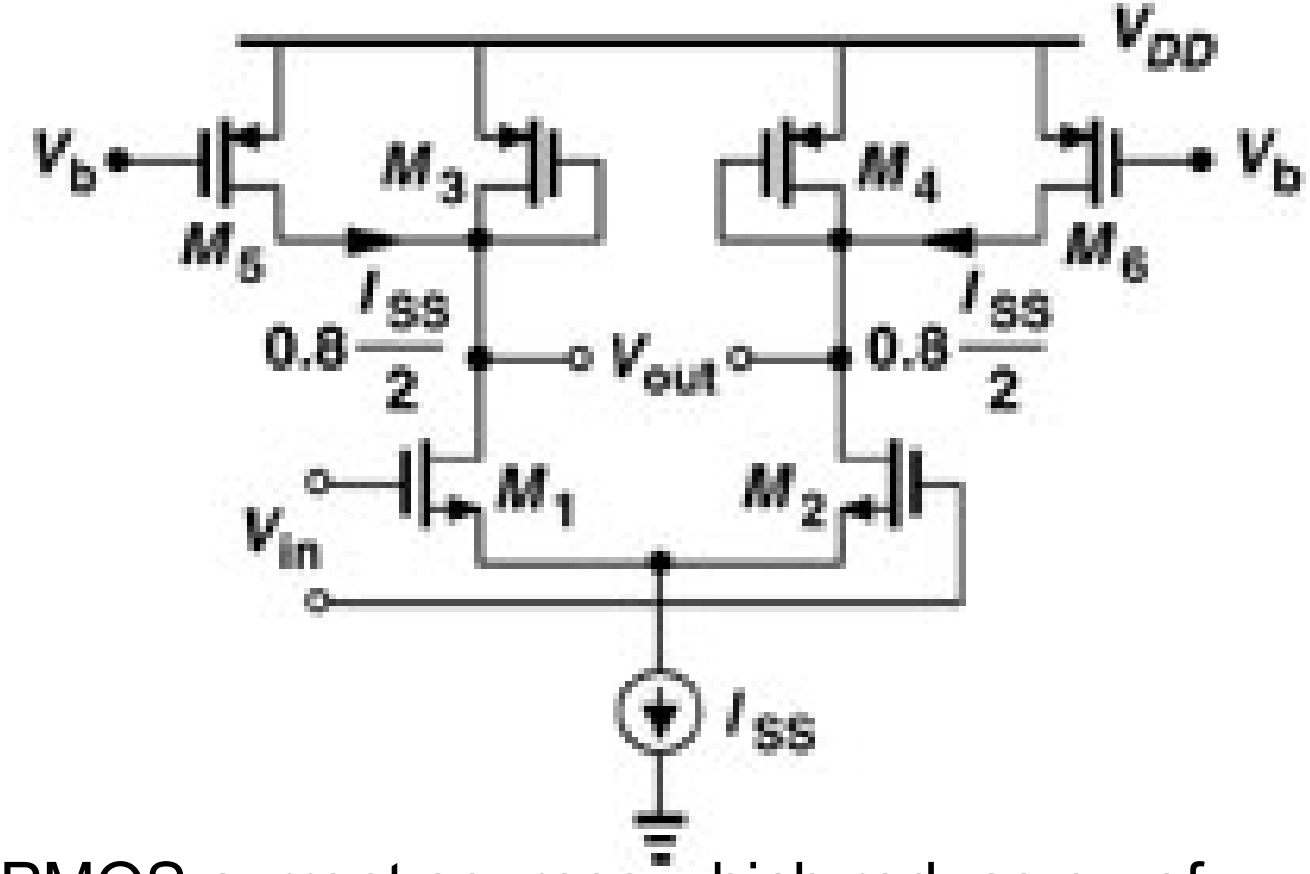
$$A_{V,diff} = -g_{mN}(r_{oN} \parallel r_{oP})$$

Problems with Diode-connected MOS Loads



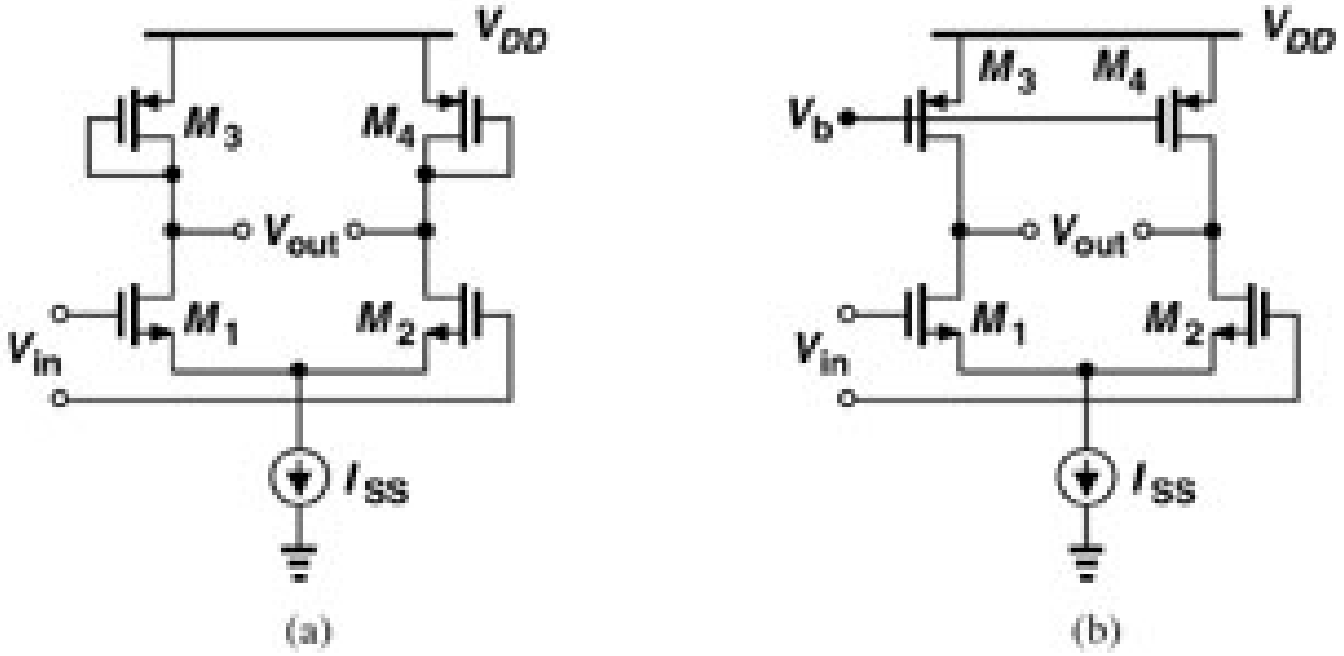
- Tradeoff among output voltage swing, voltage gain and CM input range:
- In order to achieve high gain, $(W/L)_P$ must be decrease, thereby increasing $|V_{GSP}-V_{THP}|$ and lowering the CM level at nodes X and Y.

Overcoming Diode-connected Load swing problem for higher gains:



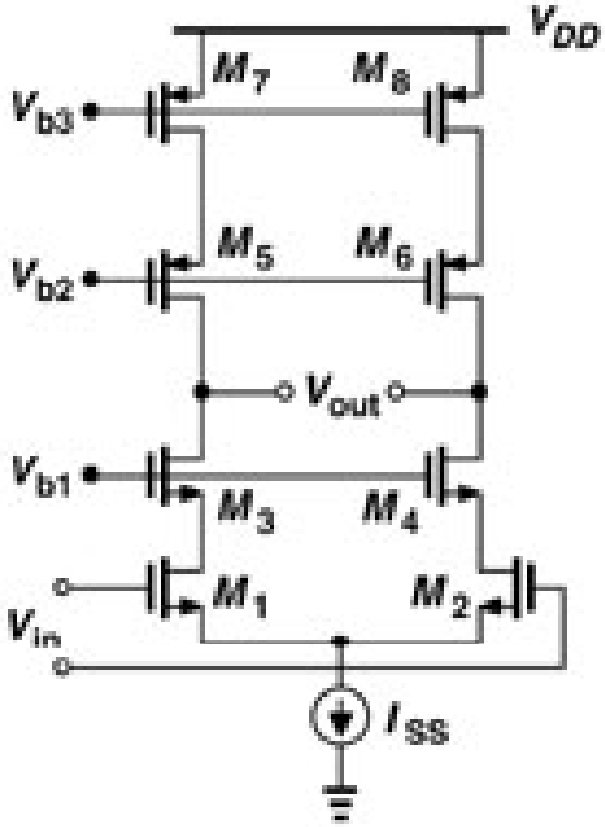
Use PMOS current sources which reduce g_m of diode-connected MOS, instead of lowering $(W/L)_P$ of load. Gain can be increased by factor of 5.

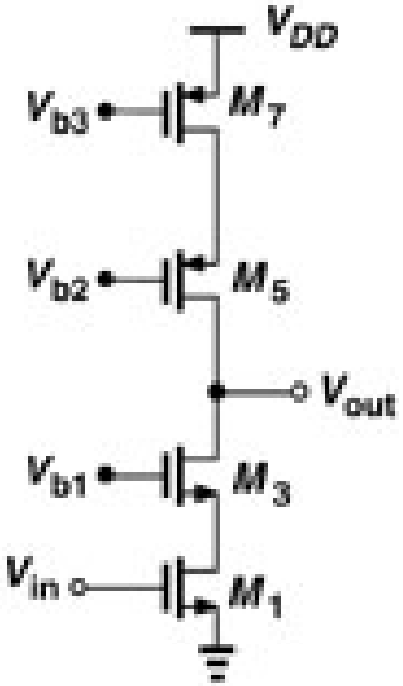
Problems with Current-Source MOS Loads



- In sub-micron technologies, it's hard to obtain differential gains higher than 10-20.

Solution to low-gain problem: Cascoding



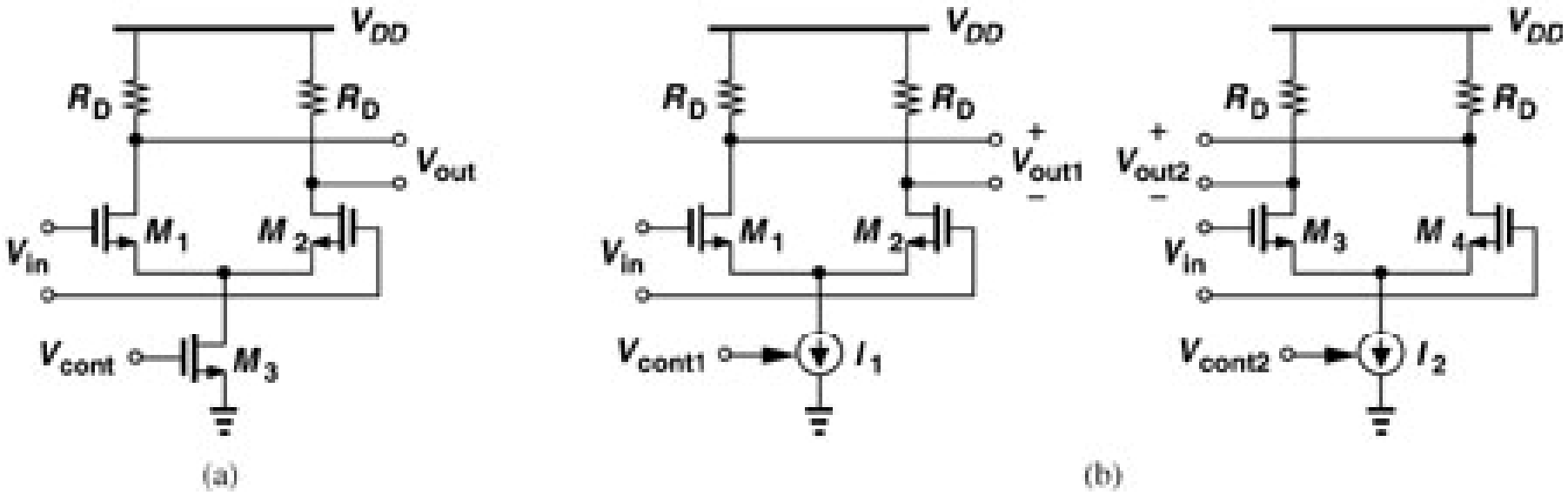


$$A_{V,diff} \approx g_{m1}[(g_{m3}r_{o3}r_{o1}) \| (g_{m5}r_{o5}r_{o7})]$$

CMOS Differential Amplifiers

Gilbert Cell-L19

Can we create a differential amplifier with voltage-controlled differential gain?



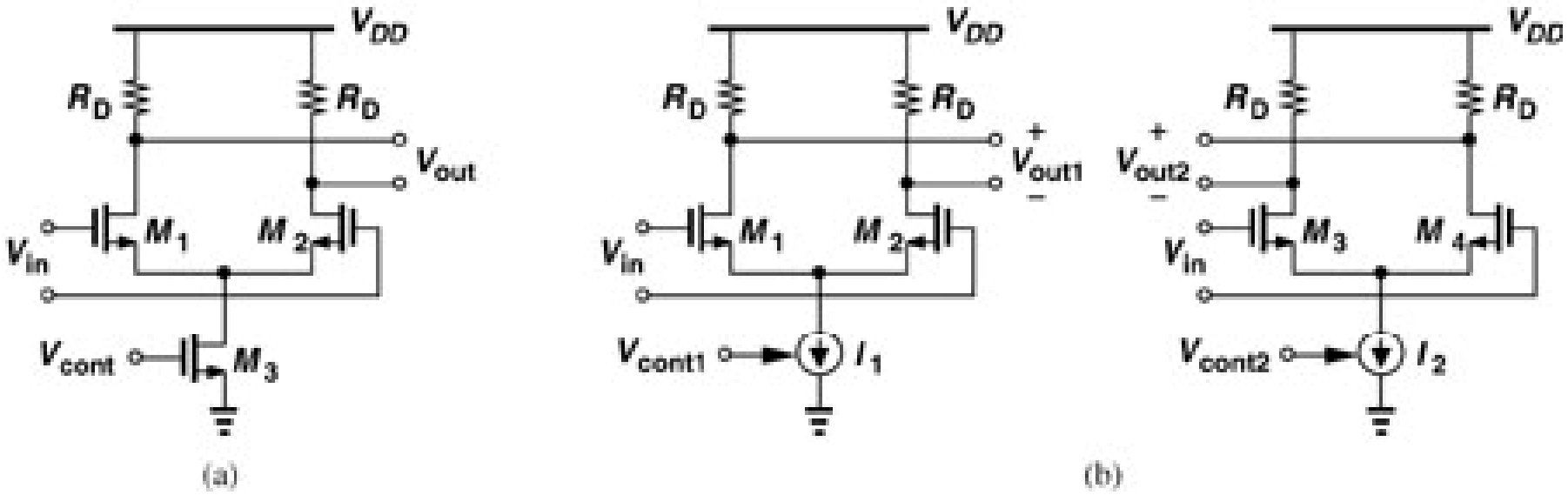
(a)is a VGA (Variable-Gain Amplifier). V_{cont} determines I_{ss}, which determines the differential gain.

Gain may be varied from 0 to some maximum value.

Can we create a differential amplifier with voltage-controlled differential gain?

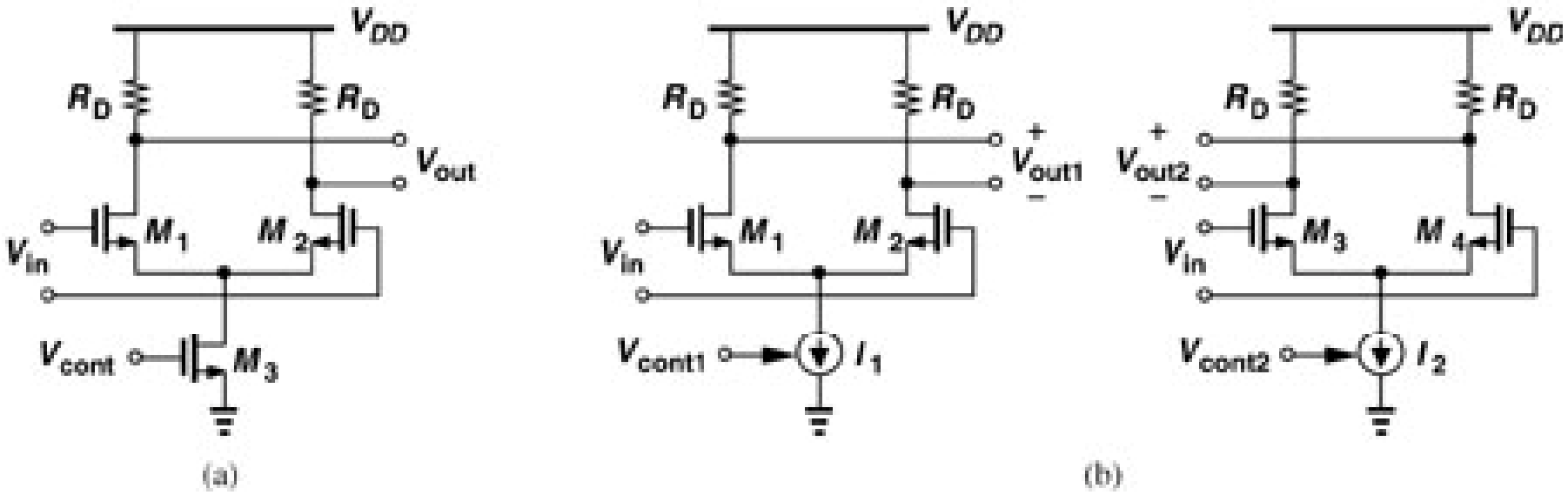
What do we do if we want to vary the gain continuously from some negative value to some positive value?

Can we create a differential amplifier with voltage-controlled differential gain?



In circuits (b) the two amplifiers have opposite differential gain simply by interchanging the order of output subtraction)

Can we create a differential amplifier with voltage-controlled differential gain?

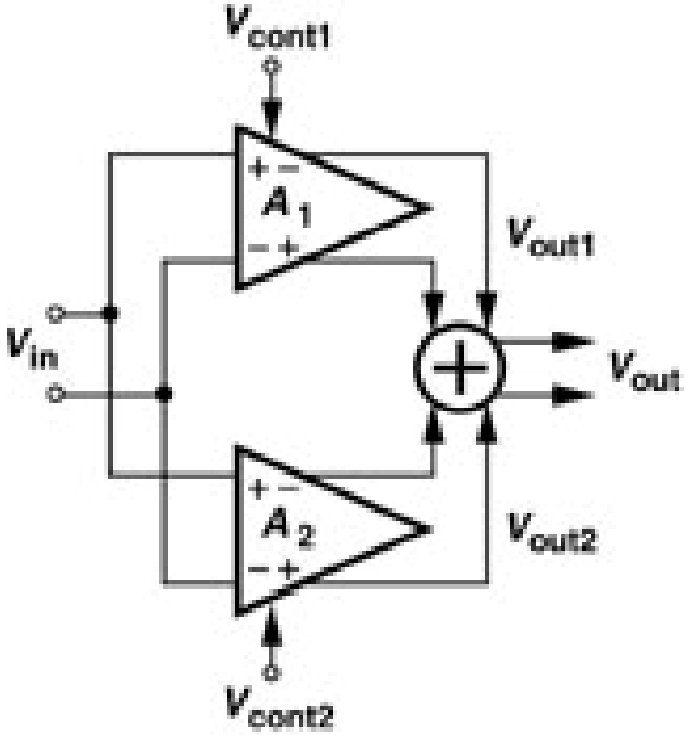


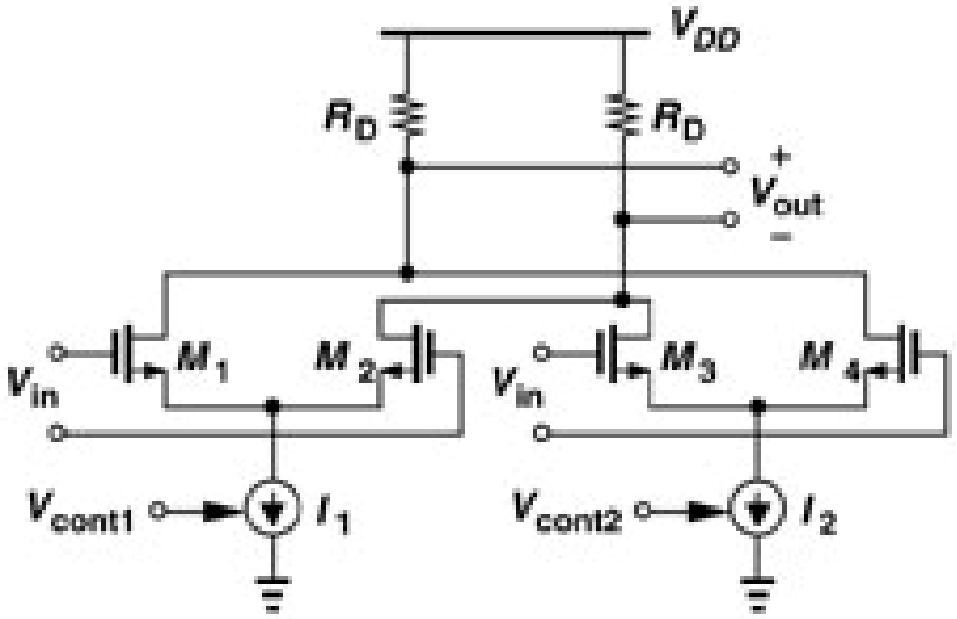
If $I_1=I_2$ then $V_{out,1}/V_{in}= -g_mR_D = - V_{out,2}/V_{in}$

If we vary I_1 and I_2 in opposite directions, the gains will follow along these directions.

How should we combine the two differential outputs?

How to combine the differential outputs?

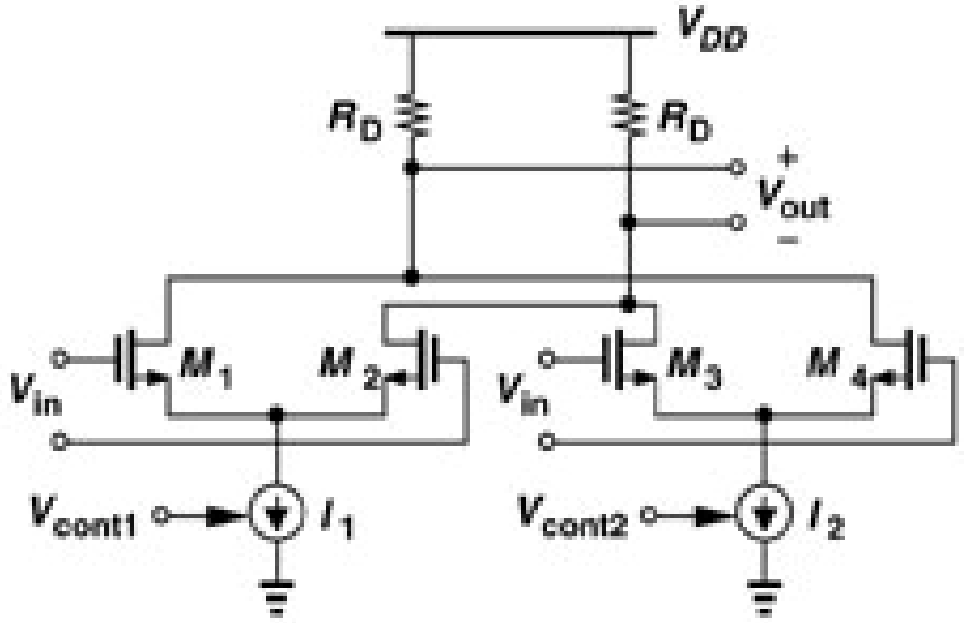




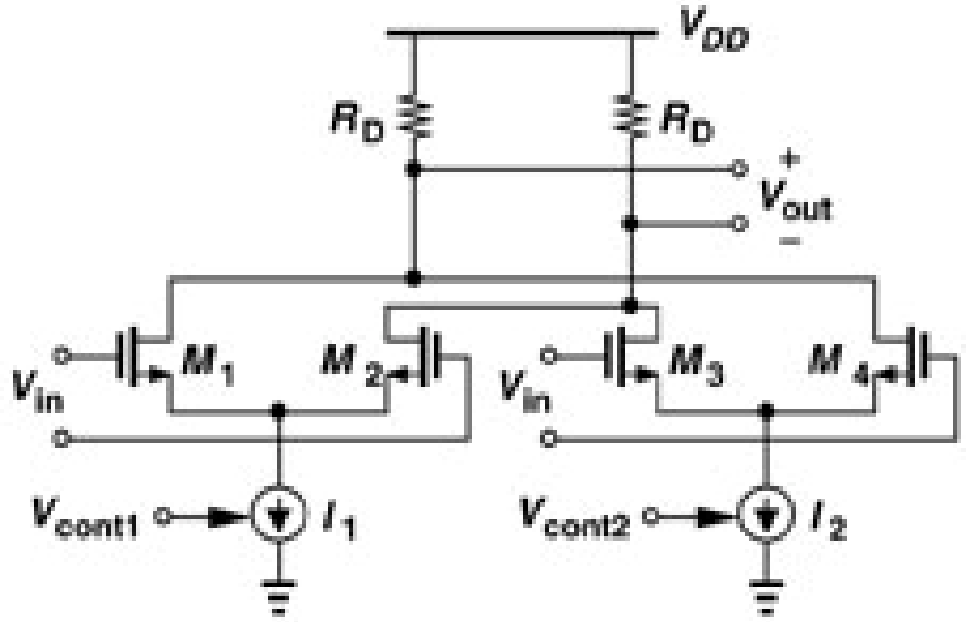
On the left, we conceptually see the two voltages ADDED UP.

Gains A_1 and A_2 are voltage controlled.

How to combine the differential outputs?
Math will show the implementation method.



Does it work as intended? Can gain be varied positively as well as negatively?

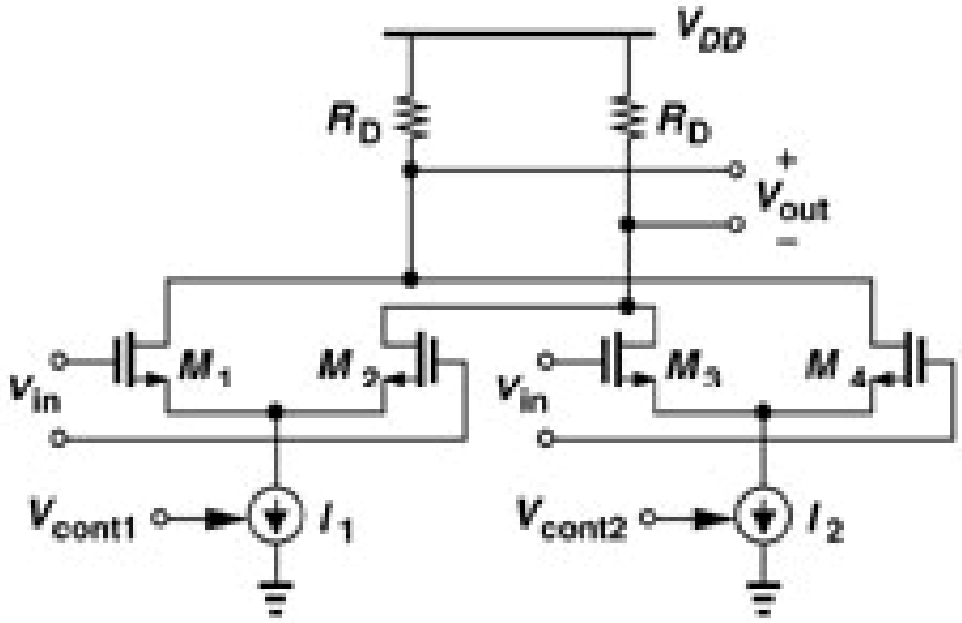


If $I_1=0$ then $V_{out}=g_mR_D$.

If $I_2=0$ then $V_{out}= -g_mR_D$.

If $I_1=I_2$ then $V_{out}=0$!!

Next phase in the conceptual development: Do we really need two separate control signals??



Recall the basic structure of a differential amplifier: The inputs difference cause one of the MOS currents to go up, and at the same time the current of the opposite MOS goes down by the same amount → Let I_1 , I_2 come from diff. amp.

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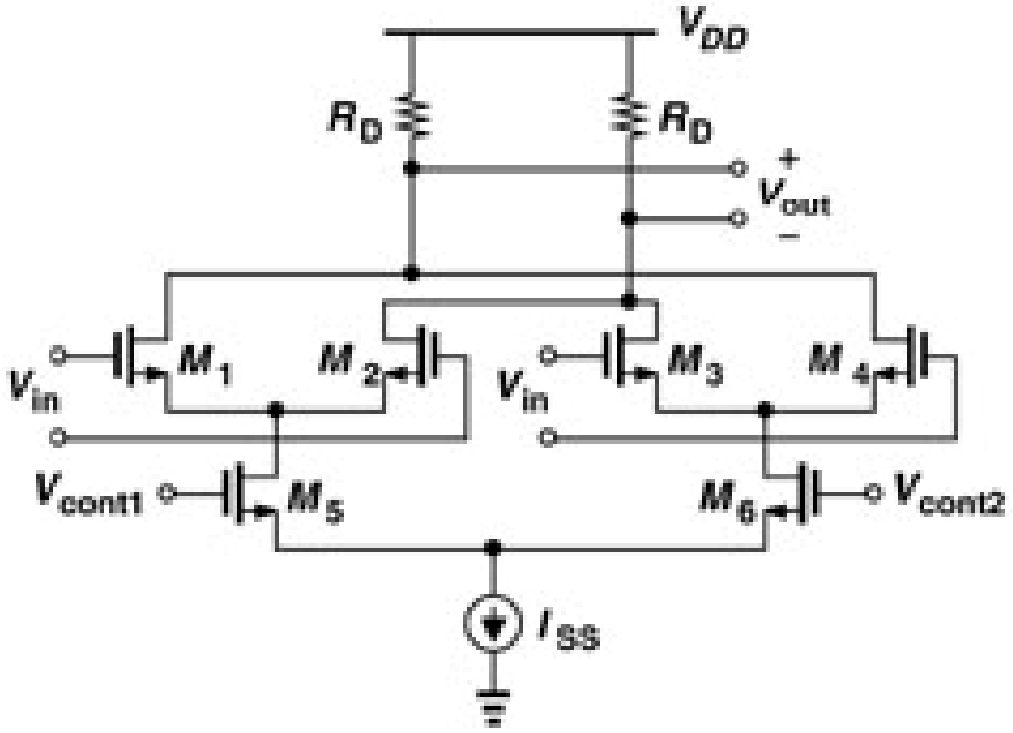
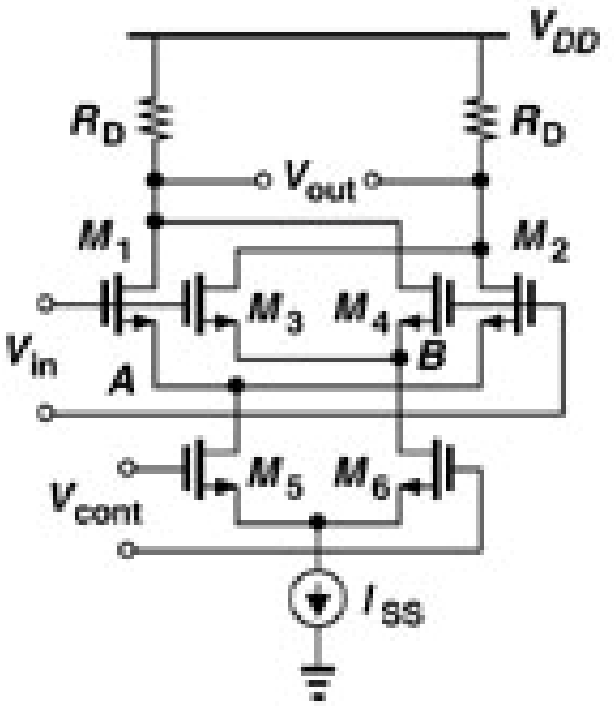
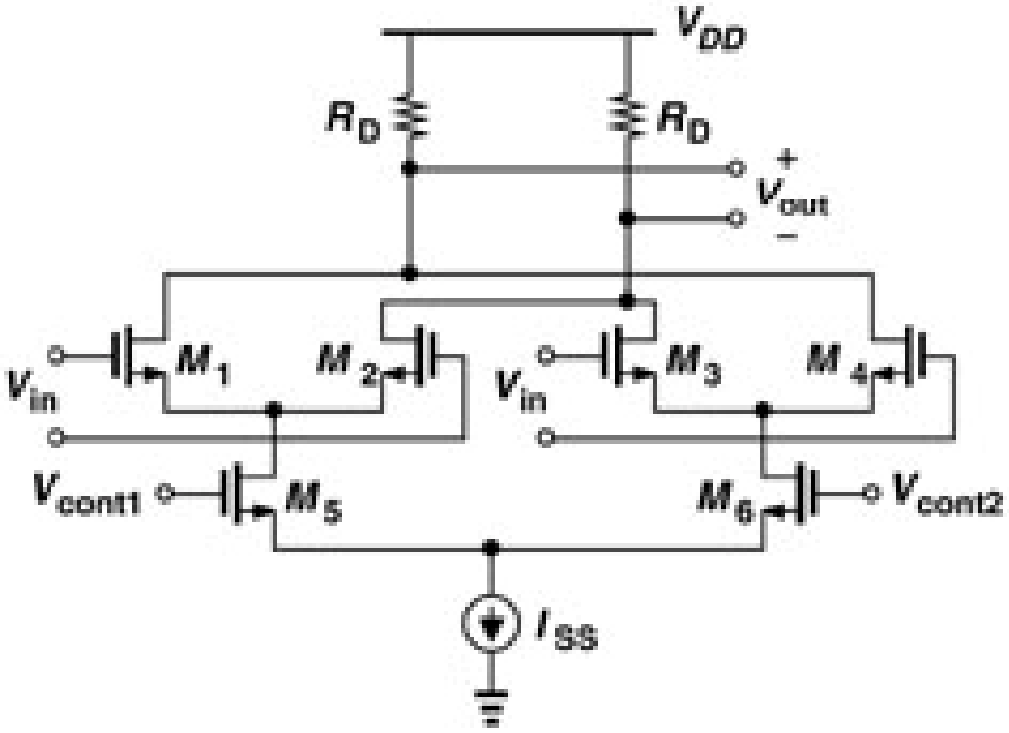
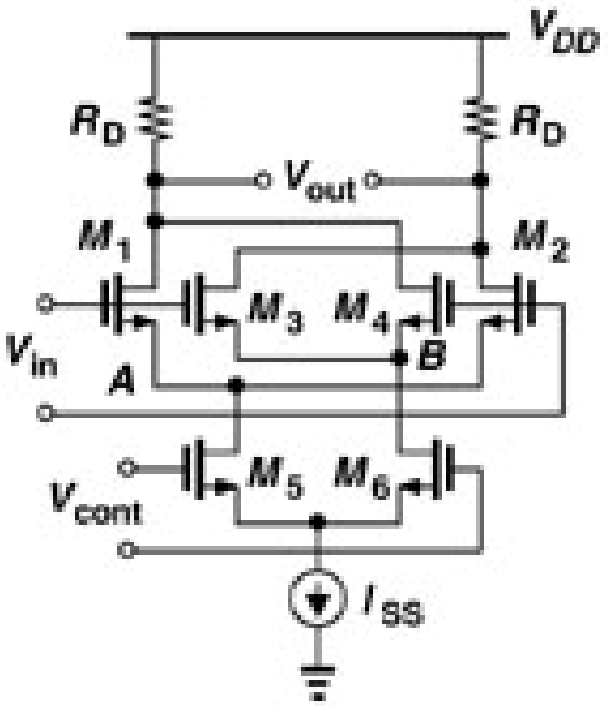




Left: If $|V_{cont1} - V_{cont2}|$ is large we have "current stealing", and then gain is either most positive or most negative.

Gilbert Cell





Right: Actual Implementation

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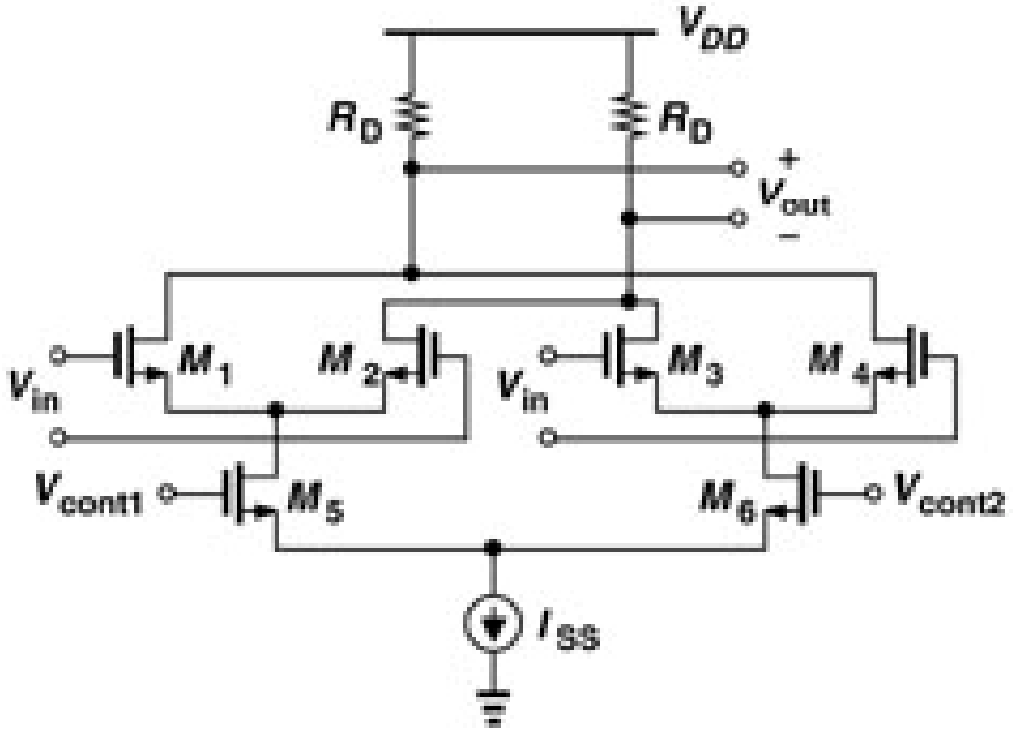

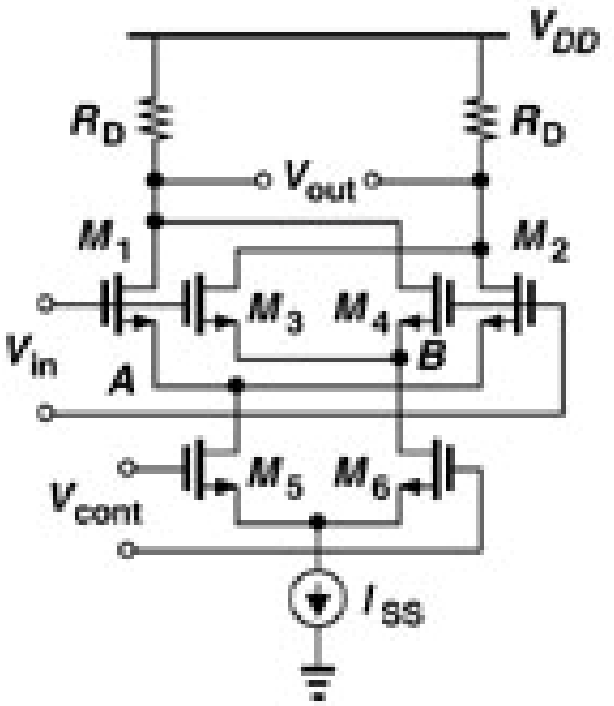

$$V_{OUT} = kV_{in}V_{cont}$$

Applications of Gilbert Cell

- Analog Multiplier
  - Mixer
  - Phase Detector
  - AM Modulation
- VGA: Variable-gain amplifier
  - AGC (Automatic Gain Control)

It’s a versatile general-purpose tool

Can switch input and control signals!