

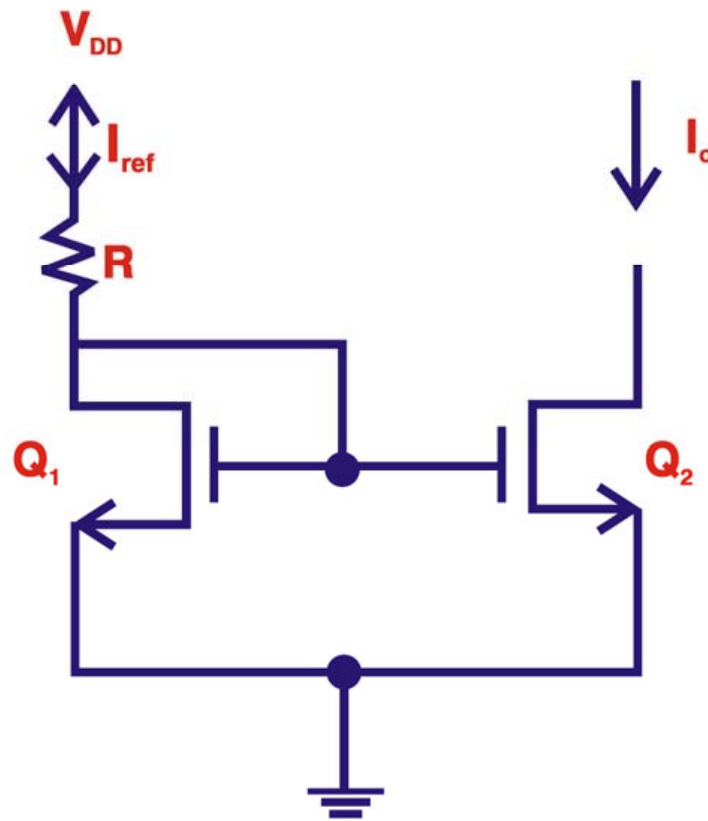
Chapter 5

Passive and Active Current Mirrors

MOSFET Current Mirror Current Sources

Basic Concepts

Let us study the most basic Current Mirror circuit, consisting of two matching MOSFET transistors connected back-to-back, such that both have the same Gate-to-Source voltage:



Given:

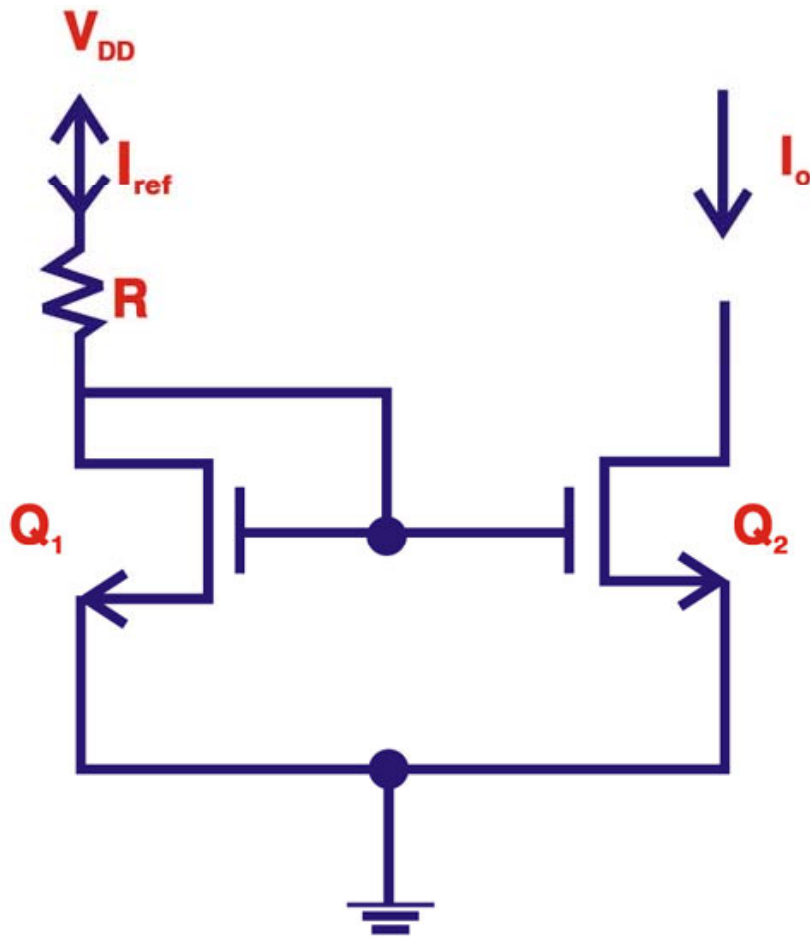
(*) The two enhancement-type NMOS transistors have matching features, as follows: $V_{TH,1} = V_{TH,2}$, $k_{n,1}' = k_{n,2}'$, $\lambda_1 = \lambda_2 = 0$

(*) “By structure” we have that $V_{GS,1} = V_{GS,2}$

(*) Typically the supply V_{DD} , resistor R and a desired reference current I_{ref} are all given.

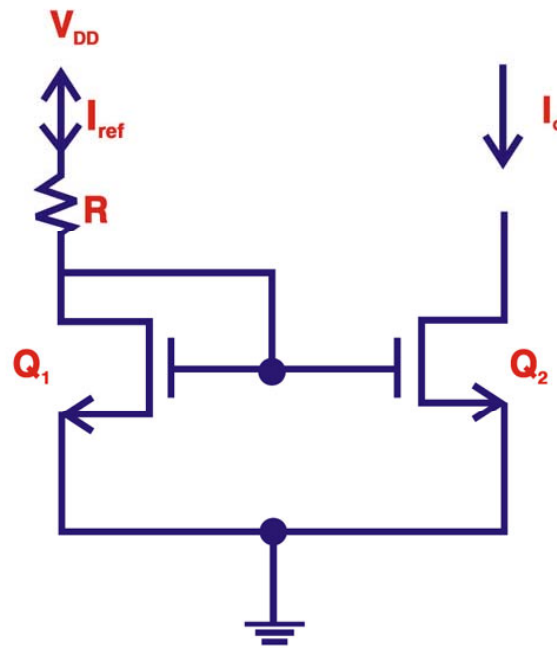
(*) The ratio $(W/L)_1$ is not necessarily equal to the ratio $(W/L)_2$

(*) “By structure” we have that $V_{GD,1} = 0$, and because the transistor is an enhancement-type, this guarantees that transistor 1 is always in Saturation Mode

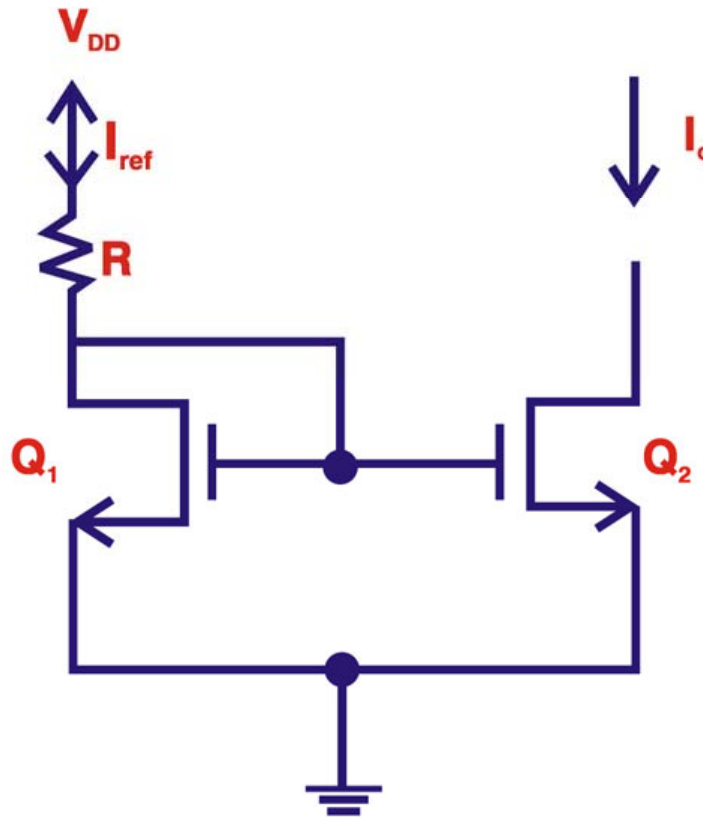


Need: Using the transistors geometries $(W/L)_1$ and $(W/L)_2$ as design parameters, we want to create a DC current I_o , as long as transistor Q_2 is in Saturation Mode

The Drain of transistor Q_2 is connected to a load circuit, not necessarily a resistor. The load circuit typically involves one or more additional MOSFET transistors. Depending on the load, transistor Q_2 may be in any of three modes: Saturation, Triode or Cutoff. Of course, only when it is in Saturation it will work as originally planned (a DC current source)



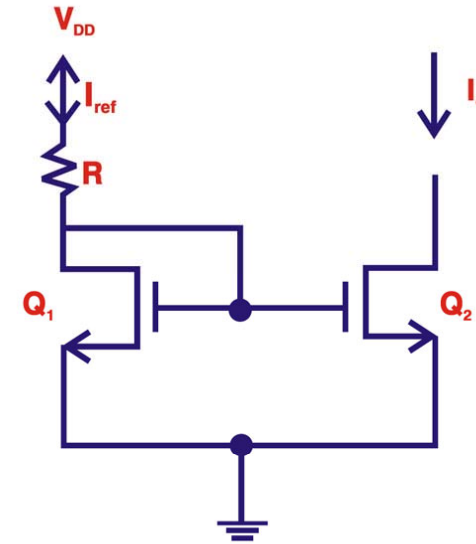
The current I_o always goes away from the load circuit and into Q_2 . Such a DC current source is said to be a sink.



Design of a Current Mirror DC Sink

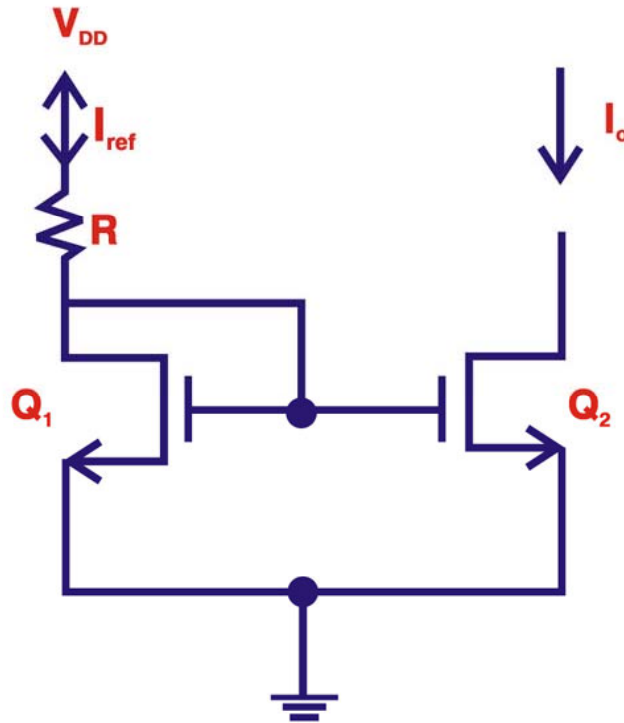
We shall look first at Q_1 :

$$I_{D,1} = I_{ref} = \frac{1}{2} k_{n,1} \left(\frac{W}{L}\right)_1 (V_{GS,1} - V_{TH,1})^2$$
$$= \frac{V_{DD} - V_{GS,1}}{R}$$



So, indeed if I_{ref} is specified and V_{DD} and R are given, then by the right-hand term the needed voltage $V_{GS,1}$ is specified. Then, using the middle term, need to solve for $(W/L)_1$.

Example 1:



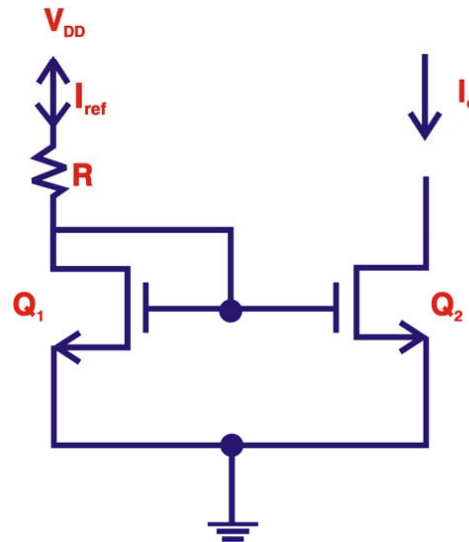
Let $V_{DD} = 5V$, $V_{TH,1} = 1V$, $k_{n,1}' = 20\mu A/V^2$ and $R = 1K\Omega$.
What should be $(W/L)_1$ needed for creating $I_{ref} = 1mA$?

Solution of Example 1:

$$I_{ref} = 1mA = \frac{V_{DD} - V_{GS,1}}{R} = \frac{5 - V_{GS,1}}{1} \Rightarrow V_{GS,1} = 4V$$

$$\Rightarrow I_{ref} = 1mA = \frac{1}{2} k_{n,1} \left(\frac{W}{L}\right)_1 (V_{GS,1} - V_{TH,1})^2 = \frac{1}{2} \cdot 20 \cdot 10^{-3} \left(\frac{W}{L}\right)_1 (4 - 1)^2 \Rightarrow$$

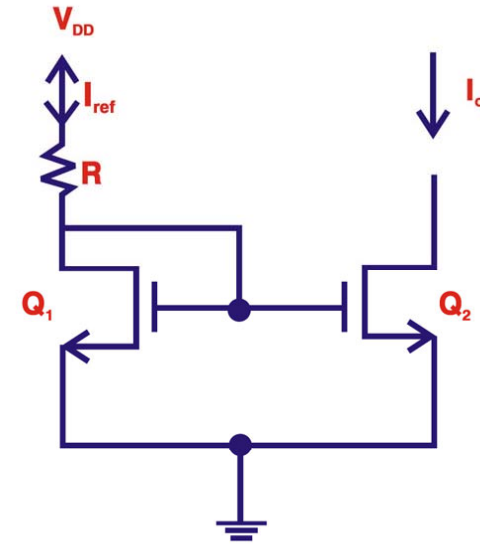
$$\Rightarrow \left(\frac{W}{L}\right)_1 = 11.11$$



Let us now focus our attention on the "mirror" transistor Q_2 :

$$I_{D,2} = I_o = \frac{1}{2} k_{n,2} \left(\frac{W}{L} \right)_2 (V_{GS,2} - V_{TH,2})^2$$

$$I_{D,1} = I_{ref} = \frac{1}{2} k_{n,1} \left(\frac{W}{L} \right)_1 (V_{GS,1} - V_{TH,1})^2$$



We now divide the two equations and use all the given matching parameters of the two transistors.

$$\frac{I_o}{I_{ref}} = \frac{0.5k_{n,2}'\left(\frac{W}{L}\right)_2(V_{GS,2} - V_{TH,2})^2}{0.5k_{n,1}'\left(\frac{W}{L}\right)_1(V_{GS,1} - V_{TH,1})^2}$$

Obviously, many terms cancel out and we are left with the following simple design formula:

$$\frac{I_o}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

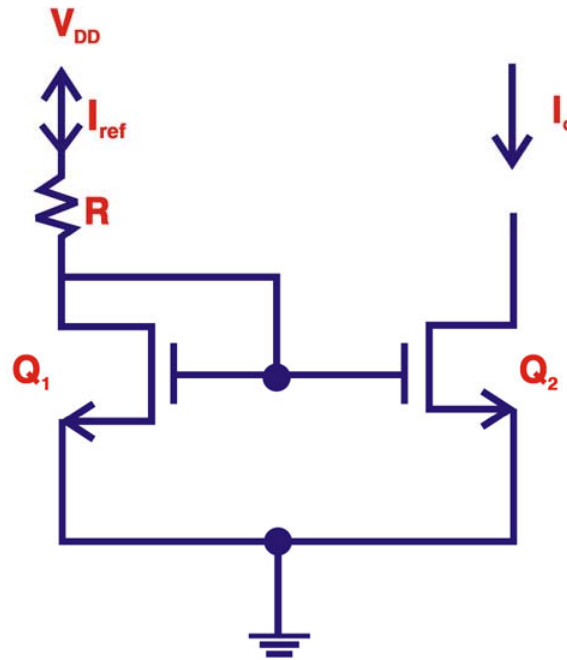
Example 2 (Follow-up to Example 1)

What should be $(W/L)_2$ if we want $I_o = 7\text{mA}$?

Solution

By Example 1 we have that $I_{\text{ref}} = 1\text{mA}$ and $(W/L)_1 = 11.11$.

Therefore:



$$\frac{I_o}{I_{\text{ref}}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \Rightarrow \frac{7\text{mA}}{1\text{mA}} = \frac{\left(\frac{W}{L}\right)_2}{11.11} \Rightarrow \left(\frac{W}{L}\right)_2 = 77.77$$

Question:

What do we do if we want to create a source DC current source, rather than a sink ?

[A "source" is when the current goes from the current source into the load circuit]

Answer:

If we build a current mirror current source using PMOS transistors (rather than NMOS) then the output DC current will be "sourced" and not "sunk".

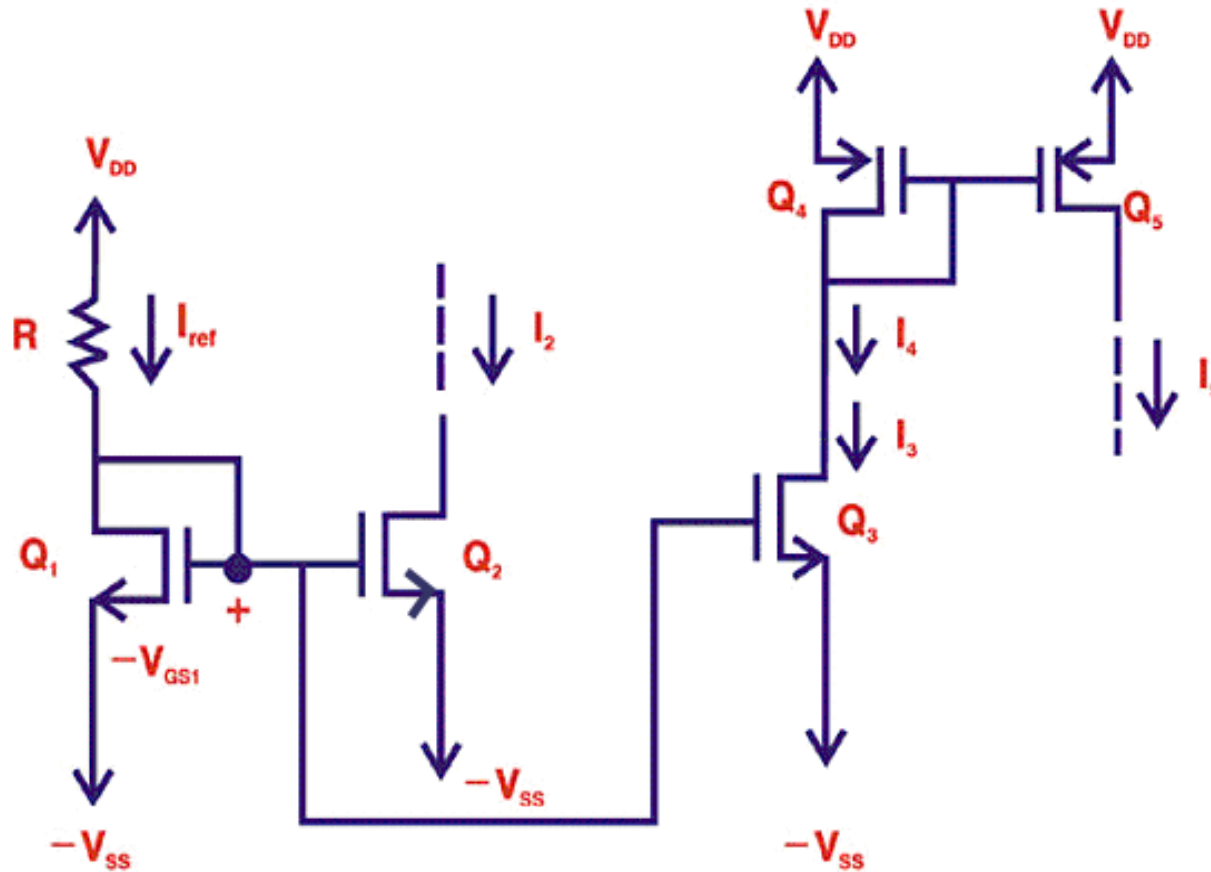
Question:

If we need to generate multiple different DC current sources and sinks,
what is the total number of resistors needed for the design?

Answer:

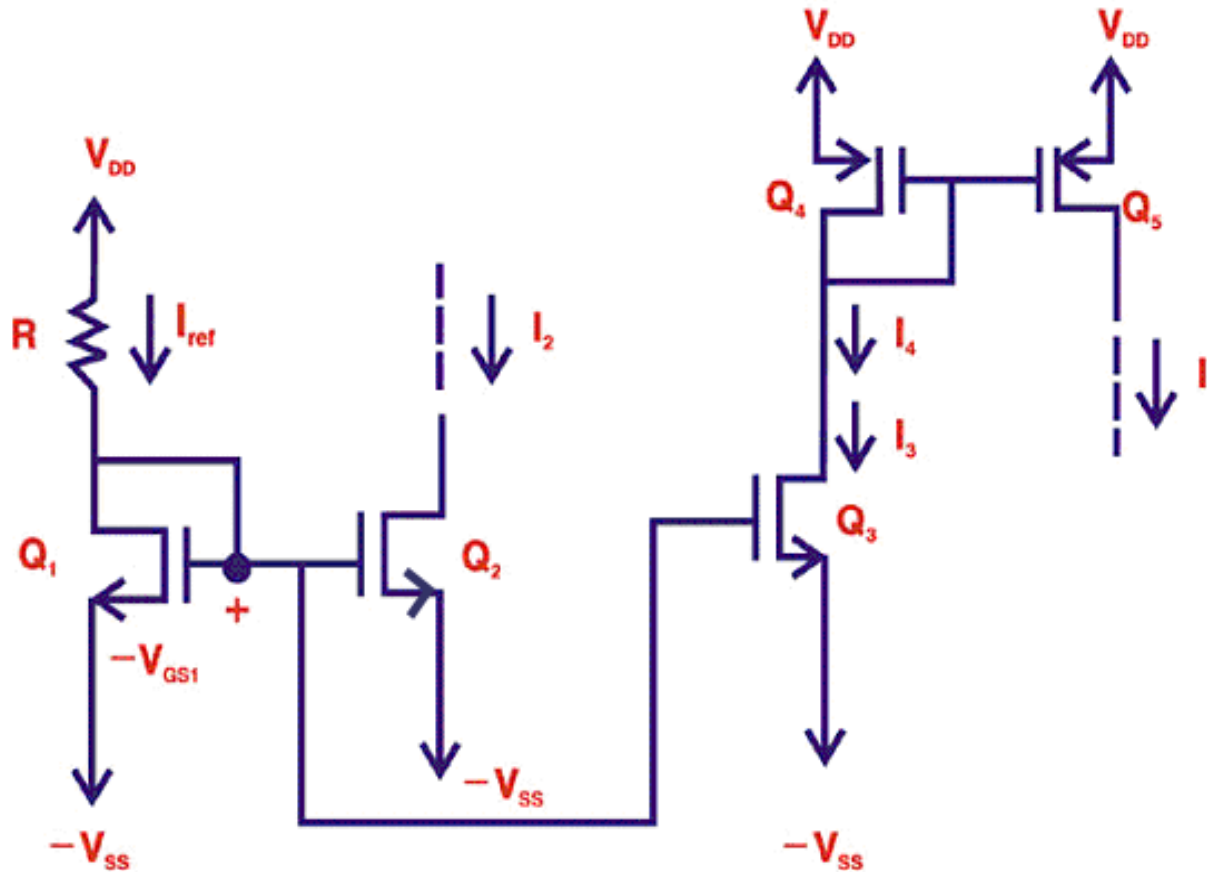
Just one resistor for the entire circuit!

Current Steering



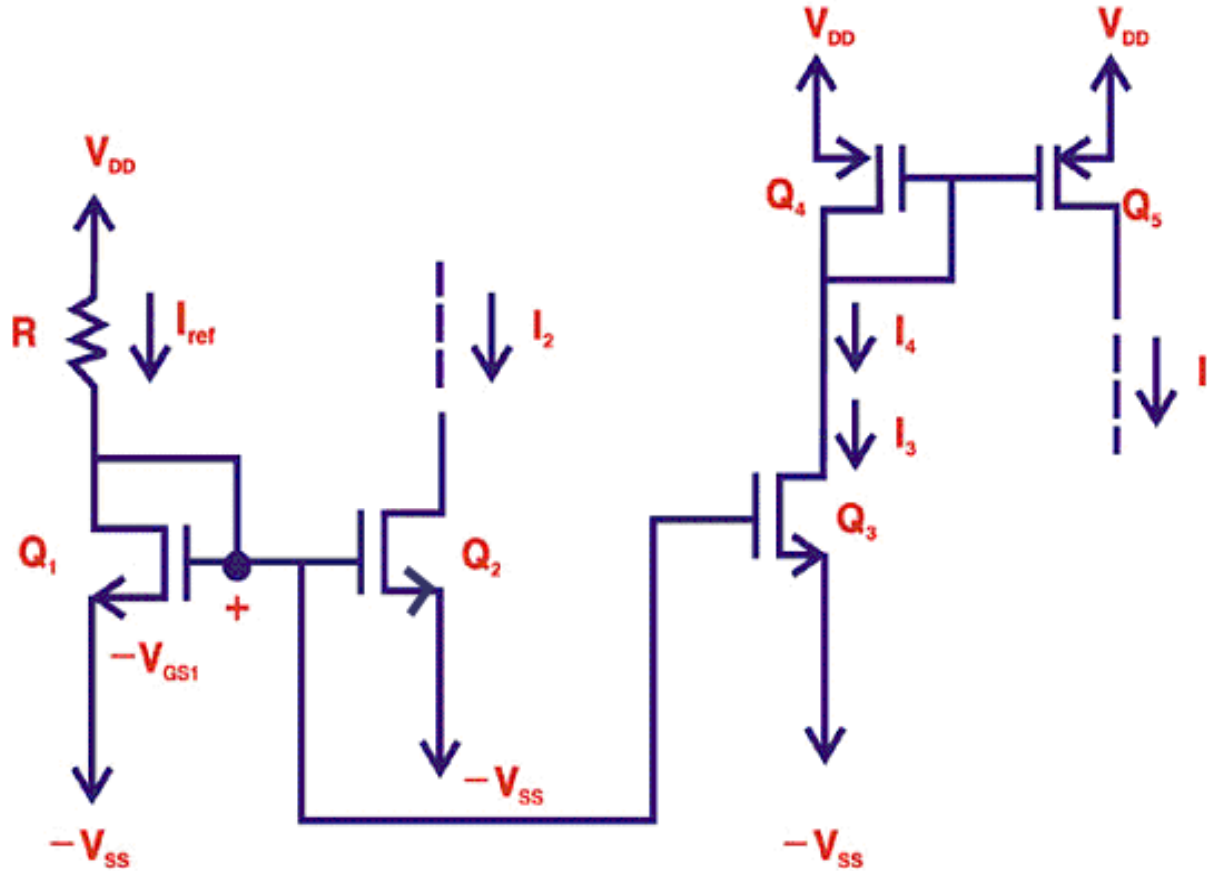
The use of a negative DC supply $-V_{SS}$ does not change the fact that, by-structure, both transistors, in every mirror pair, have the same V_{GS} voltage.

Recalculation of Reference Current



$$I_{D,1} = I_{ref} = \frac{1}{2} k_{n,1} \left(\frac{W}{L} \right)_1 (V_{GS,1} - V_{TH,1})^2 = \frac{V_{DD} - (-V_{SS} + V_{GS,1})}{R}$$

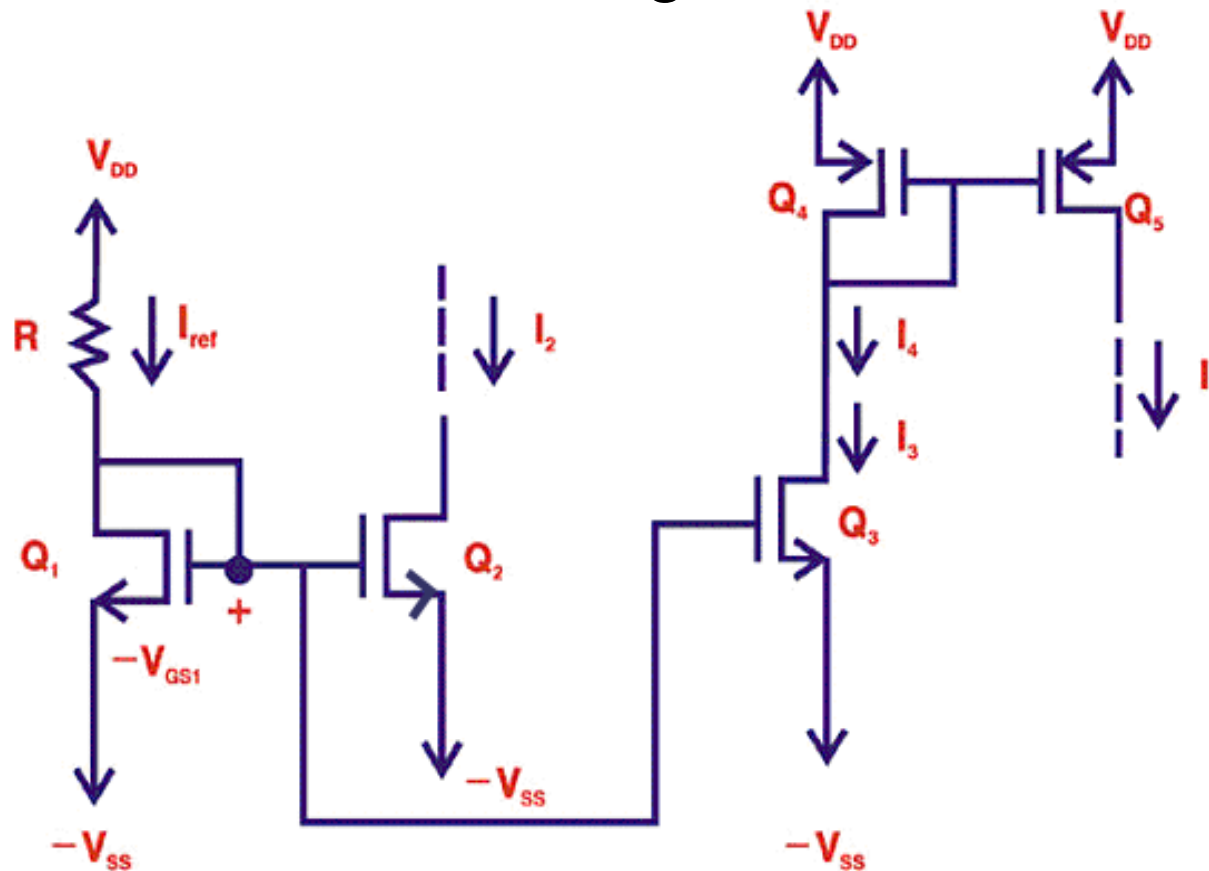
NMOS Current Mirror Sinks:



$$\frac{I_2}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}$$

$$\frac{I_3}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1}$$

Current Steering Mechanism:

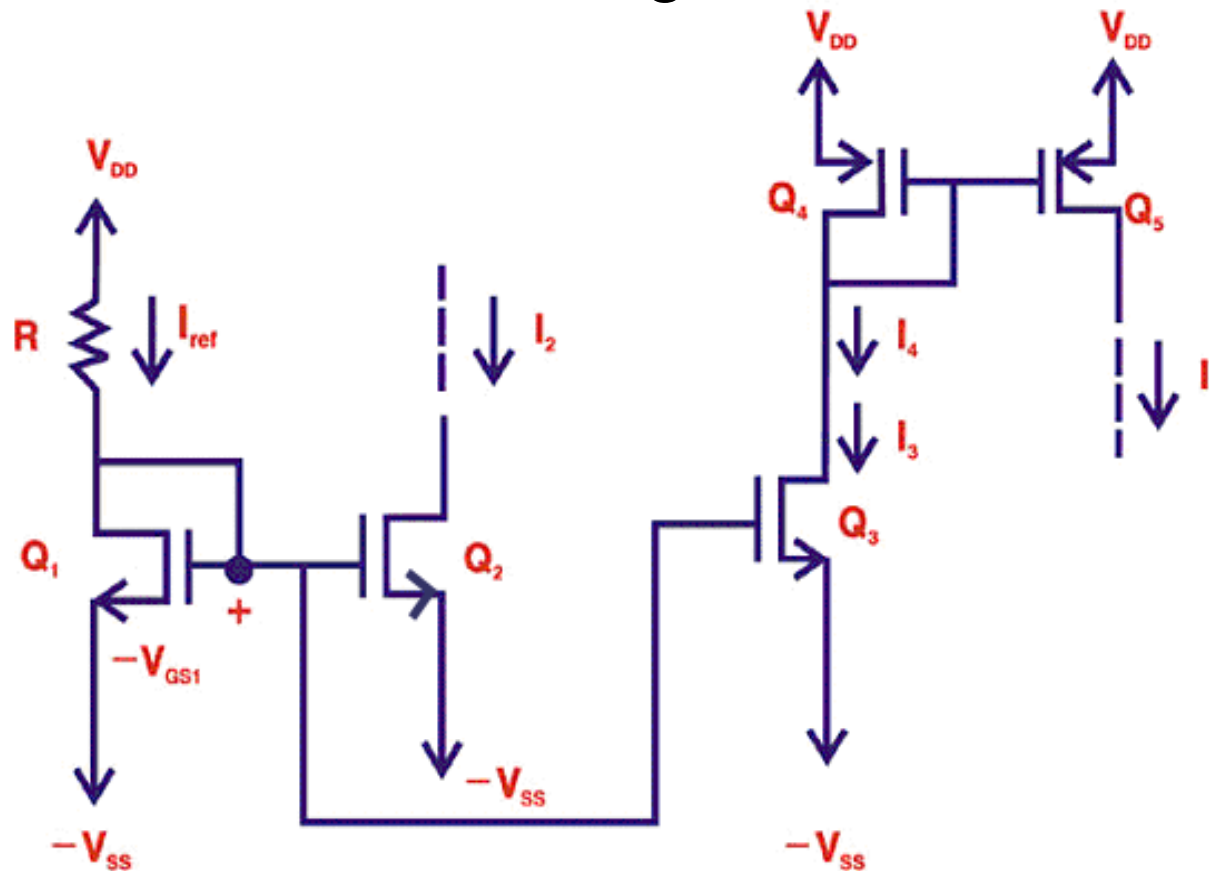


The Drain current of the NMOS transistor Q3 comes from the Drain of the PMOS transistor Q4.

$$I_4 = I_3$$

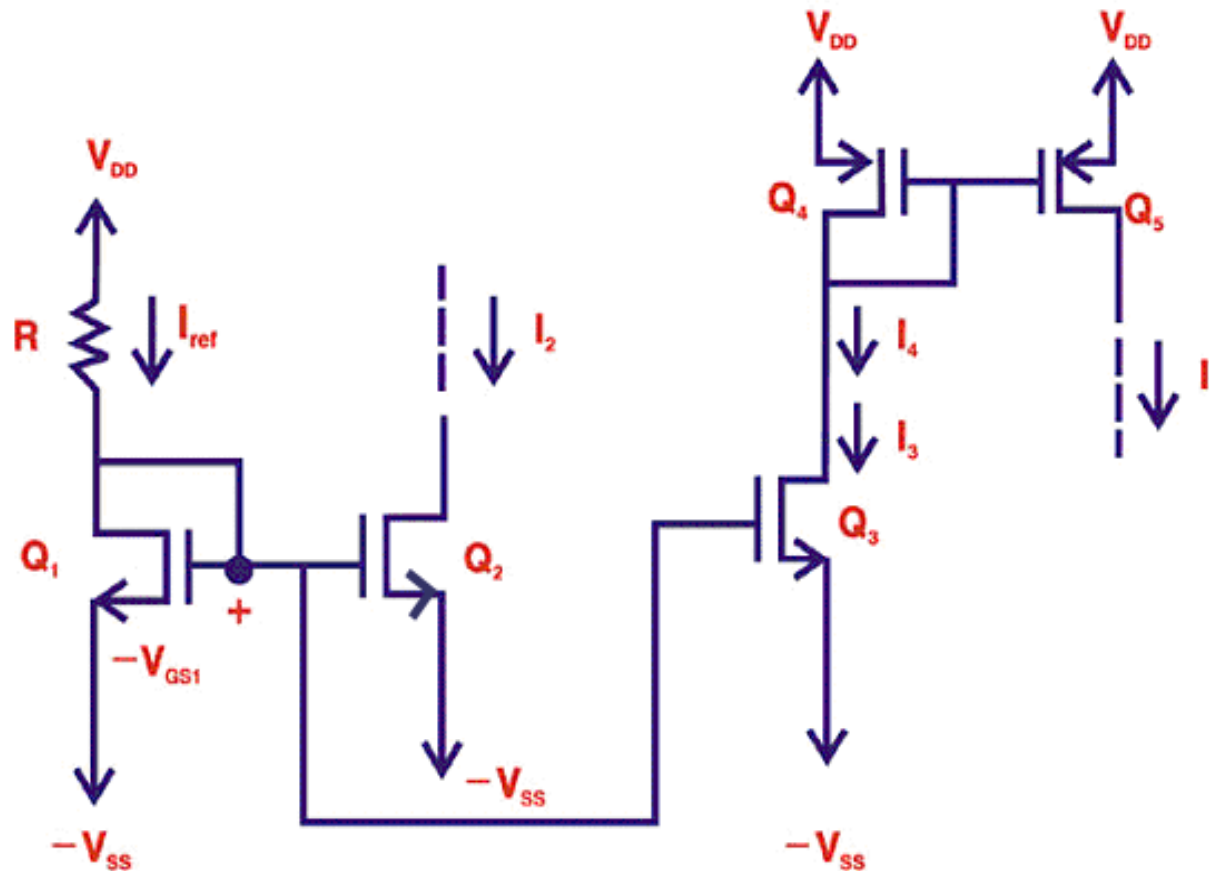
Can "steer" a current from NMOS current mirror to PMOS current mirror, or vice versa.

Current Steering Mechanism:



There is no need for the NMOS and PMOS to be matching: Only all the NMOS transistors must match among themselves, and the PMOS transistors must be mutually matching.

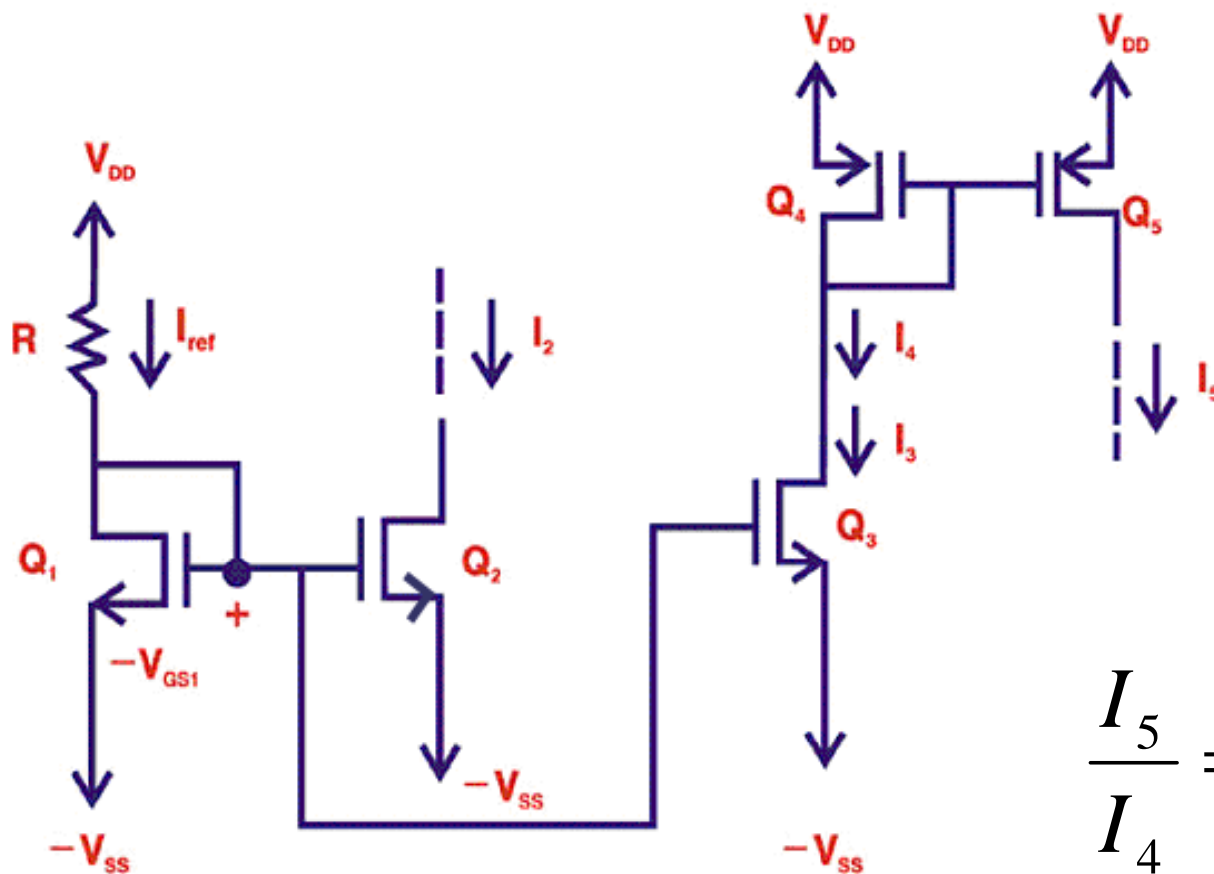
PMOS Current Mirror



For the PMOS transistors Q_4 and Q_5 , the following parameters must match:

$$V_{TH,4} = V_{TH,5}, \quad k_{p,4}' = k_{p,5}', \quad \lambda_4 = \lambda_5$$

PMOS Current Mirror



$$\frac{I_5}{I_4} = \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}$$

We can now relate the sourced current I_5 to the reference current I_{ref} :

$$\frac{I_5}{I_{ref}} = \frac{I_3}{I_{ref}} \cdot \frac{I_4}{I_3} \cdot \frac{I_5}{I_4} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} \cdot 1 \cdot \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}$$

$$\frac{I_5}{I_{ref}} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} \cdot \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}$$

- 1) We need only one resistor R , no matter how large is the number of DC currents generated.
- 2) By using current steering we can create sourcing currents from sinking currents or vice versa.
- 3) The reference current can reside either in a NMOS current mirror or in a PMOS current mirror.

Example (a follow-up to the previous example)

Given: $V_{DD} = 5V$, $V_{SS} = 0$

$V_{TH,1} = V_{TH,2} = V_{TH,3} = 1V$, $k_{n,1}' = k_{n,2}' = k_{n,3}' = 20\mu A/V^2$ and $R = 1K\Omega$.

$V_{TH,4} = V_{TH,5} = -1V$, $k_{p,4}' = k_{p,5}' = 30\mu A/V^2$

Need: A reference current of $I_{ref} = 1mA$, one sink current of $7mA$ and one source current of $5mA$.

Question: Using the diagram scheme just discussed, what should be all (W/L) ratios of all five transistors?

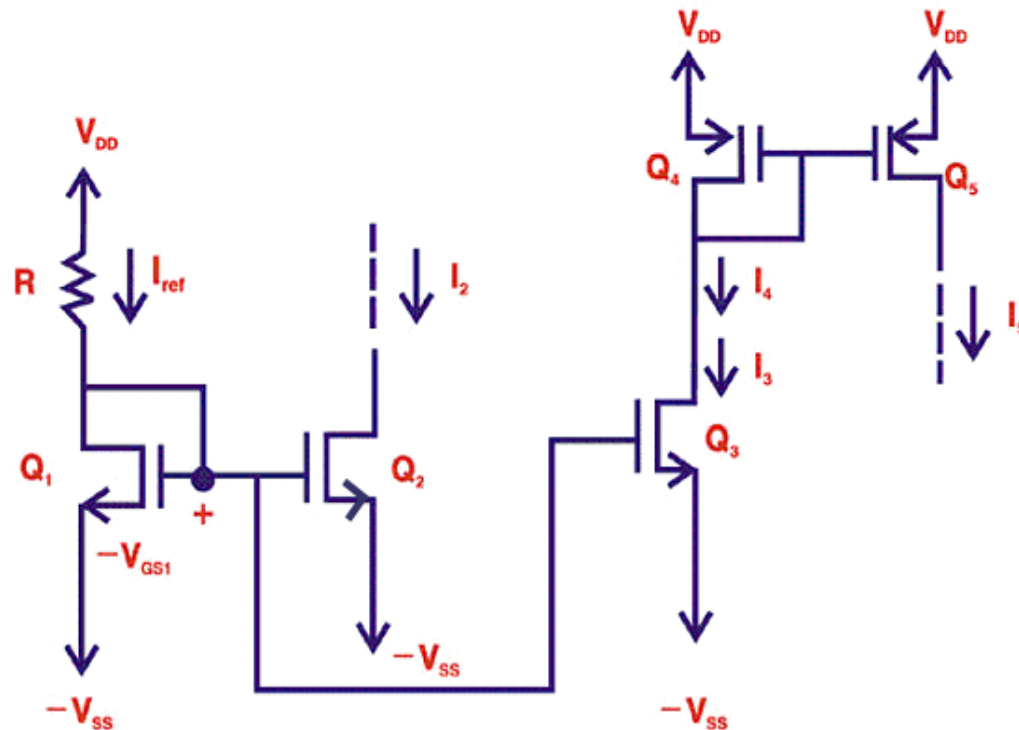
Solution

The beginning of the solution is identical to what has been done in the previous examples.

Let's quote the results:

$(W/L)_1 = 11.11$ and $(W/L)_2 = 77.77\mu\text{A}$.

Current I_2 is then the desired sink current



Now:

$$\frac{I_5}{I_{ref}} = \frac{5mA}{1mA} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} \cdot \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4} = \frac{\left(\frac{W}{L}\right)_3}{11.11} \cdot \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4}$$

There are infinitely many choices for the geometric dimensions of transistors Q_3 , Q_4 and Q_5 . For instance, we may take $(W/L)_3 = 11.11$, $(W/L)_4 = 10$ and $(W/L)_5 = 50$. Current I_5 is then the required source current.

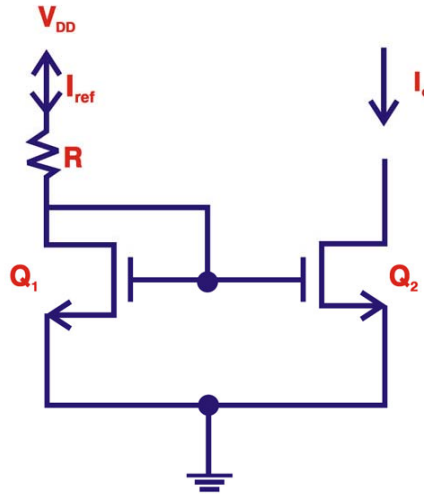
The channel-length modulation effect may be responsible for errors in the operation of a Current Mirror Current Source.

For instance, depending on the load of Q2 we may get $V_{DS,2} \neq V_{DS,1}$. As a result the value of I_2 will slightly vary, depending on the load. It means that the current source is not ideal - it has a finite output resistance, equal to r_o of the respective output transistor.

Improved Current-Mirror Current Sources – L20

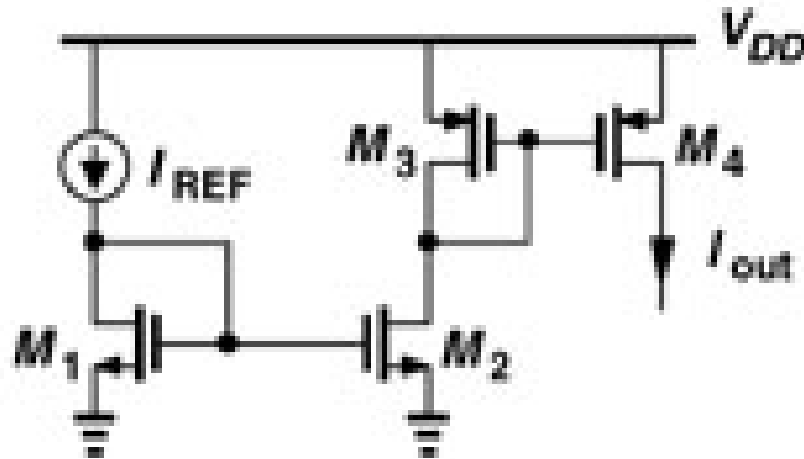
Cascode Current Mirror

Reference Current



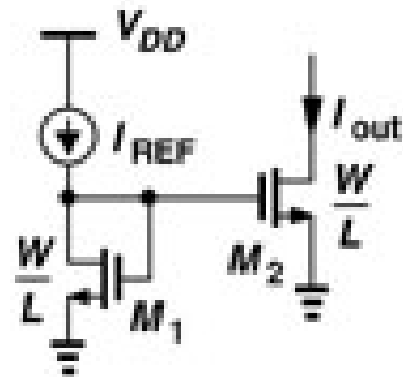
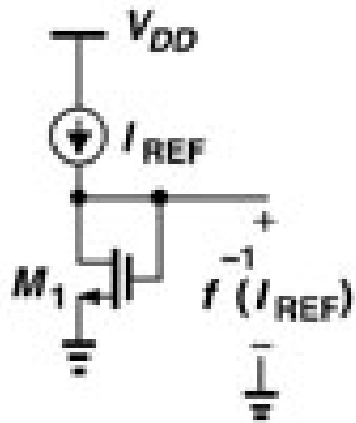
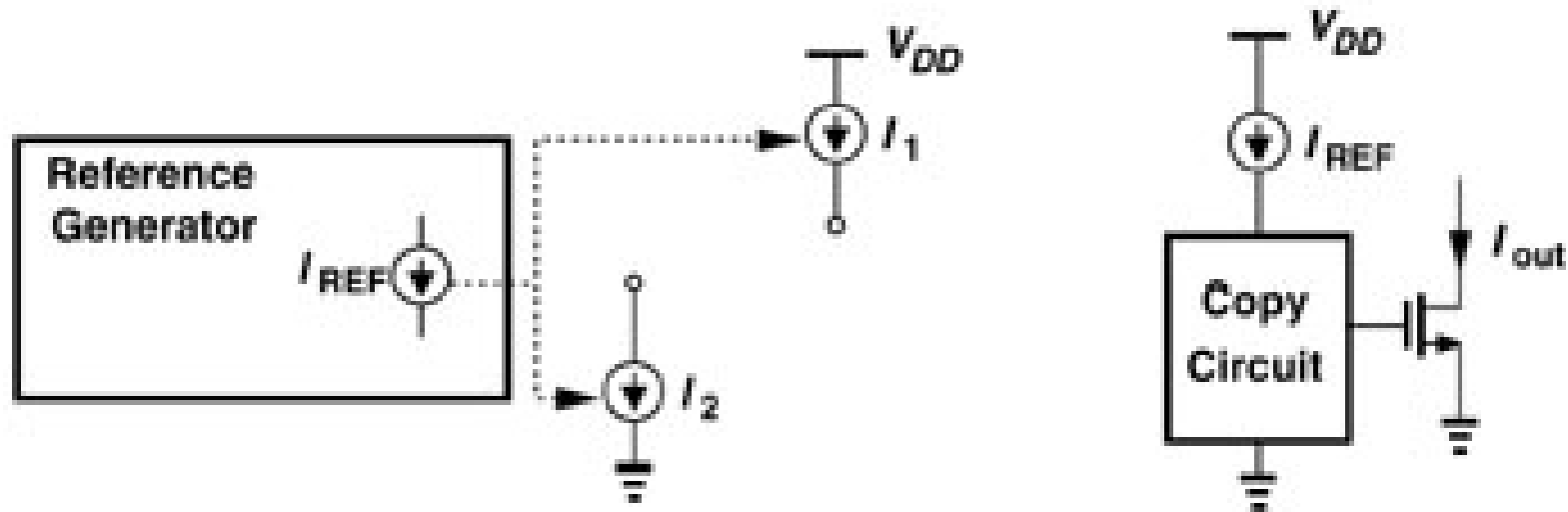
- I_{ref} must be very stable and accurate, not subject to fluctuations in:
 - V_{DD}
 - Temperature
- We do not implement I_{ref} just with a resistor!

Example

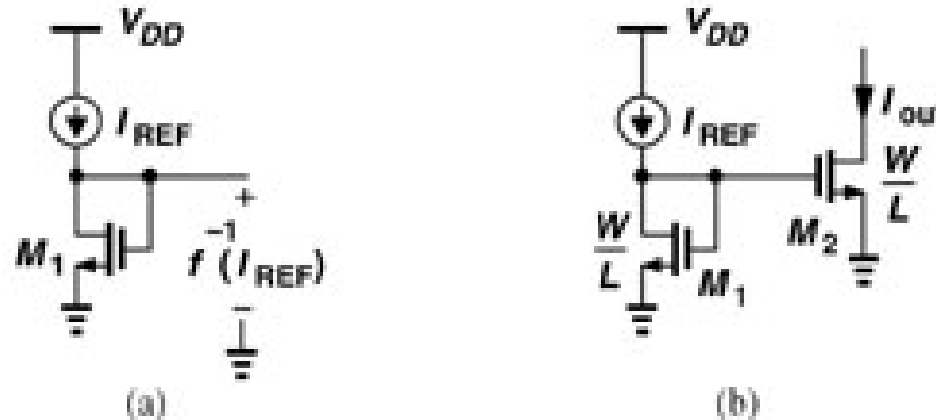


- NMOS Current Mirror steering current to a PMOS current Mirror.
- I_{ref} is shown only symbolically. Its circuit is more complicated, often involving BJT transistors (for temperature stabilization)!

Reference Currents

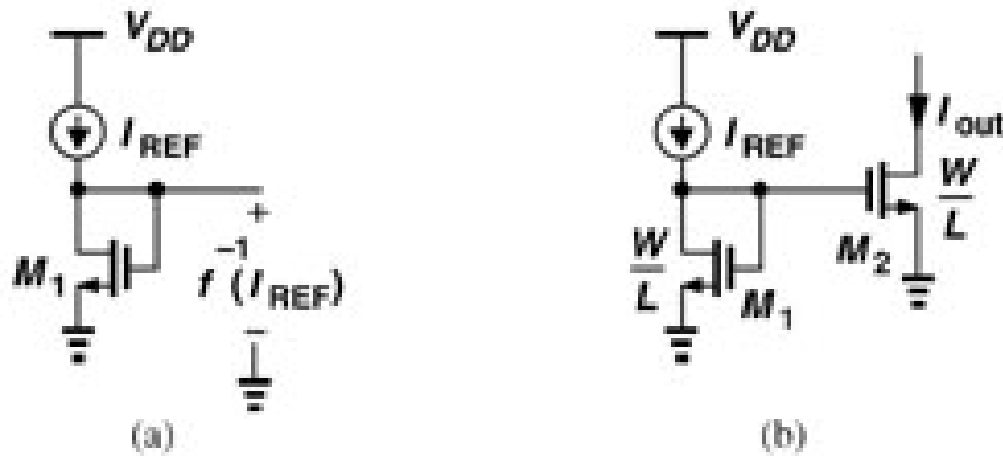


λ effect introduces large error in the mirrored current



- $I_{out} = I_{ref}$ only if $\lambda = 0$ in both transistors, or we arrange that both transistors have the same V_{DS} , which is impossible, as V_{D2} depends on the circuit that I_{out} is connected to.

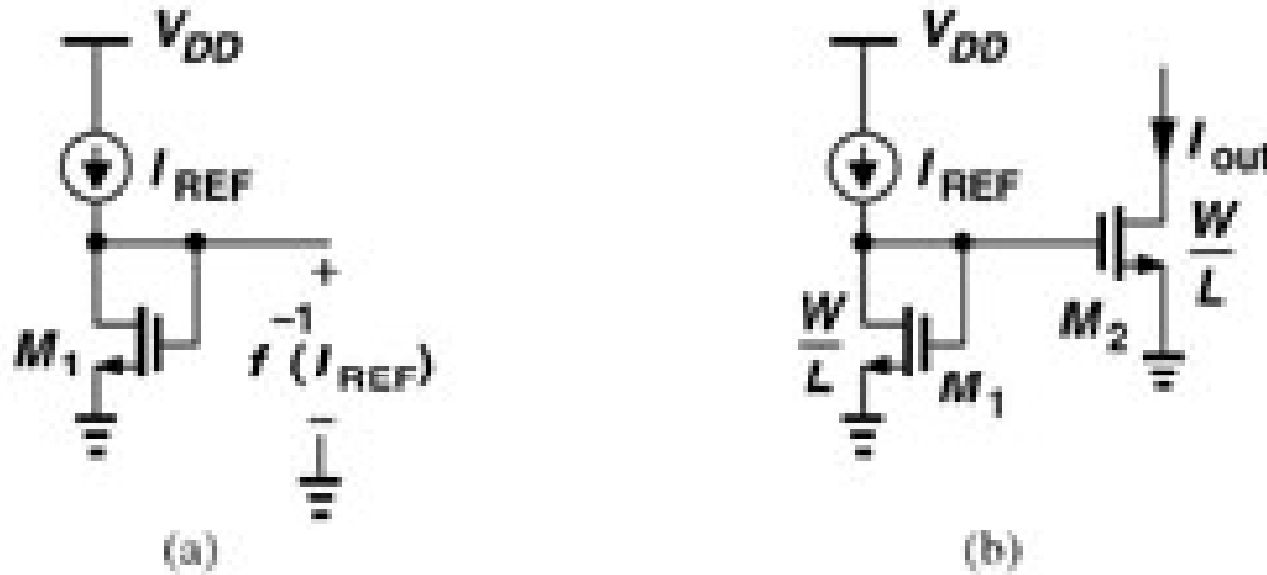
λ effect introduces large error in the mirrored current



$$I_{D,1} = I_{ref} = \frac{1}{2} k_{n,1} \left(\frac{W}{L}\right)_1 (V_{GS,1} - V_{TH,1})^2 (1 + \lambda_1 V_{DS,1})$$

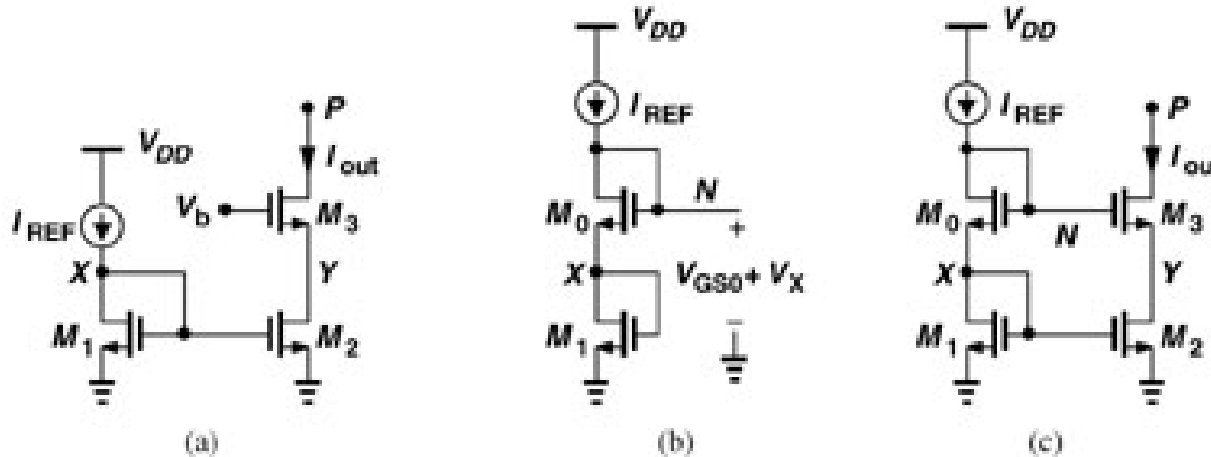
$$I_{D,2} = I_{out} = \frac{1}{2} k_{n,2} \left(\frac{W}{L}\right)_2 (V_{GS,2} - V_{TH,2})^2 (1 + \lambda_2 V_{DS,2})$$

If $W/L, k_n', V_{TH}$ and λ are all symmetric then:



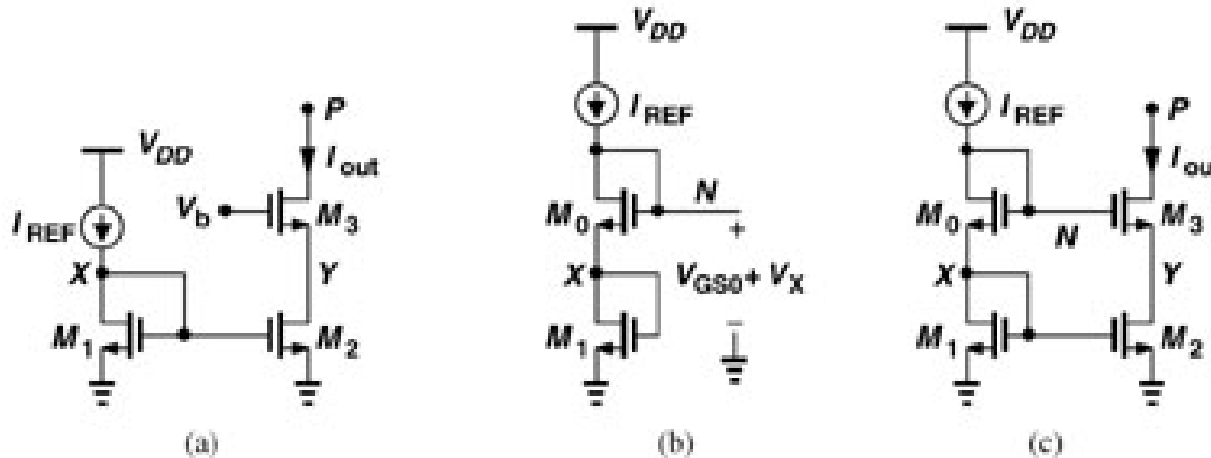
$$\frac{I_{out}}{I_{ref}} = \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}}$$

How can the Cascode idea help in creating improved current mirrors?



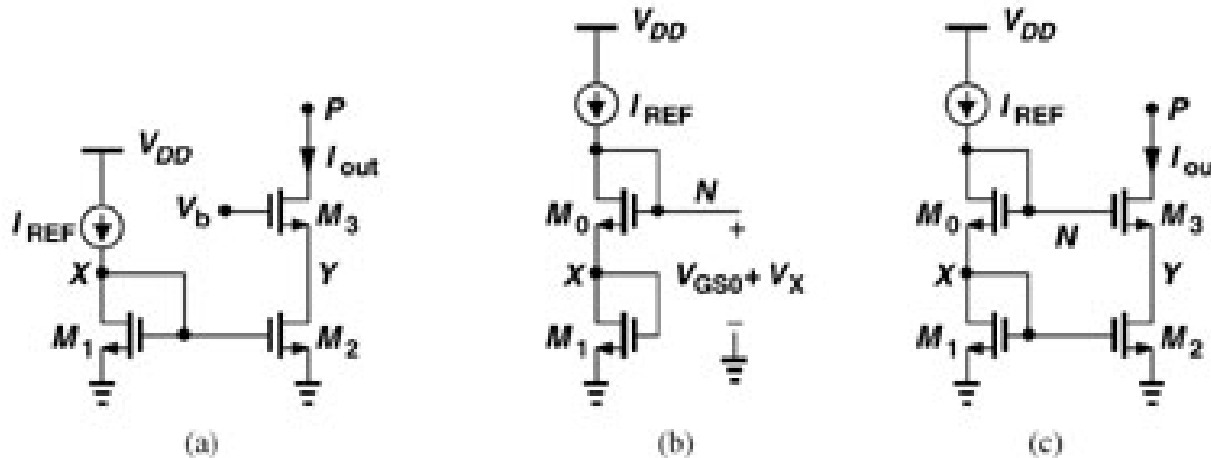
- (a): By choosing a suitable bias voltage V_b we can force V_Y to equal V_X , and then I_{out} will be a perfect mirror image of I_{ref}
- The cascode M_2 and M_3 also provides a larger output resistance.

How do we generate V_b ?



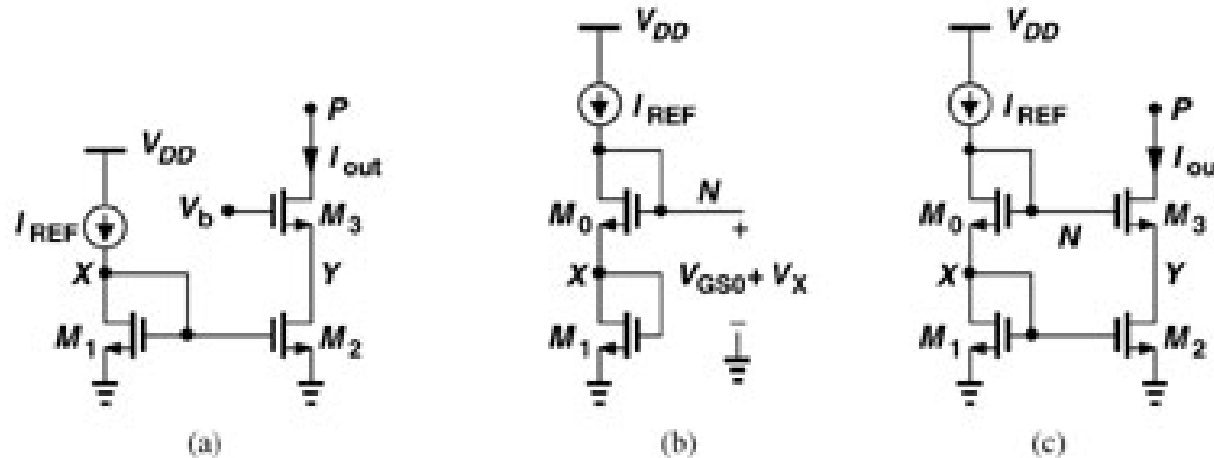
- We need $V_Y = V_X$, therefore:
- $V_b - V_{GS3} = V_X \rightarrow V_b = V_{GS3} + V_X$
- We see that we need to add to V_X some suitable V_{GS}

(b): That's why we stack one more diode-connected M_0 on top of M_1 :



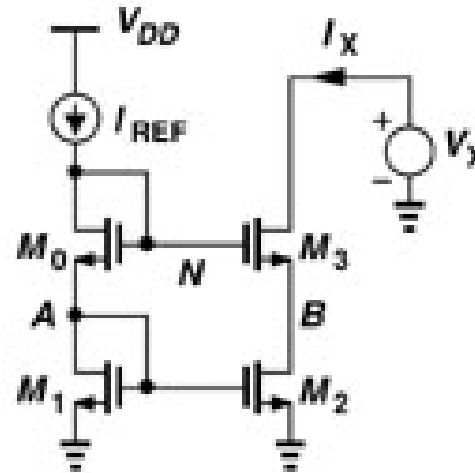
- $V_N = V_{GS0} + V_X$
- Let's match M_0 to M_3 and connect their gates.
- By structure we can create: $V_{GS0} = V_{GS3}$

(c): Implementation of a Cascode Current Mirror

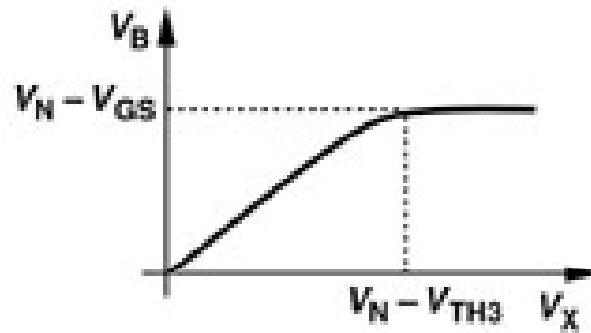


- $V_N = V_{GS0} + V_X = V_{GS3} + V_Y$
- We need to choose $(W/L)_3/(W/L)_0 = (W/L)_2/(W/L)_1$
- Then: $V_{GS0} = V_{GS3}$ and $V_X = V_Y$ with no need to add a supply V_b .

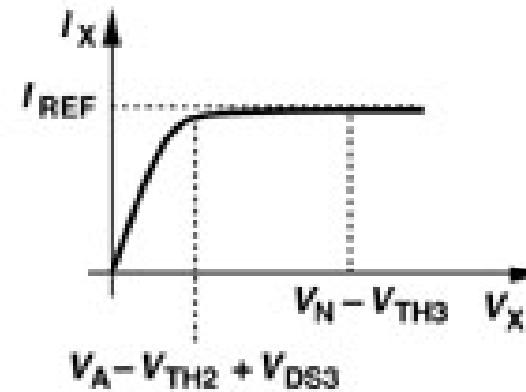
How low can V_X be before “trouble begins”?



(a)

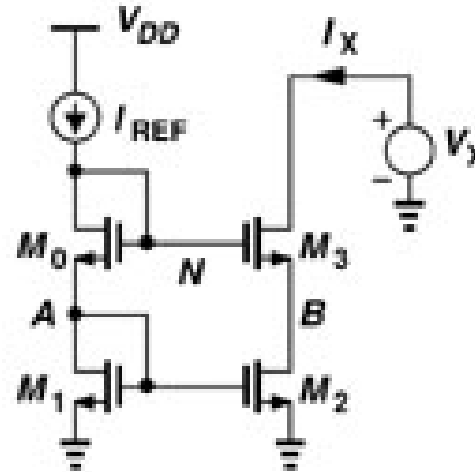


(b)

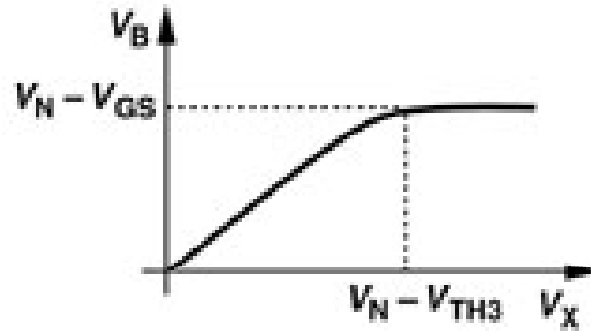


(c)

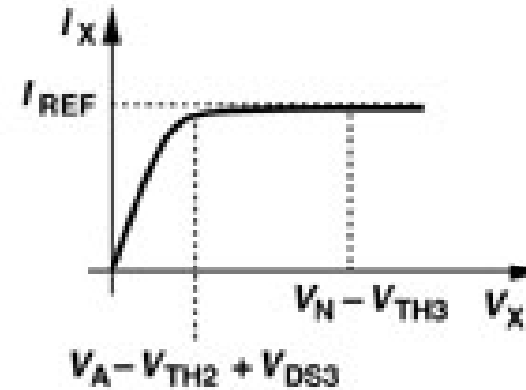
We can show that M_3 goes into Triode Mode before M_2 does, and current source still functions



(a)

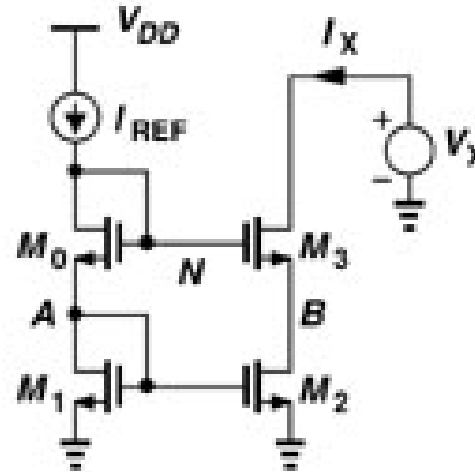


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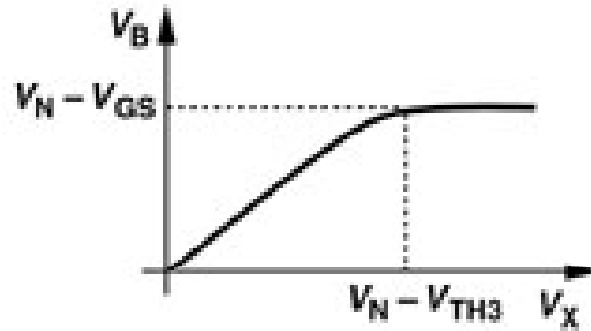


(c)

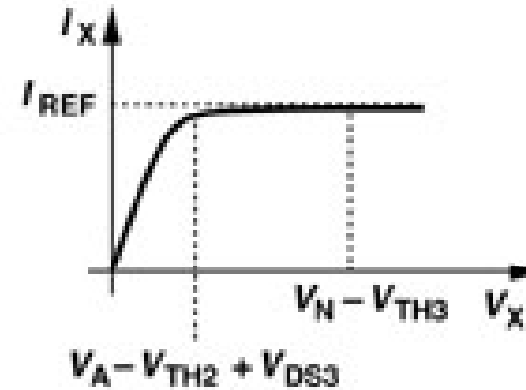
Only when M_2 too enters Triode Mode performance begins to deteriorate rapidly



(a)



(b)

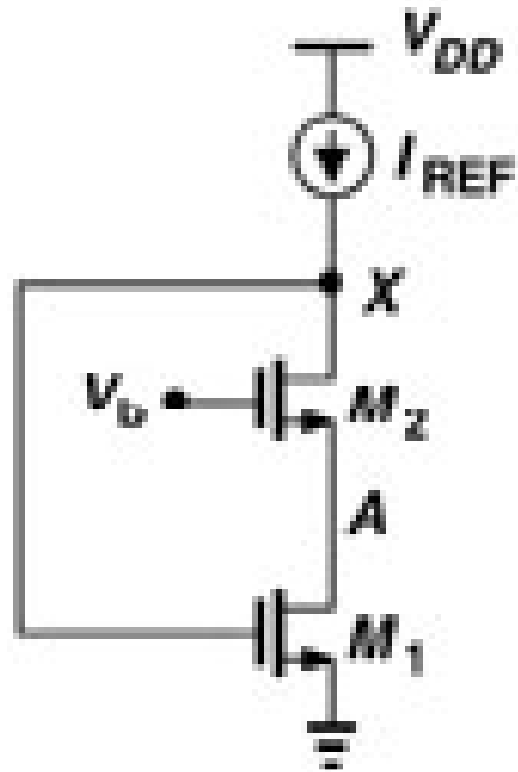


(c)

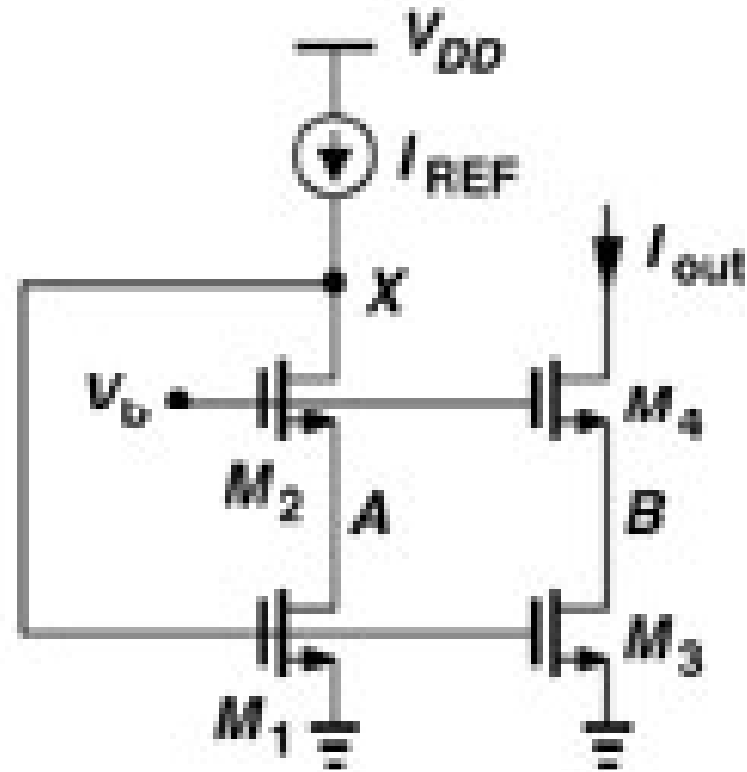
Accuracy vs. “Headroom” Tradeoff

- “Headroom”: The DC range of output voltage for which operation is still ok (in the case of Current Mirror Current Source, we talk about the range of V_X (of previous slide) for which I_{out} still mimics I_{ref})
- A simple current mirror allows for larger headroom, but it is less accurate.
- Cascode has a much narrower headroom, but it is much more accurate.

Tricky cascode structure that saves one V_{TH} of headroom

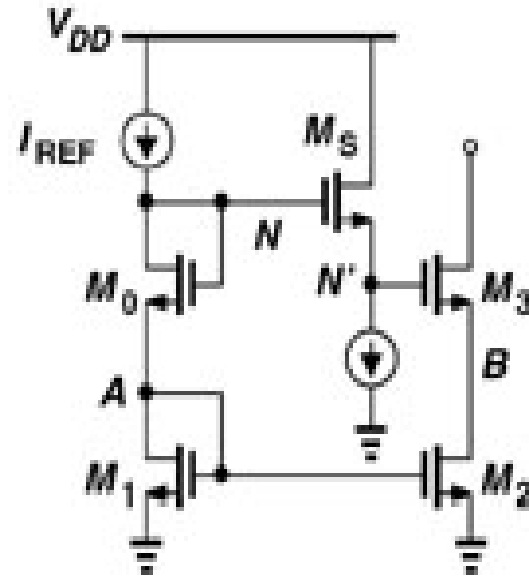
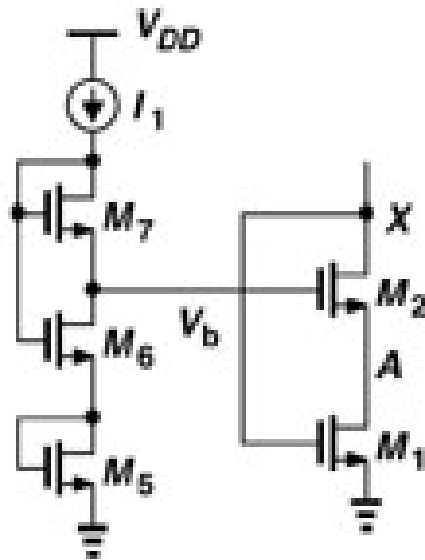
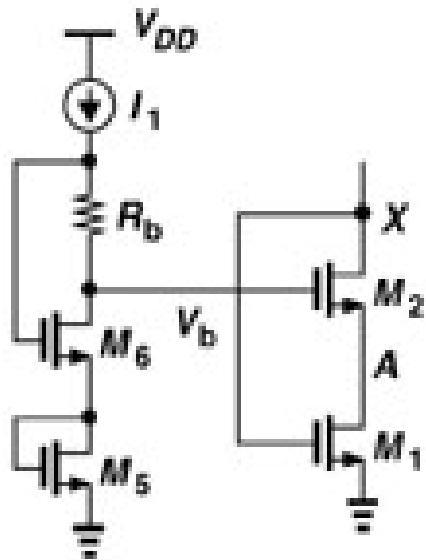


(a)



(b)

Actual implementations of the “larger headroom” cascode current mirror

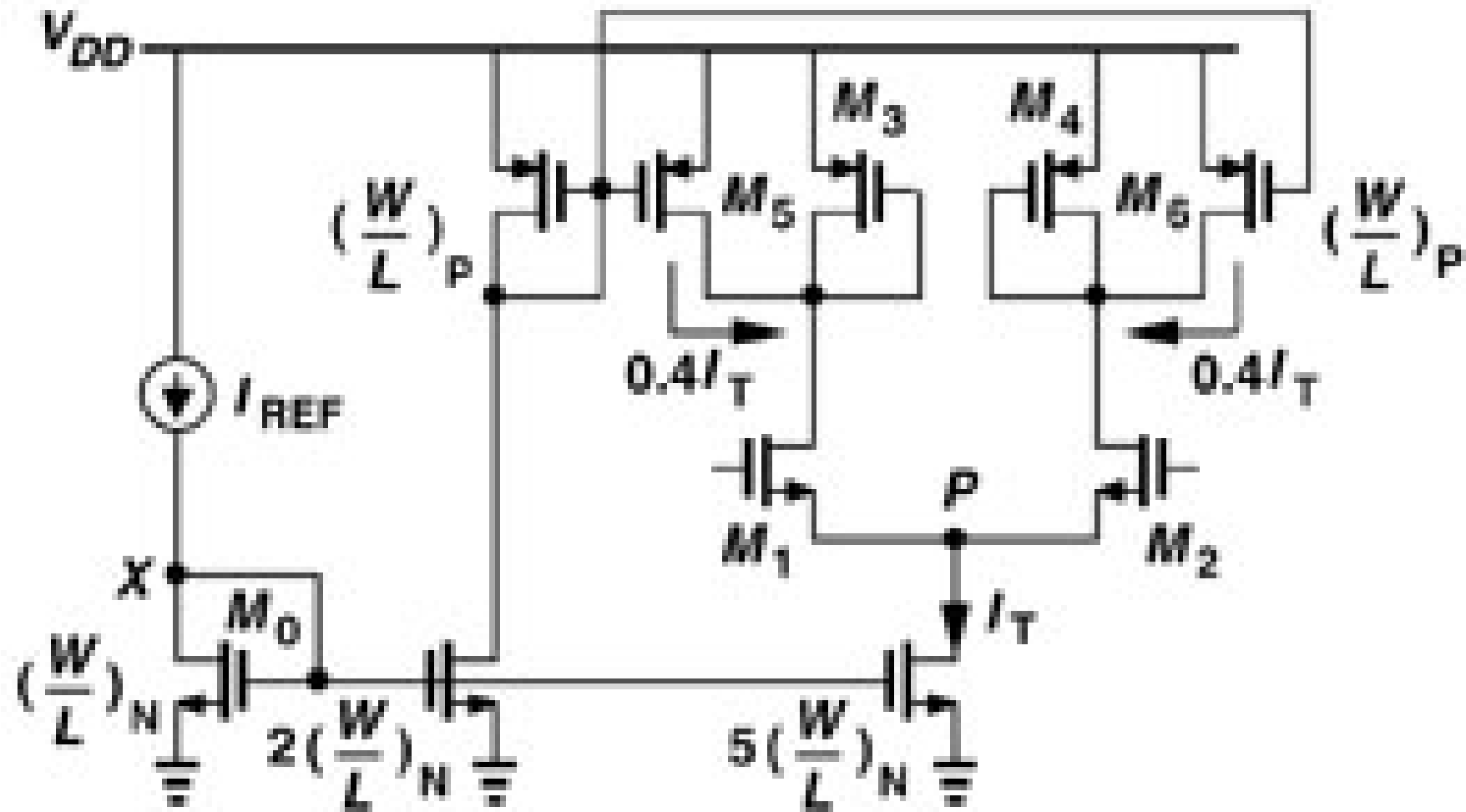


We shall skip the topic – it is not needed anywhere later on.

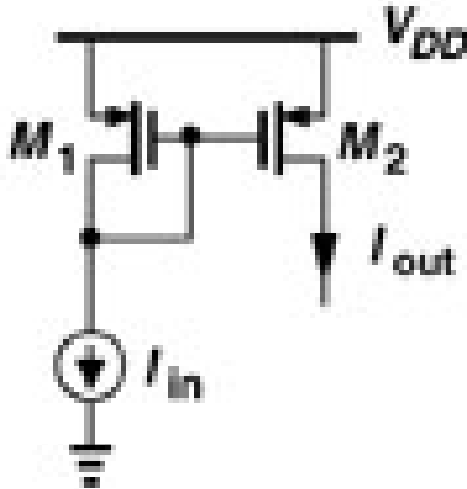
CMOS Differential Amplifiers

Current Mirror Current Source
Load – L21

Typical Amplifier Example

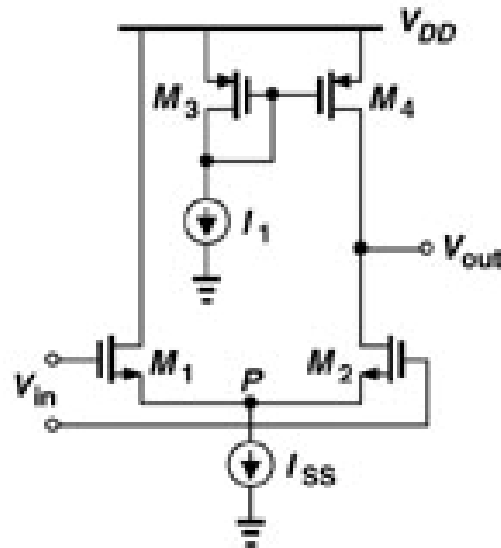


Idea: non-inverting “current assist”



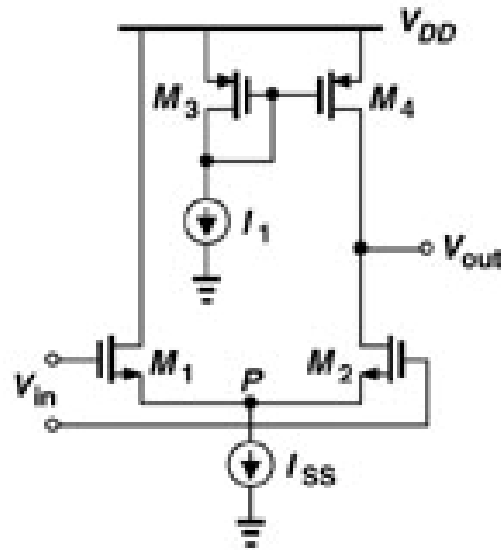
- In this simple PMOS current mirror we have $I_{out} \approx I_{in}$
- If I_{in} increases by a small signal ΔI , I_{out} increases by the same amount (if transistors are identical)

Differential Amplifier with current mirror load and single-ended output: Attempt 1



- Since we are interested in a single-ended output we don't need a load on the left branch
- Current symmetry is determined by the GS circuitry.
- What is the single-ended differential gain?

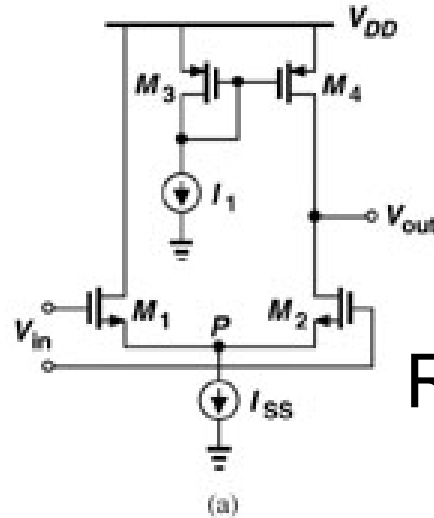
Voltage Gain Computation Approaches



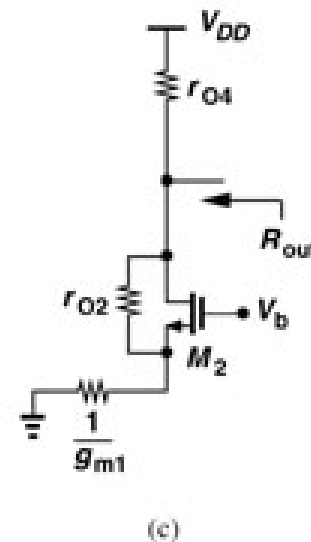
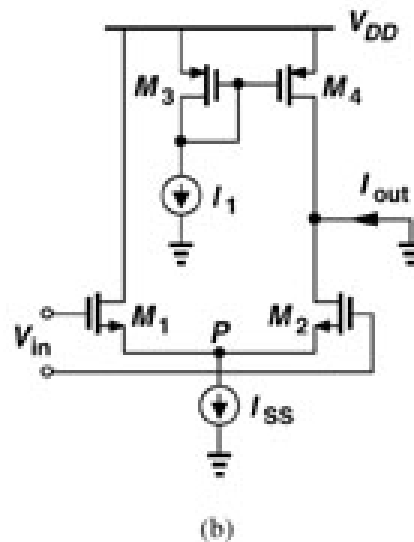
- Cannot use the half-circuit method.
- Method 1: $A_V = G_m R_{out}$
- Method 2: Source Follower \rightarrow CG amp

Generalized G_m and R_{out} approach

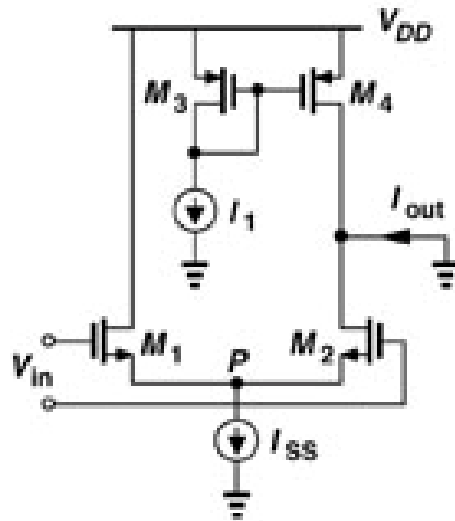
G_m computation



R_{out} computation

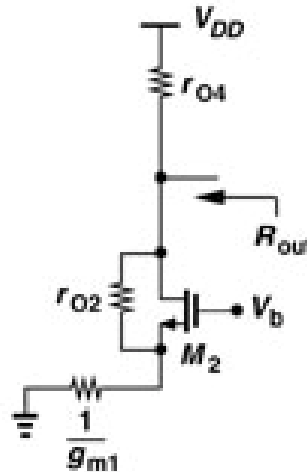


G_m computation



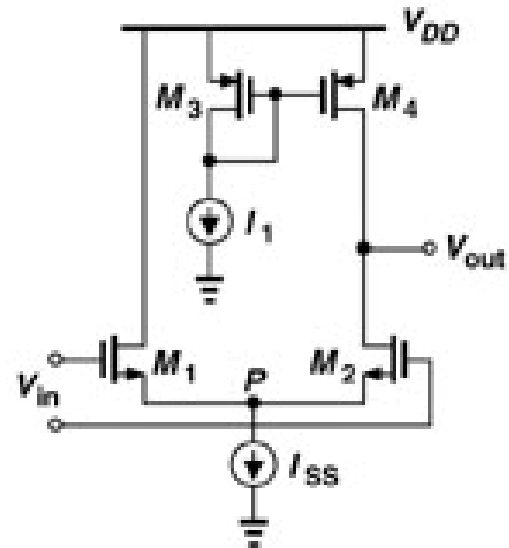
- $G_m = I_{out} / V_{in}$ in the shown polarity and for output short-circuited to ground.
- $G_m = (g_{m1} V_{in} / 2) / V_{in} = g_{m1} / 2$
- Explanation: break V_{in} into positive half and negative half

R_{out} computation



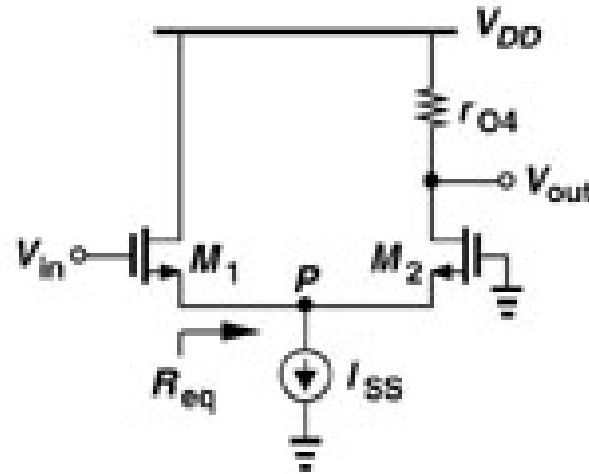
- $R_{out} = [(1 + g_{m2} r_{o2})(1/g_{m1}) + r_{o2}] \parallel r_{o4} \approx (2r_{o2}) \parallel r_{o4}$
- Explanation: M_2 is degenerated by M_1 's output resistance $1/g_{m1}$; M_4 's output resistance is r_{o4}

Voltage Gain



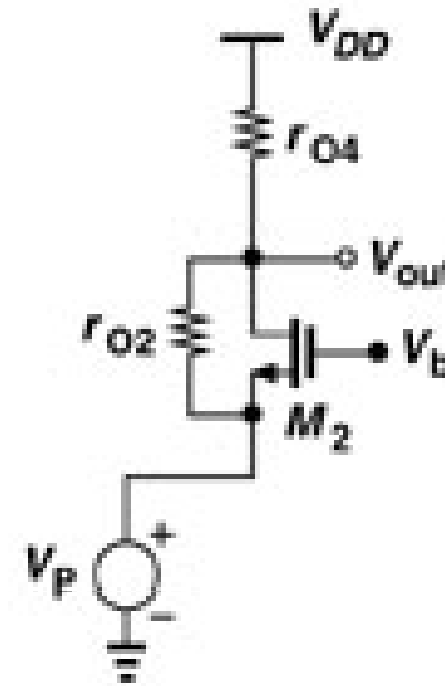
- $|A_V| = G_m R_{out} \approx (g_{m1}/2)[(2r_{o2}) || r_{o4}]$

Gain computation – CD → CG approach



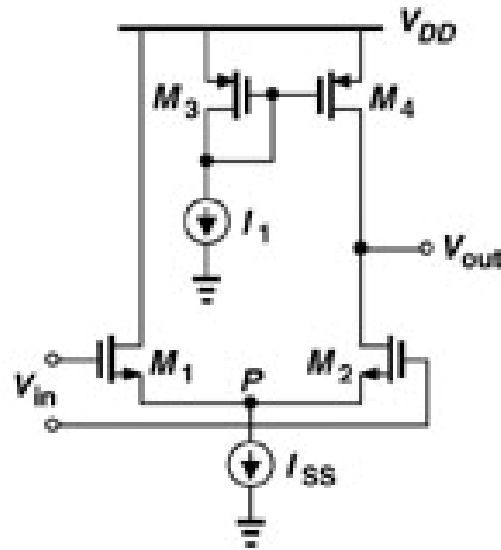
- $A_V = V_{out} / V_{in} = (V_P / V_{in})(V_{out} / V_P)$
- Source follower M_1 : $V_P / V_{in} = R_{L,M2} / (R_{L,M2} + (1/g_{m1}))$
- $R_{L,M2} \approx (1/g_{m2}) + (r_{o4} / (g_{m2} r_{o2}))$
- Result: $V_P / V_{in} \approx (1 + (r_{o4} / r_{o2})) / (2 + (r_{o4} / r_{o2}))$

CD \rightarrow CG approach



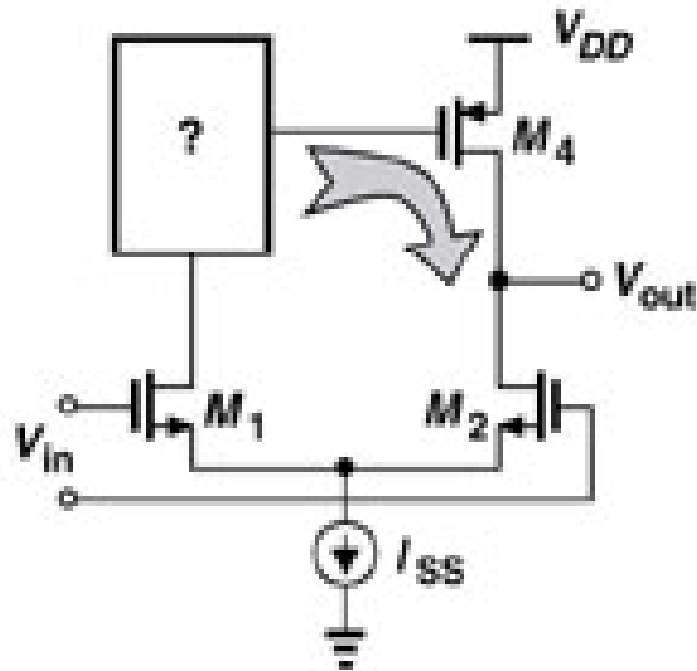
- CG M_2 :
- Result: $V_{out}/V_P \approx (1 + g_{m2}r_{o2}) / (1 + (r_{o2}/r_{o4}))$
- Overall result comes out to be the same as obtained by the other method.

Differential Amplifier with current mirror load and single-ended output: Attempt 1

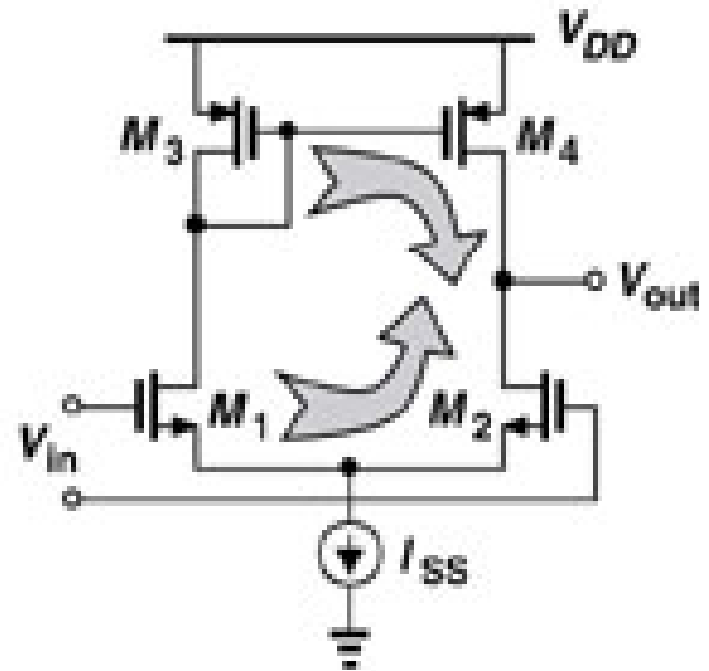


- Drawback of the circuit: Small-signal gain of M_1 is “wasted”
- Can get a better gain using the “current assist” idea shown earlier.

Active Current Mirror Load



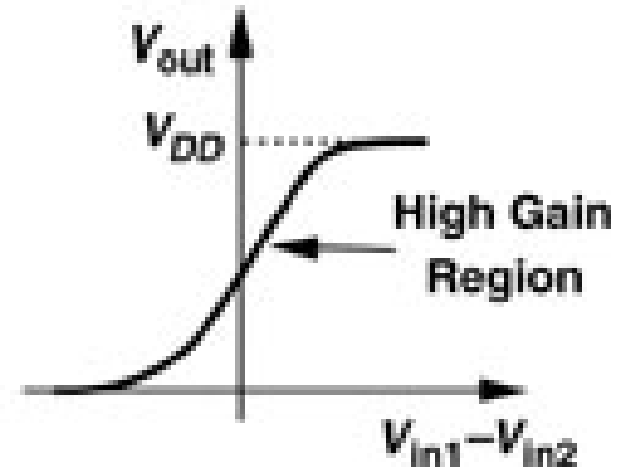
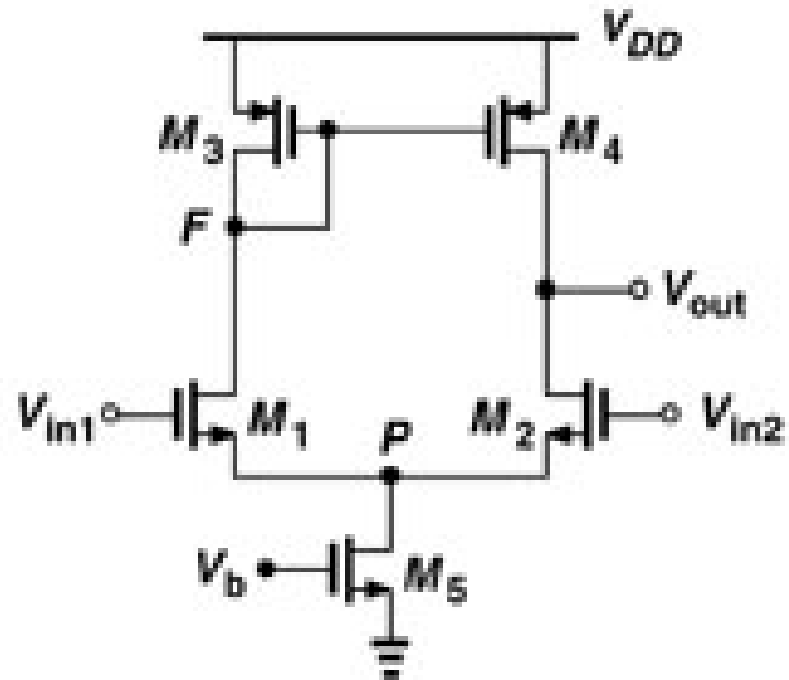
(a)



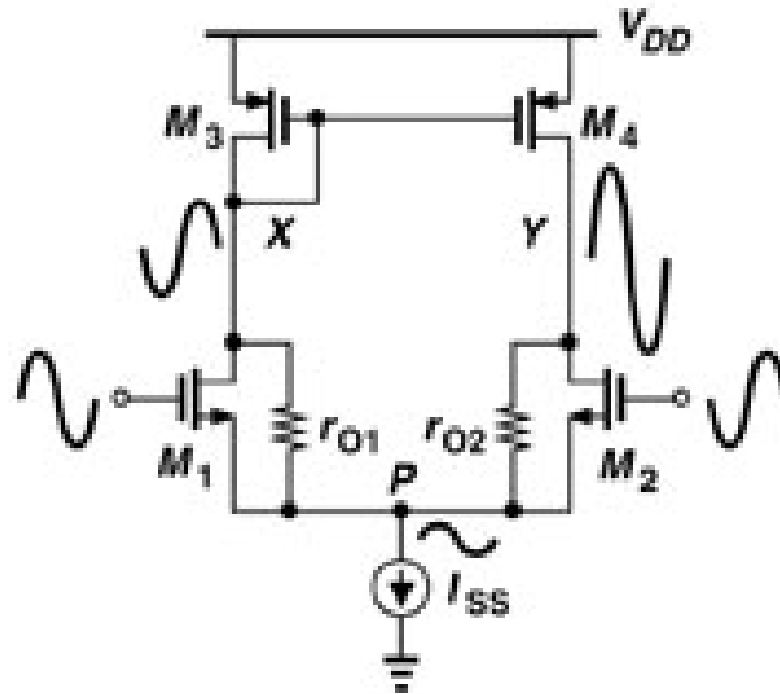
(b)

Idea: If V_{G1} slightly increases, I_1 increase by ΔI and I_2 decreases by ΔI . Also at the same time I_4 increases by ΔI . Both cause V_{out} to increase!

Open Loop Constraints



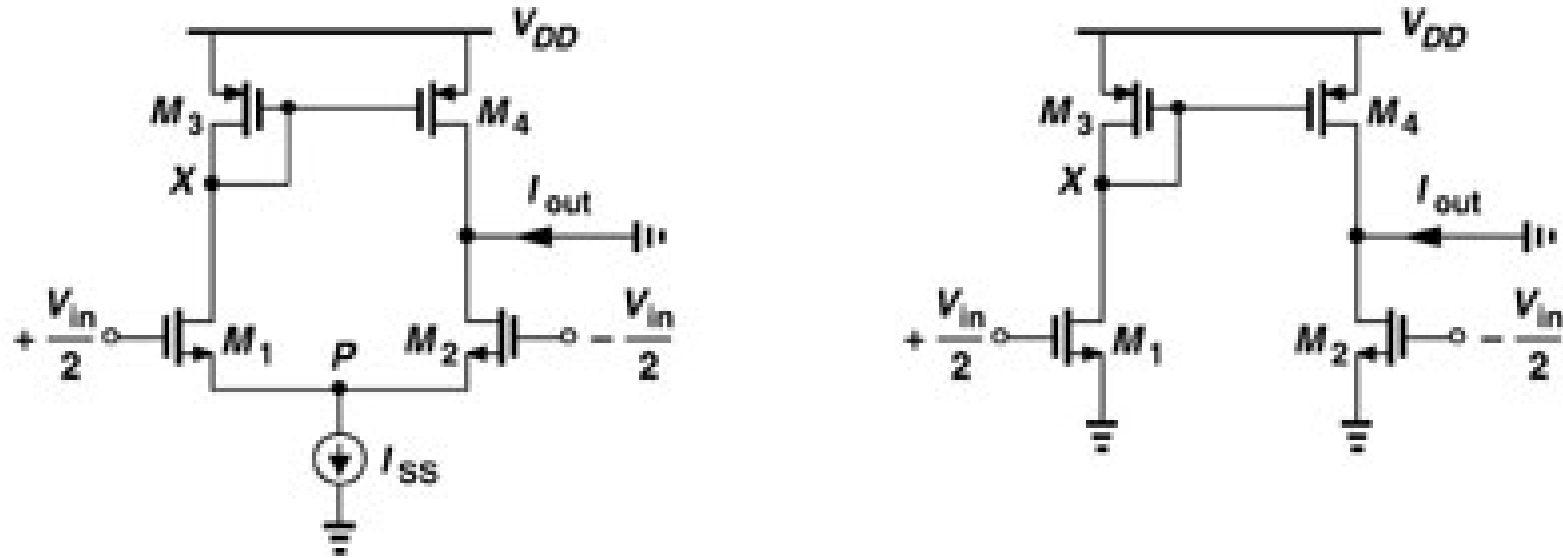
Small-Signal Single-ended Voltage Gain



$$A_V \approx G_m R_{out}$$

Again, can't use half-circuit method
(see signals above)

Calculation of G_m

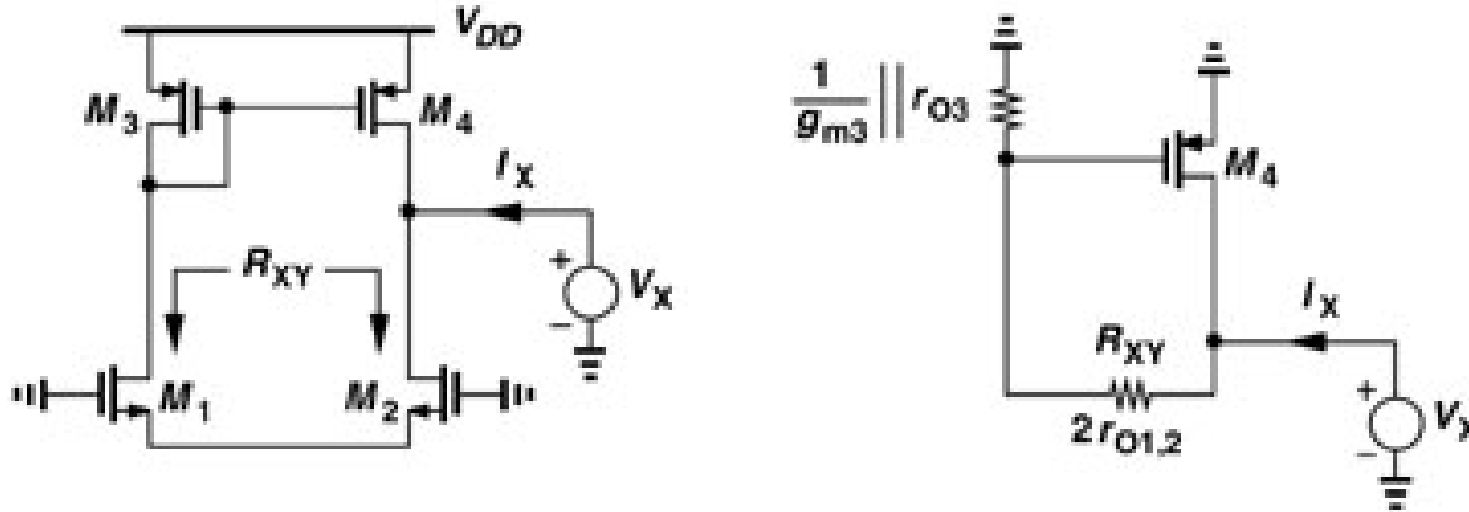


$$I_{D1} = I_{D3} = I_{D4} = g_{m1,2} V_{in} / 2 \quad I_{D2} = -g_{m1,2} V_{in} / 2$$

$$I_{out} = I_{D2} - I_{D4} = -g_{m1,2} V_{in} \Rightarrow G_m = g_{m1,2}$$

Note: Active Current Mirror load increased G_m by factor of 2!

Complicated Calculation of R_{out}

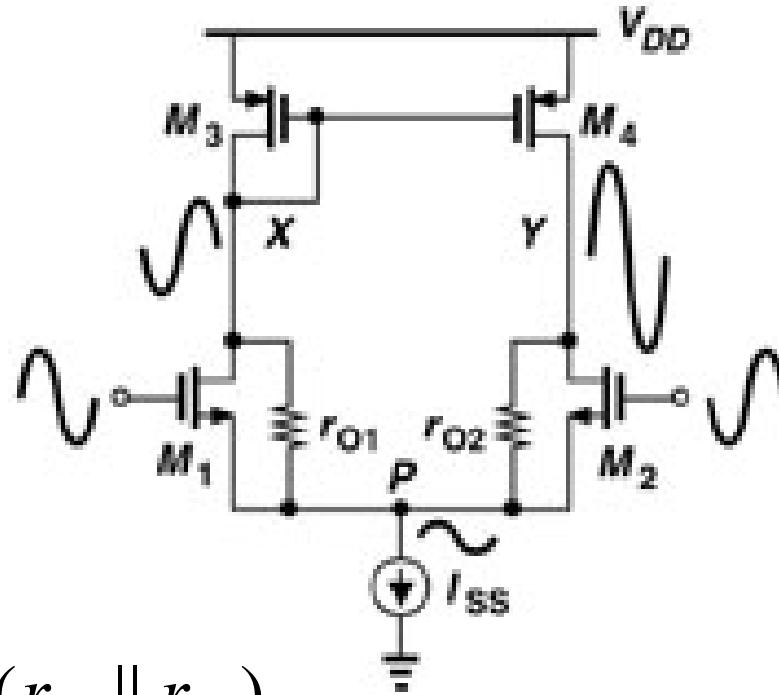


$$I_X = 2 \frac{V_X}{2r_{o1,2} + 1/g_{m3}} + \frac{V_X}{r_{o4}}$$

$$R_{out} \approx r_{o2} \parallel r_{o4}, \quad (2r_{o1,2} \gg [1/g_{m3}] \parallel r_{o3})$$

Note: R_{out} of this case is inferior to that of “no assist” case

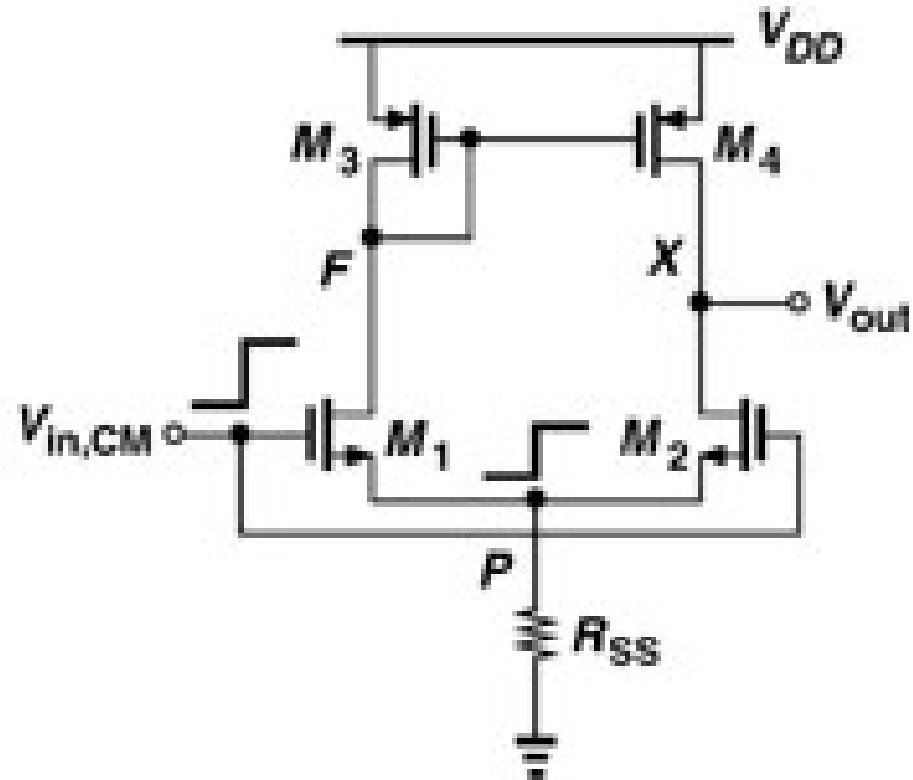
Small-Signal Gain



$$A_V \approx g_{m1,2} (r_{o2} \parallel r_{o4})$$

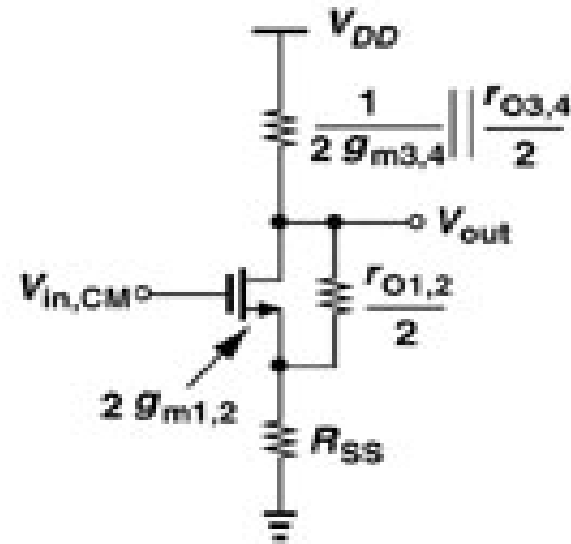
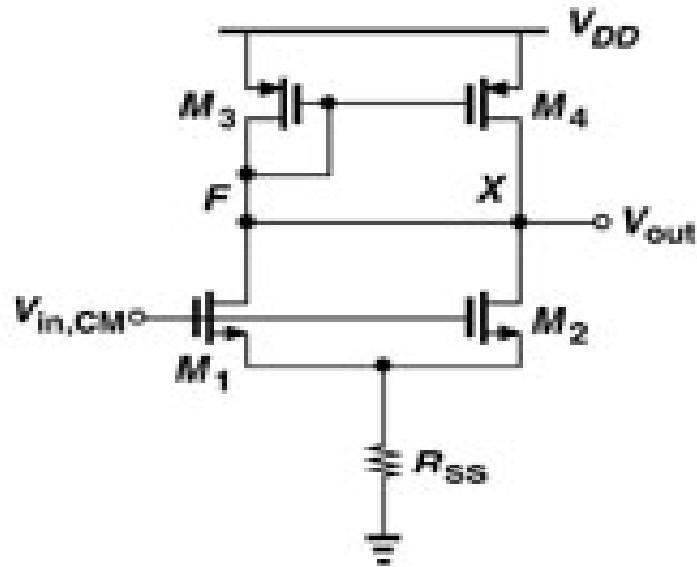
Overall gain is somewhat larger than that of the “no assist” case

Common Mode Characteristics



$$A_{CM} = \frac{\Delta V_{out}}{\Delta V_{in,CM}}$$

Common Mode Single-ended Gain



$$A_{CM} \approx \frac{-\frac{1}{2g_{m3,4}} \parallel \frac{r_{O3,4}}{2}}{\frac{1}{2g_{m1,2}} + R_{SS}} = \frac{-1}{1 + 2g_{m1,2}R_{SS}} \frac{g_{m1,2}}{g_{m3,4}}$$

Even with perfect symmetry $A_{CM} \neq 0$ if $R_{SS} < \infty$

Common Mode Rejection Ratio for single-ended output

$$CMRR = \left| \frac{A_{DM}}{A_{CM}} \right|$$

$$= g_{m1,2} (r_{o1,2} \parallel r_{o3,4}) \frac{g_{m3,4} (1 + 2g_{m1,2} R_{SS})}{g_{m1,2}}$$

$$= g_{m3,4} (r_{o1,2} \parallel r_{o3,4}) (1 + 2g_{m1,2} R_{SS})$$