Lecture 11:

RIE of Silicon
- Poly-silicon and Bulk-silicon-

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RIE in Thin Film Etching (1)

- Thin poly silicon etch in surface micromachining
  - Usually, photo resist is used for etch mask material

(a) Oxide/nitride deposition, **polysilicon deposition & patterning (RIE is performed)**

(b) Nitride deposition, sacrificial oxide deposition

(c) Anchor patterning, **polysilicon deposition & patterning (RIE is performed)**

(d) Sacrificial wet etch in HF

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Detailed view of the multi-level polysilicon that are a critical part of a microengine.

Detailed view of polysilicon beam with PR mask after RIE.
**RIE in Bulk Etching (1)**

- Thick polysilicon, epipoly silicon, and bulk silicon etch
  - Selectively remove significant amounts of silicon from a substrate
  - Maximum etch thickness is several hundred micro meters.
  - Usually, oxide hard mask and photo resist are used for etch mask material

  (When etch thickness is less then 10 µm, photo resist is used)
RIE in Bulk Etching(2)

DRIE for through wafer holes (400 µm deep 50x50 µm² holes)

6 µm beam poly etch (before resist strip).

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RIE Principles (1)

- **RIE**: Reactive Ion Etching
- Process in which chemical etching is accompanied by ionic bombardment
- Combination of physical and chemical etching
- Faster and simpler etching in a few cases
- Anisotropic etching

![Typical parallel-plate reactive ion etching system](image)

Diffuser Nozzles
RIE Principles (2)

• Basic steps in a plasma etching process

1. Generation of Etchant Species

2. Diffusion to Surface

3. Adsorption

4. Reaction

5. Desorption

6. Diffusion into convection flow

Plasma

Gas Flow

Film

Byproducts

Ion Bombardment

Boundary layer

Sheath layer

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RIE Principles (3)

• Typical reactions and species present in a plasma used for plasma etching

• Typically there are about $10^{15}$ cm$^{-3}$ neutral species (1 to 10% of which may be free radicals) and $10^8$-$10^{12}$ cm$^{-3}$ ions and electrons.
## RIE Principles (4)

<table>
<thead>
<tr>
<th></th>
<th>Plasma Etching</th>
<th>Reactive Etching</th>
<th>Physical Etching</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Substrate Location</strong></td>
<td>Barrel Reactor: Surrounded by plasma</td>
<td>Planar Reactor: On grounded electrode in Plasma</td>
<td>Ion: On powered electrode in plasma</td>
</tr>
<tr>
<td><strong>Pressure (torr)</strong></td>
<td>$10^{-1} \sim 1$</td>
<td>$10^{-1} \sim 1$</td>
<td>$10^{-2} \sim 10^{-1}$</td>
</tr>
<tr>
<td><strong>Ion energy (eV)</strong></td>
<td>0</td>
<td>$1 \sim 100$</td>
<td>$100 \sim 1000$</td>
</tr>
<tr>
<td><strong>Active Species</strong></td>
<td>Atoms, Radicals</td>
<td>Atoms, radicals, reactive ions</td>
<td>Radicals, reactive ions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Products</strong></td>
<td>Volatile</td>
<td>Volatile</td>
<td>Volatile</td>
</tr>
<tr>
<td><strong>Mechanism</strong></td>
<td>Chemical</td>
<td>Chemical/Chemical-Physical</td>
<td>Chemical/Physical</td>
</tr>
<tr>
<td><strong>Etch Profile</strong></td>
<td>Isotropic</td>
<td>Isotropic/Anisotropic</td>
<td>Isotropic/Anisotropic</td>
</tr>
<tr>
<td><strong>Selectivity</strong></td>
<td>$30 : 1 \sim 10 : 1$</td>
<td>$10 : 1 \sim 5 : 1$</td>
<td>$30 : 1 \sim 5 : 1$</td>
</tr>
<tr>
<td><strong>Resist Compatibility</strong></td>
<td>Excellent</td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td><strong>Device Damage</strong></td>
<td>Little</td>
<td>Little</td>
<td>Some possible</td>
</tr>
<tr>
<td><strong>Etch Rate (um/min)</strong></td>
<td>$0.1 \sim 0.5$</td>
<td>$0.1 \sim 0.5$</td>
<td>$0.05 \sim 0.1$</td>
</tr>
<tr>
<td><strong>Resolution (um/min)</strong></td>
<td>3</td>
<td>2</td>
<td>$1 \sim 2$</td>
</tr>
</tbody>
</table>


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Basic Method of RIE (1)

- Chemical
  - Thermalized neutral radicals chemically combine with substrate material forming volatile products
  - Isotropic
  - Pure Chemical Reaction
  - High Pressure
  - Batch Wafer Type
  - Less Electrical Damage
Basic Method of RIE (2)

• Sputtering
  – The ion energy mechanically ejects substrate material
  – Anisotropic
  – By Purely Physical Process
  – High Directionality
  – Low Pressure: long mean free path
  – Single Wafer Type
  – Low Etch rate

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Basic Method of RIE (3)

• Energetic Ion Enhanced
  – Ion bombardment enhances or promotes the reaction between an active species and the substrate material
  – Damage Enhanced Chemical Reactivity
  – Chemical Sputtering
  – Chemically Enhanced
  – Physical Sputtering
  – Ion Reaction
Basic Method of RIE (4)

• Protective Ion Enhanced
  – An inhibitor film coats the surface forming a protective barrier which excludes the neutral etchant
  – Sidewall passivation
  – Stopping lateral attack by neutral radical
  – Ion directionality
  – Involatile polymer film
  – Additive film former
    (N₂, HBr, BCl₃, CH₃F)
Summary of RIE Mechanisms and Systems

Ionic species

Reactive neutral species
• Free radicals important

Charge
+++++++ Mask erosion

Mask

Film or substrate

Undercutting

Chemical etching
• Isotropic, very selective

Physical etching
• Anisotropic, non-selective

Trenching

Ion-enhanced etching
• Needs both ions and reactive neutrals
• May be due to enhanced etch reaction or removal of etch by product or inhibitor
• Anisotropic, selective

Sidewall-inhibitor deposition
• Sources: etch byproducts, mask erosion, inlet gases
• Removed on horizontal surfaces by ion bombardment
• A possible mechanism in ion enhanced etching
Characterization of RIE Performance

- Etch performance valuation
  - Etch rate
  - Anisotropy (define as $1 - A/H$)
  - Selectivity to mask material
  - Micro-loading effect (RIE lag)
  - Macro-loading effect
    (dark field or bright field)
  - Etch uniformity
  - Surface quality
Plasma Etch & RIE & MERIE

**Plasma Etch**
- Plasma Sheath Potential: low
- Ion Bombardment: weak
- Chemical Reaction: dominant
- Etch Selectivity: high
  - Isotropic Etching

**Conventional RIE**
- Plasma Sheath Potential: high
- Strong Ion Bombardment plus Chemical Reaction
  - high etch rate
  - Anisotropic Etching

**MERIE**
(Magnetically Enhanced RIE)
- Magnetic Field Parallel to Cathode
- Secondary Electron confined near Cathode
  - increasing ionization
  - higher etch rate

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Schematic of ICP (Inductively Coupled Plasma)

- Process gases
- Source RF
- Plasma
- Process chamber
- Wafer
- E-Chuck
- Helium backside cooling
- RF coils
- Bias RF

- Low pressure (< 5 mTorr) and low temperature (-50ºC ~ +50ºC) etching
- Independent power control and high density plasma (~ $10^{12}$)
- Improved Plasma Uniformity
Mask Materials for RIE

• Etch mask
  – PR (Photo Resist), Hard mask (SiO$_2$, Al) is used
  – Selectivity
    = etch rate of etching material / etch rate of mask
  – Usually, standard PR (for CMOS) is not adequate for O$_2$ plasma etch → hard mask required

  – Selectivity of silicon:AZ1512
    • Cl based etch (physical etch): <2
    • F based etch (chemical etch): < 10
      (if O$_2$ gas is inserted the chamber the selectivity would be lower than 10)
Reaction in RIE Process (1)

- Reactants
  - Cl-based (Cl₂, BCl₃)
    - Sputtering or ion-enhanced etch mechanism
    - High anisotropy
    - Low selectivity
  - F-based (SF₆)
    - Chemical etch mechanism
    - High selectivity
    - High etch rate
    - Isotropic etching
  - Br-based (HBr, Br₂)
    - Good anisotropy
    - Sidewall passivation: SiBrₓ (x<4)
    - Good selectivity to oxide
Reaction in RIE Process (2)

- An example of RIE mechanisms (Cl based)

Ion and electron formation
\[ e + \text{Cl/Cl}_2 \rightarrow \text{Cl}^+ / \text{Cl}_2^+ + 2e \]

Etchant formation
\[ e + \text{Cl}_2 \rightarrow 2\text{Cl} + e \]

Adsorption of etchant on the substrate
\[ \text{Cl/Cl}_2 \rightarrow \text{Si}_{\text{surf}} - \text{nCl} \]

Reaction on surface
\[ \text{Si}_{\text{surf}} - \text{nCl} \rightarrow \text{SiCl}_{x(ads)}^{(ions)} \]

Product desorption
\[ \text{SiCl}_{x(ads)}^{(ions)} \rightarrow \text{SiCl}_{x(gas)} \]
Reaction in RIE Process (3)

- An example of RIE mechanisms (F based Si etch)
Reaction in RIE Process (4)

- An example of RIE mechanisms (Br based Si etch)

\[
\begin{align*}
HBr & \rightarrow \text{H} + \text{Br} \\
\text{Br} + \text{Si} & \rightarrow \text{SiBr}_4
\end{align*}
\]

- Small amount $\text{O}_2$ for sidewall passivation
- A little $\text{NF}_3$ for preventing black silicon
- Endpoint by time
CCP: BCl₃ Recipe and Example (1)

- System: Drytek DRIE-284
- Process parameter

<table>
<thead>
<tr>
<th></th>
<th>Step 1</th>
<th>Step 2</th>
<th>Step 3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power</strong></td>
<td>200 W</td>
<td>300 W</td>
<td>475 W</td>
</tr>
<tr>
<td><strong>Pressure</strong></td>
<td>20 mTorr</td>
<td>20 mTorr</td>
<td>40 mTorr</td>
</tr>
<tr>
<td><strong>Time</strong></td>
<td>1 min</td>
<td>1 min</td>
<td>10 min</td>
</tr>
<tr>
<td><strong>Gas</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cl₂</td>
<td>0 sccm</td>
<td>2 sccm</td>
<td>50 sccm</td>
</tr>
<tr>
<td>BCl₃</td>
<td>14 sccm</td>
<td>14 sccm</td>
<td>5 sccm</td>
</tr>
<tr>
<td>N₂</td>
<td>7 sccm</td>
<td>7 sccm</td>
<td>0 sccm</td>
</tr>
</tbody>
</table>

- Etch rate: 850 nm/min
- Selectivity: 8.5:1 for oxide hard mask
CCP: BCl$_3$ Recipe and Example (2)

- Fabrication example (proportional amplifier)
CCP: SF₆ Recipe and Example (1)

• System: Drytek DRIE-284
• Process parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>150 W</td>
</tr>
<tr>
<td>Pressure</td>
<td>150 mTorr</td>
</tr>
<tr>
<td>SF₆</td>
<td>30 sccm</td>
</tr>
<tr>
<td>O₂</td>
<td>10 sccm</td>
</tr>
</tbody>
</table>

• Etch rate: 4.2 μm/min
• Selectivity: 14.2:1 for oxide hard mask
CCP: SF$_6$ Recipe and Example (2)

- Fabrication example (vortex amplifier)
CCP: Poly-Si Etch Test (1)

- **System:** Drytek DRIE-284

- **Process parameter**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>300 W</td>
</tr>
<tr>
<td>Pressure</td>
<td>75~250 mTorr</td>
</tr>
<tr>
<td>Cl\textsubscript{2}</td>
<td>58 sccm</td>
</tr>
<tr>
<td>He\textsubscript{2}</td>
<td>100 sccm</td>
</tr>
</tbody>
</table>
CCP: Poly-Si Etch Test (2)

- Test results


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ICP: Poly-Si Etch Recipe of ISRC (1)

- System: STS ICP poly Etcher
- Process parameter (Br based etch)

<table>
<thead>
<tr>
<th></th>
<th>Step 1 (native oxide etch)</th>
<th>Step 2 (poly-Si etch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Coil</td>
<td>600 W</td>
<td>900 W</td>
</tr>
<tr>
<td>Platen</td>
<td>100 W</td>
<td>50 W</td>
</tr>
<tr>
<td>Pressure</td>
<td>2 mTorr</td>
<td>2 mTorr</td>
</tr>
<tr>
<td>Time</td>
<td>15 sec</td>
<td>60 sec</td>
</tr>
<tr>
<td>Temperature</td>
<td>20 °C</td>
<td>20 °C</td>
</tr>
<tr>
<td>Gas</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cl₂</td>
<td>20 sccm</td>
<td>0 sccm</td>
</tr>
<tr>
<td>HBr</td>
<td>0 sccm</td>
<td>20 sccm</td>
</tr>
<tr>
<td>O₂</td>
<td>0 sccm</td>
<td>1 sccm</td>
</tr>
</tbody>
</table>

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ICP: Poly-Si Etch Recipe of ISRC (2)

- Etch rate of poly-Si: 0.3 um/min
- Selectivity to PR: 3:1
- Selectivity to oxide: 100:1
- Etch profile: 88 ° to 90 °
ICP RIE System in ISRC (1)

- STS ICP poly Etcher (in CMOS area)
  - Plasma source type: ICP (inductively coupled plasma)
  - Main feed gas : HBr, Cl₂, Ar, SF₆, O₂, He₄
  - Main power: 13.56 MHz – 1000 W
  - Bias power: 13.56 MHz - 30/300 W
ICP RIE System in ISRC (2)

- STS ICP poly etcher for MEMS
  - Plasma source type: ICP (inductively coupled plasma)
  - Pump
    - Dry pump: Edwards iH80 800 ℓ/m
    - Turbo pump Leybold MAG 1500 CT 1000 ℓ/sec
  - RF generator
    - ENI ACG-10B 1000 W, 13.56 MHz
    - ENI ACG-3B 300 W, 13.56 MHz
  - Gas
    - HBr – 50 sccm
    - Cl2 – 20 sccm
    - O2 – 20 sccm
    - Ar – 50 sccm
## Various Gas for Poly-Si Etching

<table>
<thead>
<tr>
<th>Gas</th>
<th>Reactor Type</th>
<th>Pressure (torr)</th>
<th>Etch Rate (μm/min)</th>
<th>Etch Selectivity</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCl₄/Argon</td>
<td>Planar</td>
<td>.4</td>
<td>.02(Undoped)</td>
<td>Poly Si : SiO₂</td>
<td>15:1</td>
</tr>
<tr>
<td>SiF₄(50%)/Argon(50%)</td>
<td>Planar</td>
<td>.2</td>
<td>.4(Undoped)</td>
<td>Poly Si : SiO₂</td>
<td>25:1</td>
</tr>
<tr>
<td>CF₄/O₂</td>
<td>Barrel</td>
<td>.2</td>
<td>.05 ~ .1(Undoped)</td>
<td>Poly Si : Si₃N₄ : SiO₂</td>
<td>25 : 2.5 : 1</td>
</tr>
<tr>
<td>CF₄/O₂(4%)</td>
<td>Planar</td>
<td>.4</td>
<td>.057(Phos doped)</td>
<td>Poly Si : SiO₂</td>
<td>10:1</td>
</tr>
<tr>
<td>C₂ClF₃</td>
<td>Planar</td>
<td>.225</td>
<td>.05(Phos doped)</td>
<td>Poly Si : SiO₂</td>
<td>3.5 :1</td>
</tr>
<tr>
<td>CF₄(92%)/O₂(8%)</td>
<td>Planar</td>
<td>.35</td>
<td>.115(Phos doped)</td>
<td>Poly Si : SiO₂</td>
<td>10:1</td>
</tr>
<tr>
<td>C₂F₄(50%)/CF₃Cl(50%)</td>
<td>Planar</td>
<td>.4</td>
<td>.159(Phos doped)</td>
<td>Poly Si : SiO₂</td>
<td>8:1</td>
</tr>
<tr>
<td>C₂F₄(81%)/CF₃Cl(19%)</td>
<td>Planar</td>
<td>.4</td>
<td>.082(Phos doped)</td>
<td>Poly Si : SiO₂</td>
<td>5:1</td>
</tr>
<tr>
<td>C₂F₄(92%)/Cl₂(8%)</td>
<td>Planar</td>
<td>.35</td>
<td>.057(Phos doped)</td>
<td>Poly Si : SiO₂</td>
<td>6:1</td>
</tr>
<tr>
<td>CF₃Cl</td>
<td>Planar</td>
<td>.35</td>
<td>.08(Phos doped)</td>
<td>Poly Si : SiO₂</td>
<td>13:1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>.03(Undoped)</td>
<td>Poly Si : SiO₂</td>
<td>6:1</td>
</tr>
</tbody>
</table>

Deep Reactive Ion Etching (1)

- Uses high density plasma to alternatively etch silicon and deposit etch resistant polymer on sidewall
  - Unconstrained geometry 90° side walls
  - High aspect ratio 1:30
  - Easily masked (PR, SiO₂)
- Bosch process: sidewall passivation → etch → sidewall passivation → etch ...

![Diagram showing phases of Deep Reactive Ion Etching](image)
Deep Reactive Ion Etching (2)

- Characteristics of the Deep RIE process
  - $\text{SF}_6$ flow: 30 ~ 150 sccm
  - $\text{C}_4\text{F}_8$ flow: 20 ~ 100 sccm
  - Etch cycle: 5 ~ 15 sec
  - Deposition cycle: 5 ~ 12 sec
  - Pressure: 0.25 ~ 10 Pa
  - Temperature: 20 ~ 80 °C
  - Etch rate: 1.5 ~ 4 um/min
  - Selectivity to resist mask: more than 75:1
  - Selectivity to oxide mask: more than 150:1
  - Sidewall angle: $90^\circ \pm 2$
  - Etch depth capability: up to 500 um
Deep Reactive Ion Etching (3)

- Fence (levee) structure and trench (furrow) structure have different etch side wall profile
Deep Reactive Ion Etching (4)

- Characteristics of Bosch process
  - Scalloping
  - Under cut
Deep RIE Example (1)

- Fabrication example (deep trench)

350 μm-depth
100 μm-depth
80 μm-depth, 4.5 μm space width, 2 μm line width
Deep RIE Example (2)

- Fabrication example (IMU device)

Gyroscope

Accelerometer (170/μm-depth)
RIE Lag in Deep RIE Process

- RIE lag (microloading effect)
  - Etch rate of a wafer with a larger open area is different from the wafer with a smaller open area
  - Smaller hole has a lower etch rate than the larger holes
  - Etchants are more difficult to pass through the smaller hole
  - Etch byproducts are harder to diffuse out
  - Lower pressure can minimize the effect.

Plasma-Therm, SLR-7701-10R-B data
Footing in Deep RIE Process (1)

- Footing

![Diagram of footing in Deep RIE Process]

Toppled structures
Footing in Deep RIE Process (2)

- Footing formation
  - There is notching at the foot of the silicon trench in a conventional deep RIE of SOI substrate due to charge accumulation at the base of the trench.
Footing in Deep RIE Process (3)

- Footing SEM pictures

Notching

Fragments
Reducing Footing Phenomenon in SOI Process

- Deep RIE with SOI kit (Surface Technology Systems, STS)
  - A conventional approach to reduce footing (notching) is to increase the passivation during the overetch
  - This increase process time and is only practical for similar feature sizes with short overetch time
  - The SOI kit on the system controls the charging and hence broadens the process window significantly without increased passivation

Deep etched trench in 20 um SOI layer with good profile and notch control (8 um gap)

Isolated 10 um line features deep etched in a 20 um SOI layer with notch control (8 um gap centre, 500 um gap either side)
Reducing Footing Phenomenon in SOG Process

- Prevention method of a notching caused by surface charging
  - To prevent silicon from a notching in deep RIE process by introducing a self-aligned metal interlayer to a silicon/glass bonded fixture.
  - A metal interlayer prevents a charge buildup at the bottom of a silicon trench, therefore silicon structures do not suffer from charge-induced local damage.

An automatically aligned metal interlayer prevents silicon from notching by fast charge relaxation.

Test result for a simple trench: a 5 μm width silicon trench processed (Left picture) without a self-aligned metal interlayer (Right picture) with a self-aligned metal interlayer.
Latest Deep RIE in ALCATEL

- AMS 4200 for volume production cluster platform
  - Each process module is fitted with an Alcatel patented high-density ICP type plasma source.
  - The source is fixed on top of a diffusion chamber surrounded by a number of permanent magnets.
  - Achievements of the DRIE:
    - Profile control
    - High mask selectivity: >300:1
    - Super High Aspect Ratio: >100:1
Latest Deep RIE in STS

- **STS’ Pegasus Systems**
  - The Power Handling capability is improved
    - Improved Etch Rates
  - The plasma generation area is larger
    - Improved Etch Rates
    - Enhanced Etch Uniformity
  - Produces a neutral high radical density in the centre of the wafer and a uniform ion density across the whole wafer surface
    - Enhanced Etch Depth Uniformity
    - Improved Feature profile control

- The STS Pegasus system offer full compatibility with CMOS fabs and foundries
  - No Electrostatic Damage
  - Excellent Particle Control
  - Low Ionic / Metal Contamination

**ER** 9.91μm/min
**Profile** 91.65 deg
**Selectivity**: PR 117:1
Deep RIE I in ISRC (1)

- ICP deep silicon RIE (in MEMS area, for 4 inch wafer)
- Plasma-Therm, SLR-7701-10R-B
- Plasma source type: ICP (inductively coupled plasma)
- High aspect ratio up to 20~30
- Feature
  - 2 kW, ICP source and 500W bias power
  - gas line: C₄F₈, SF₆, Ar, O₂, NF₃, C₂F₆

<table>
<thead>
<tr>
<th></th>
<th>Deposition</th>
<th>Etch A</th>
<th>Etch B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time (sec)</td>
<td>5</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Gas (sccm)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C₄F₈</td>
<td>100</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>SF₆</td>
<td>0.5</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>Ar</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Power (W)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RF1 (bias)</td>
<td>1</td>
<td>13</td>
<td>13</td>
</tr>
<tr>
<td>RF2 (source)</td>
<td>825</td>
<td>825</td>
<td>825</td>
</tr>
<tr>
<td>Pressure (mTorr)</td>
<td>22</td>
<td>23</td>
<td>23</td>
</tr>
</tbody>
</table>
Deep RIE I in ISRC (2)

- Etch rate: 2.35 um/min (at 500 um opening)

- Under cut at the top of 4 um line & space: 0.4 um
- RIE lag (2 um/4 um): 24% etch rate difference

- Selectivity to resist mask: 75:1
- Selectivity to oxide mask: 199:1

- Sidewall profile (levee): 88.5°
- Sidewall profile (furrow): 90°

- Etch depth capability: up to 500 um
Deep RIE I in ISRC (3)

5.2 μm

74 μm

Dong-il "Dan" Cho
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Deep RIE II in ISRC (1)

- ICP deep silicon RIE II (in MEMS area, for 6 inch wafer)
- OERLIKON, Versaline
- Plasma source type: ICP (inductively coupled plasma)
- High aspect ratio up to 20~30
- Pump
  - Dry pump: Alcatel ADP122P 1,500ℓ/min
  - Turbo pump: Edwards STP-A1303CV 900ℓ/sec
- RF generator
  - PM, Coil: 2500W 2MHz
  - Electrode: 600W, 13.56MHz

<table>
<thead>
<tr>
<th>Time (sec)</th>
<th>Deposition</th>
<th>Etch A</th>
<th>Etch B</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>150</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>0</td>
<td>250</td>
<td>250</td>
</tr>
<tr>
<td>1</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Gas (sccm)</th>
<th>Deposition</th>
<th>Etch A</th>
<th>Etch B</th>
</tr>
</thead>
<tbody>
<tr>
<td>C₄F₈ 150</td>
<td>0</td>
<td>250</td>
<td></td>
</tr>
<tr>
<td>SF₆ 0</td>
<td>30</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>Ar 30</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Deposition</th>
<th>Etch A</th>
<th>Etch B</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF1 (ICP) 2000</td>
<td>250</td>
<td>250</td>
<td>2500</td>
</tr>
<tr>
<td>RF2 (source) 150</td>
<td>40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pressure (mTorr)</td>
<td>25</td>
<td>40</td>
<td>70</td>
</tr>
</tbody>
</table>
Deep RIE II in ISRC (2)

- Process parameter of High Rate 2 um recipe
  - Etch rate: 4 um/min
  - Aspect ratio: 25
  - Selectivity to resist mask: > 100:1
  - Selectivity to oxide mask: > 200:1
  - Uniformity: 1.2%
  - Verticality: 90°±1
  - Undercut: 150 nm
  - Scallop pitch: 160 nm
  - Scallop depth: 50 nm
Deep RIE II in ISRC (3)

- Process results using ‘SNU High Etch Rate 2 um’ recipe
Deep RIE II in ISRC (4)

- Process results using ‘SNU SOI’ recipe
  - Anti-footing recipe for SOI process

5 μm line width

20 μm line width

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Reference


Reference


RIE Principles (2)

- Basic steps in a plasma etching process

1. Generation of etching species
2. Diffusion to surface
3. Adsorption
4. Reaction
5. Desorption and diffusion into bulk gas

Plasma flowing gas

Stagnant gas layer

Thick film or bulk silicon