

# **PVD and CVD**

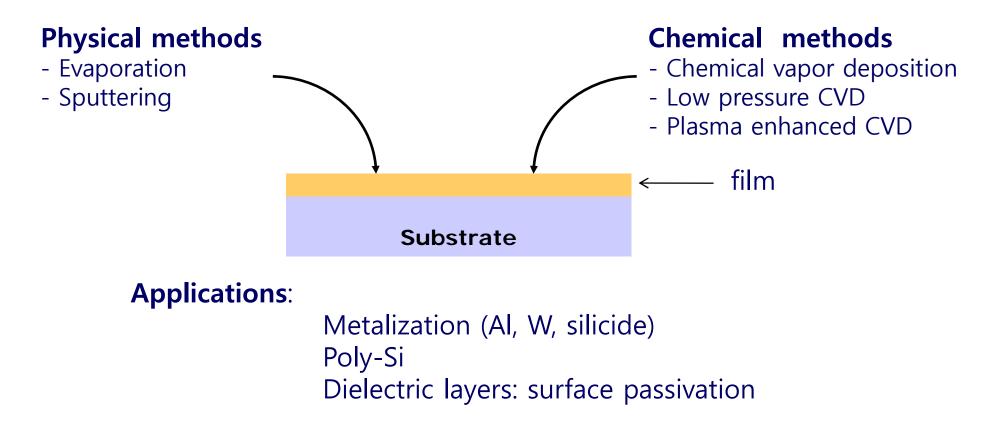
#### (Physical Vapor Deposition and Chemical Vapor Deposition)

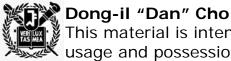
#### Dong-Il "Dan" Cho

School of Electrical Engineering and Computer Science, Seoul National University Nano/Micro Systems & Controls Laboratory

# Thin Film Deposition (1)

- Deposition •
  - The transformation of vapors into solids, frequently used to grow solid thin film and powder materials





Nano/Micro Systems & Controls Lab.

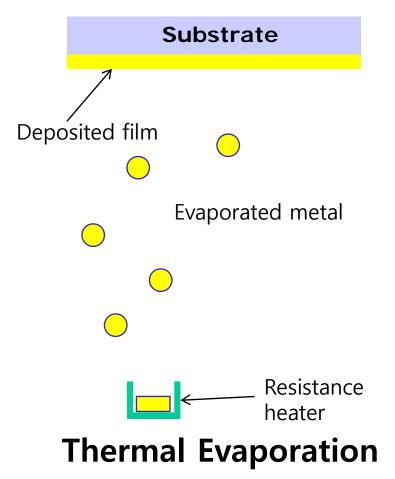
This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

# Thin Film Deposition (2)

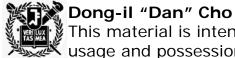
- Physical Vapor Deposition (PVD)
  - Direct impingement of particles on the hot substrate surface
  - Thermal evaporation, electron-beam evaporation, sputtering
- Chemical Vapor Deposition (CVD)
  - Convective heat and mass transfer as well as diffusion with chemical reactions at the substrate surfaces
  - More complex process than PVD
  - More effective in terms of the rate of growth and the quality of deposition
  - LP/AP CVD, Thermal/PE/Ph/LC CVD



# **PVD** : Evaporation (1)



Gas Pressure : 10<sup>-5</sup> Torr



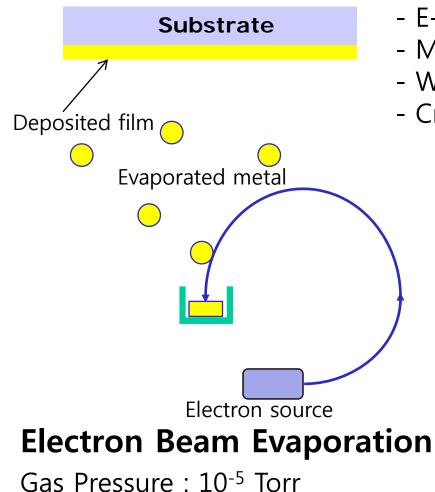
Dong-il "Dan" Cho Nano/Micro Systems & Controls Lab. This material is intended for students in 4541.844 class in the Spring of 2009. Any other

usage and possession is in violation of copyright laws

- Thermal evaporator
- Materials: Au, Al, Ti, Cu, Ni, Cr, Ag, Co, Sn, Pd



#### **PVD** : Evaporation (2)



- E-gun evaporator
- Materials: Ti, Cr, Au, Al, Ni, Ag
- Within wafer uniformity: < 5%
- Crucible liner 6pocket crucible

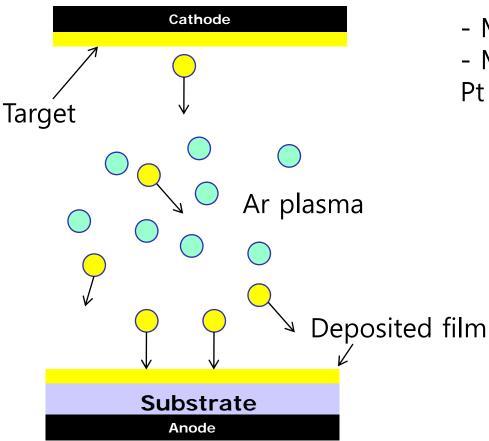


Dong-il "Dan" Cho

Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

# **PVD** : Sputtering (1)



- Metal sputter

- Materials: Cr, Mo, Ti, Cu, Al, W, Ni, Pt



#### Gas Pressure : 1~ 10 mTorr



# **PVD : Sputtering (2)**

- Wavics sputter
- Materials: Ti, Al, Mo, Cu



- Au sputter
- Materials: Au, Ti (adhesion, Cr (adhesion)
- Within wafer uniformity: < 5%
- Wafer heating : 20°C ~ 250°C





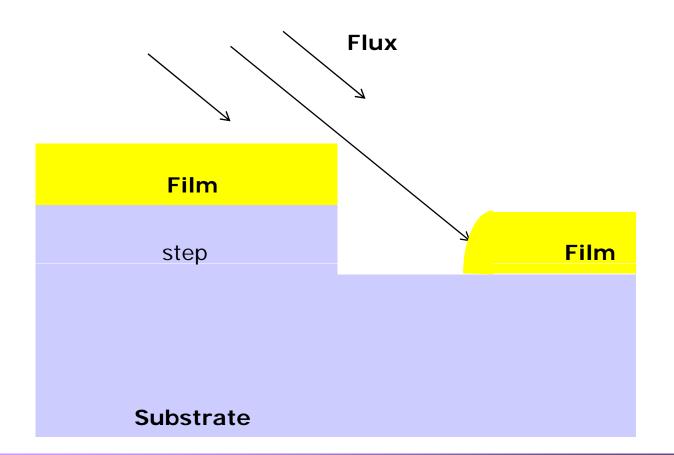
#### **Thermal evaporation VS Sputtering**

	Thermal Evaporation	Sputtering	
Rate	Thousand atomic layers at a time	On atomic layer at a time	
Choice of materials	Limited	Almost unlimited	
Surface damage	Very low	Ionic bombardment damage	
Adhesion	Poor	Good (on most materials)	
Uniformity	Difficult to control	Easy to control	
Film properties	Difficult to control	Can be controlled by pressure and temperature	
Step coverage	↓↓↓↓↓↓↓↓↓↓↓↓↓↓ ↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓↓	$\begin{array}{c} \begin{array}{c} \begin{array}{c} \begin{array}{c} \end{array} \\ \end{array} \\ \end{array} \\ \end{array} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} \\ \end{array} \\ \end{array} \\ \begin{array}{c} \end{array} \\ \end{array} $	



#### Step coverage problem with PVD (1)

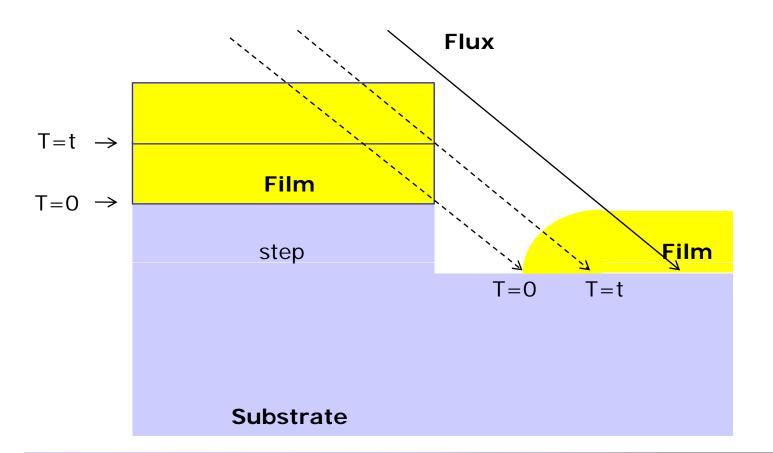
Geometrical shadowing •





#### Step coverage problem with PVD (2)

• Self-shadowing





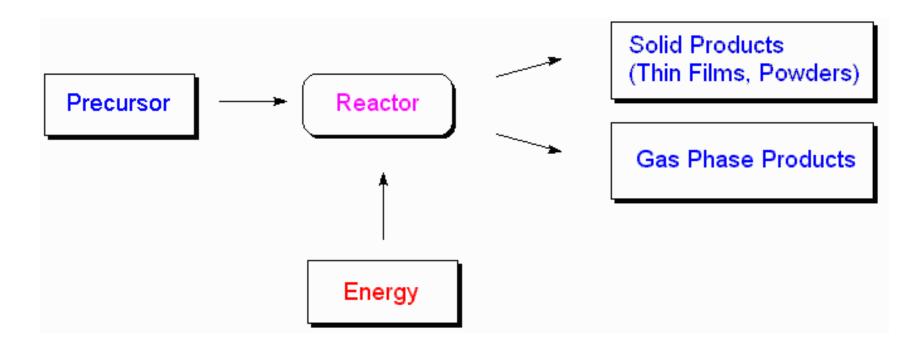
#### Methods for minimizing step coverage problems

- Rotate +Tilt substrate during deposition 1.
- Elevate substrate temperature (enhance surface diffusion) 2.
- Use large-area deposition source 3.



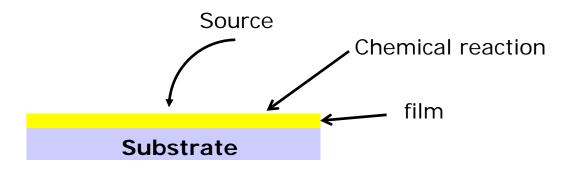
#### **Chemical Vapor Deposition (1)**

- What is Chemical Vapor Deposition? •
  - Chemical reactions which transform gaseous molecules, called precursor, into a solid material, in the form of thin film or powder, on the surface of a substrate

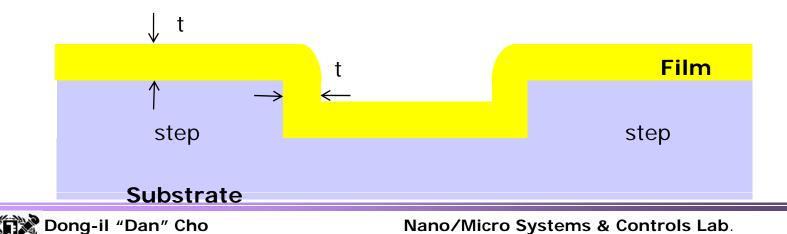




#### **Chemical Vapor Deposition (2)**



#### More conformal deposition vs. PVD



This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

#### **CVD** Reactor Parameters

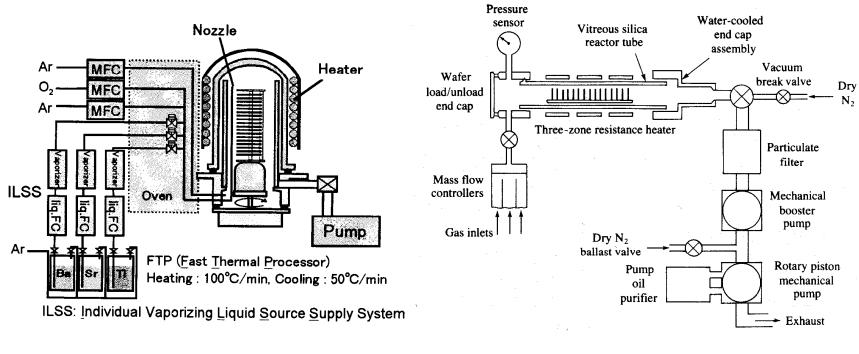
Parameters	Variations	
Temperature range	Low, Medium, High	
Deposition pressure	ATM, Low	
Reactor geometry / Wall temp.	Hot wall, Cold wall	
Energy source	Temp., R.F, UV-light	
Deposition film	Dielectric, Metal	
Reactant / Carrier gases	Metal Organic, Inorganic	



Dong-il "Dan" ChoNano/Micro Systems & Controls Lab.This material is intended for students in 4541.844 class in the Spring of 2009. Any other

usage and possession is in violation of copyright laws

#### **Examples : CVD reactors (1)**

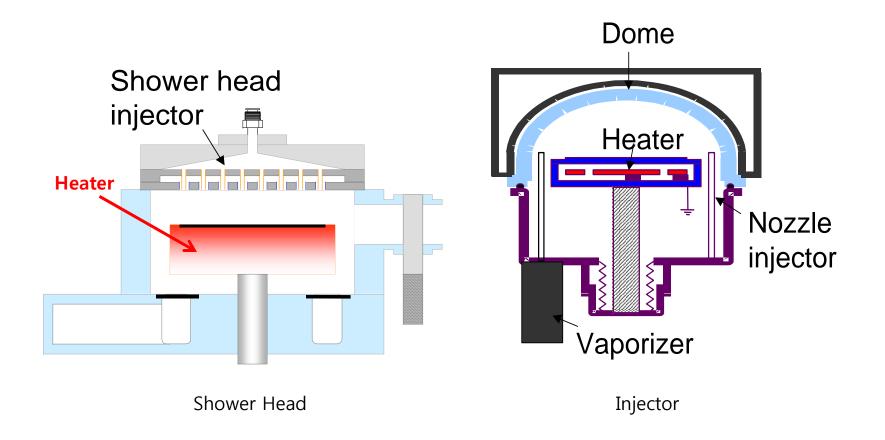


Vertical CVD Reactor

Horizontal CVD Reactor



**Examples : CVD reactors (2)** 





#### **CVD** systems

Туре	Advantage	Disadvantage	Usage	Pressure/temp
APCVD Atmospheric pressure CVD	Simple, fast	Poor step coverage	Low temp oxides	10 ~ 100 kPa 350 ~ 1200 °C
LPCVD Low pressure CVD	Excellent cleanness, conformity and uniformity	High temp, low deposition rate	Polysilicon, nitride, oxide	100 Pa 550 ~ 600 °C
PECVD Plasma enhanced CVD	Low temp	Risc for particle and chemical contamination	Low temp oxides, passivation nitrides	200 ~ 600 Pa 300 ~ 400 °C

APCVD is mass transport controlled, LPCVD is surface reaction controlled



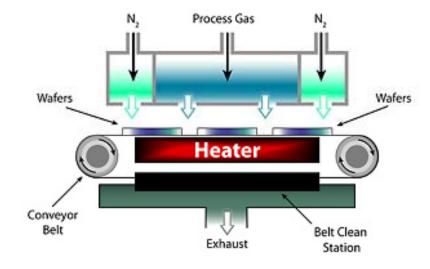
Dong-il "Dan" Cho

Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

#### **Atmospheric Pressure CVD**

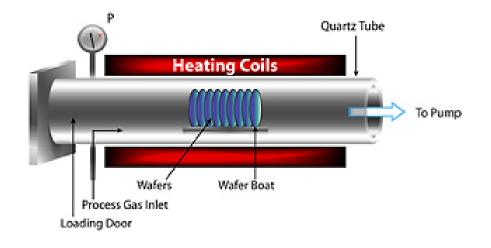
- APCVD (Atmospheric Pressure Chemical Vapor Deposition)
  - High deposition rate, poor uniformity, high contamination level, 250-450 ℃
  - Cold wall process
  - Material: epitaxial Si, poly-Si, Si<sub>3</sub>N<sub>4</sub>, SiO<sub>2</sub>, etc.





#### Low Pressure CVD

- LPCVD (Low Pressure Chemical Vapor Deposition)
  - Low deposition rate, high uniformity, 575-650 ℃
  - Good uniformity, property
  - Material: Si<sub>3</sub>N<sub>4</sub>, SiO<sub>2</sub>, poly-Si, etc.





#### LPCVD at ISRC (2)

Process name	POLY Si		
Dep. Temp.	622℃ / 624℃ / 625℃	Dep. rate	100Å/min
Gas	SiH4 : 60sccm		
Process pressure	270mTorr		

Process name	α -Si		
Dep. Temp.	549.5℃ / 555℃ / 555℃ Dep. rate 24Å/mi		24Å/min
Gas	SiH4 : 60 sccm		
Process pressure	250 mTorr		

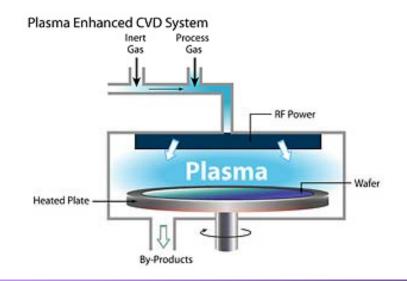
Process name	Low stress Nitride		
Dep. Temp.	825℃ / 828℃ / 825℃	Dep. rate	27Å/min
Gas	DCS-L: 21sccm, DCS-R: 30sccm,NH3-L:3.5sccm,NH3-L:5sccm		
Process pressure	150mTorr		

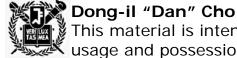




#### Plasma Enhanced CVD (1)

- PECVD (Plasma Enhanced Chemical Vapor Deposition)
  - Ionized chemical species allows a lower process temperature.
  - Film properties can be tailored by controllable ion bombardment with substrate bias voltage.
  - Material:  $Si_3N_4$ ,  $SiO_2$ , amorphous-Si, etc.
  - Faster rate and lower deposition temperature than thermal CVD
  - Cracks, pin holes, and poor stoichiometry





Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

#### Plasma Enhanced CVD at ISRC (2)

P-5000 II •

RF power	Pressure	Gas	Dep. R ate	
(W)	(Torr)	TEOS	O <sub>2</sub>	(Å/min)
350	9	220	220	About 100





#### Plasma Enhanced CVD at ISRC (3)

• STS PECVD

51512675					
Nitride					
Gas flo 5%SiH <sub>4</sub> /N <sub>2</sub>	w (sccm NH₃	i) N <sub>2</sub>	Pressure (mTorr)		
800	10	1200	580	Low Frequency (187kHz), 60W	160
			O>	vide	
Gas flc 5%SiH <sub>4</sub> /N <sub>2</sub>	w (sccn NH <sub>3</sub>	n) N <sub>2</sub>	Pressure (mTorr)	RF power (W)	Dep. rate (Å/min)
160	1500	240	550	Low Frequency (187kHz), 60W	340
	Oxinitride				
Gas flo 5%SiH <sub>4</sub> /N <sub>2</sub>	w (sccm NH <sub>3</sub>	i) N <sub>2</sub>	Pressure (mTorr)	RF power (W)	Dep. rate (Å/min)
800	250	60	580	Low Frequency (187kHz), 60W	300
Low stress nitride					
Gas flo 5%SiH <sub>4</sub> /N <sub>2</sub>	w (sccm NH <sub>3</sub>	i) N <sub>2</sub>	Pressure (mTorr)	RF power (W)	Dep. rate (Å/min)
800	10	1200	580	High Frequency (13.56MHz) : 20W(6sec), Low Frequency (187kHz) : 20W(1.5sec)	100



Systems & Controls Lab. the Spring of 2009. Any other

#### **Common CVD films**

Thin film	Typical Reactions	Equipment	Comments
SiO <sub>2</sub>	SiH <sub>4</sub> + O <sub>2</sub> $\rightarrow$ SiO <sub>2</sub> + H <sub>2</sub> Si(OC <sub>2</sub> H <sub>5</sub> ) <sub>4</sub> (+O <sub>3</sub> ) $\rightarrow$ SiO <sub>2</sub> + byproducts	LPCVD, PECVD, HDPCVD	200 ~ 800 °C 200 ~ 500 °C (LTO) – may require high T anneal. 25 ~ 400 °C (TEOS-ozone, PECVD, HDPCVD)
Si <sub>3</sub> N <sub>4</sub>	$3SiH_4 + 4NH_3 \rightarrow$ $Si_3N_4 + 12H_2$ $3SiH_2CI_2 + 4NH_3 \rightarrow$ $Si_3N_4 + 6N_2 + 6HCI$	LPCVD, PECVD	650 ~ 800 °C for oxidation mask 200 ~ 400 °C (PECVD) for passivation
Poly- silicon	Same as epitaxial Si	LPCVD	575 to 800 °C Grain structure depends on deposition conditions and doping
Epitaxial silicon	SiH <sub>4</sub> $\rightarrow$ Si + 2H <sub>2</sub> SiCl <sub>4</sub> + 2H <sub>2</sub> $\rightarrow$ Si + 4HCl Also SiHCl <sub>3</sub> , SiH <sub>2</sub> Cl <sub>2</sub>	APCVD, LPCVD	1000 ~ 1250 °C If using reduced pressure, 700 to 900 °C



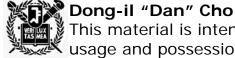
#### **CVD** Chemistries (1)

- Silicon Oxide •
  - Dry oxidation : Si +  $O_2 \rightarrow SiO_2$
  - Wet Oxidation : Si +  $2H_2O \rightarrow SiO_2 + 2H_2$
  - SiH<sub>4</sub> + O<sub>2</sub>  $\rightarrow$  SiO<sub>2</sub> + 2H<sub>2</sub>
  - SiH<sub>4</sub> + N<sub>2</sub>O  $\rightarrow$  SiO<sub>2</sub> + byproducts
  - SiCl<sub>2</sub>H<sub>2</sub> + N<sub>2</sub>O  $\rightarrow$  SiO<sub>2</sub> + byproducts
  - Si(OC<sub>2</sub>H<sub>5</sub>)<sub>4</sub>  $\rightarrow$  SiO<sub>2</sub> + byproducts



# **Example : Silicon dioxide**

- Thermally driven reaction
  - Mid-temperature : ~ 500 °C
    - "LTO" (low-temp. oxide) T < ~ 500 °C
  - SiH<sub>4</sub> + O<sub>2</sub>  $\rightarrow$  SiO<sub>2</sub> + H<sub>2</sub>
  - Cold-wall, atmospheric, ~ 0.1 μm/min
  - Hot-wall, LPCVD, ~ 0.01 μm/min
- Plasma-enhanced reaction (PECVD)
  - Low temperature : ~ 250 °C
- High temperature: ~ 700 °C
  - Tetraethyl orthosilicate (TEOS)
    - Si(OC<sub>2</sub>H<sub>5</sub>)<sub>4</sub>  $\rightarrow$  SiO<sub>2</sub> + byproducts



Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

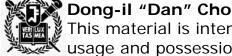
#### **CVD** Chemistries (2)

- Silicon Nitride •
  - $-3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$
  - $3SiH_2CI_2 + 4NH_3 \rightarrow Si_3N_4 + byproducts$
  - $3SiH_4 + 4N_2O \rightarrow Si_3N_4 + byproducts$
  - $3SiH_4 + N_2 \rightarrow Si_3N_4 + byproducts$



# **Example : Silicon nitride**

- Uses
  - Diffusivity of  $O_2$ ,  $H_2$  is very low in nitride
    - Mask against oxidation, protect against water/corrosion
  - Diffusivity of Na also very low
    - Protect against mobile ion contamination
- Deposition
  - Stoichiometric formulation is  $Si_3N_4$ 
    - In practice Si/N ratio varies from 0.7 (N rich) to 1.1 (Si rrich)
  - IPCVD : ~ 700 °C ~ 900 °C
    - $3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2$ ;  $3SiH_2CI_2 + 4NH_3 \rightarrow Si_3N_4 + 6N_2 + 6N_2$ 6HC
    - $\rho$  : ~ 3 g/cm<sup>3</sup>
    - Stress : ~ 10 Gdyne/cm<sup>2</sup>, tensile
  - PECVD
    - $aSiH_4 + bNH_3 \rightarrow Si_xN_yH_z + cH_2$ ;  $aSiH_4 + bN_2 \rightarrow Si_xN_yH_z + cH_2$
    - ρ: 2.4 ~ 2.8 g/cm<sup>3</sup>
    - Stress : ~2C ~5T Gdyne/cm<sup>2</sup>



#### Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

#### **CVD** Chemistries (3)

- Poly-silicon : SiH<sub>4</sub>  $\rightarrow$  Si + 2H<sub>2</sub> •
- Silicon Carbide
- Polycrystalline Diamond
- Parylene (polymerized p-xylylene)
- Refractory Metals :  $2WF_6 + 3SiH_4 \rightarrow 2W + 3SiF_4 + 6H_2$ ٠
- **II-VI** compounds ٠



#### Exaple : polysilicon

- Uses
  - Gates, high value resistors, "local" interconnects
- Deposition
  - − Silane pyrolysis : 600 ~ 700 °C , SiH<sub>4</sub>  $\rightarrow$  Si + 2H<sub>2</sub>
    - Atmospheric, cold wall, 5% silane in hydrogen, ~1/2  $\mu m/min$
    - LPCVD (~ 1 Torr), hot wall, 20 ~ 100% silane, ~ hundreds nm/min
  - Grain size dependent on growth temperature, subsequent processing
    - 950 °C phosphorus diffusion, 20 min; ~ 1  $\mu$ m grain size
    - 1050 °C oxidation; 1~3  $\mu m$  grain size
- In-situ doping
  - P-type: diborane B<sub>2</sub>H<sub>6</sub>
    - Can cause substantial increase in deposition rate
  - N-type: arsine AsH<sub>3</sub>, phosphine PH<sub>3</sub>
    - Can cause substantial decrease in deposition rate
- Dope after deposition (implant, diffusion)

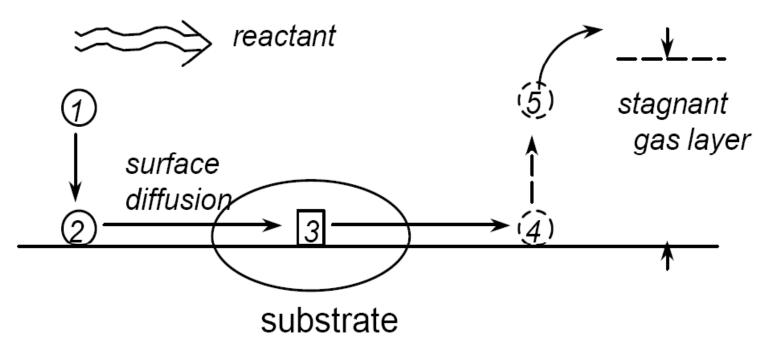


🞇 Dong-il "Dan" Cho

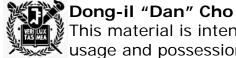
#### Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

#### **CVD** mechanisms



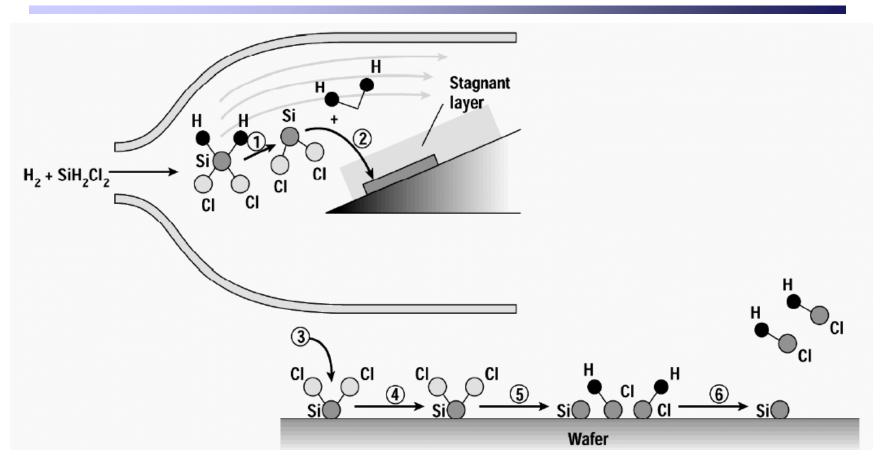
- 1 = Diffusion of reactant to surface
- 2 = Absorption of reactant to surface
- 3 = Chemical reaction
- 4 = Desorption of gas by-products
- 5 = Outdiffusion of by-product gas



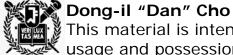
Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

#### **Example Poly-Si deposition**



(1) gas-phase decomposition and (2) transport to the surface of the wafer. At the surface the growth species must (3) adsorb, (4) diffuse, and (5) decompose, and (6) the reaction byproducts are desorbed.



Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

# Kinetics of CVD thin film deposition (1)

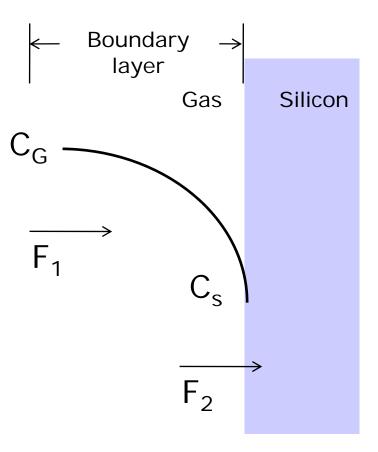
- We consider the fluxes for the two important process such as mass transfer and surface reaction
- $F_1$  = diffusion flux of reactant species to the wafer = mass transfer flux.

 $\mathbf{F}_1 = \mathbf{h}_G(\mathbf{C}_G - \mathbf{C}_S)$ 

- Where  $(C_G C_S)$  term is the difference in concentration of the reactants species between the main gas flow and the wafer surface, and  $h_G$  is the mass transfer coefficient.
- Similarly, F2 = flux of reactant consumed by the surface reaction = surface reaction flux.

#### $F_2 = K_s C_s$

Where  $K_s$  is the chemical surface reaction rate and  $C_s$  is the concentration of the reacting species at the surface.



Dong-il "Dan" Cho

Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other 33usage and possession is in violation of copyright laws

# Kinetics of CVD thin film deposition (2)

1

• In steady state

$$\mathbf{F_1} = \mathbf{F_2} \rightarrow \mathbf{C}_{\mathrm{S}} = \frac{\mathbf{h}_{\mathrm{G}}}{(\mathbf{h}_{\mathrm{G}} + \mathbf{k}_{\mathrm{S}})} \mathbf{C}_{\mathrm{G}}$$

#### **Growth Rate**

 $R_G = F_2/N_{Si}$  (N<sub>Si</sub> : # of Si atoms in a unit volume)

$$R_{G} = \frac{1}{N_{Si}} \frac{h_{G}k_{S}}{h_{G} + k_{S}} C_{G}$$

Surface reaction rate

$$k_s = k_o exp(-\frac{E_A}{kT})$$

E<sub>A</sub>: activation energy

#### k: Boltzmann constant



**Dong-il "Dan" Cho** This material is intended for

Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other <sup>34</sup> usage and possession is in violation of copyright laws

# Kinetics of CVD thin film deposition (3)

- Limiting cases of growth rate •
  - If  $K_S << h_{G'}$  then we have the surface reaction controlled case: 1.

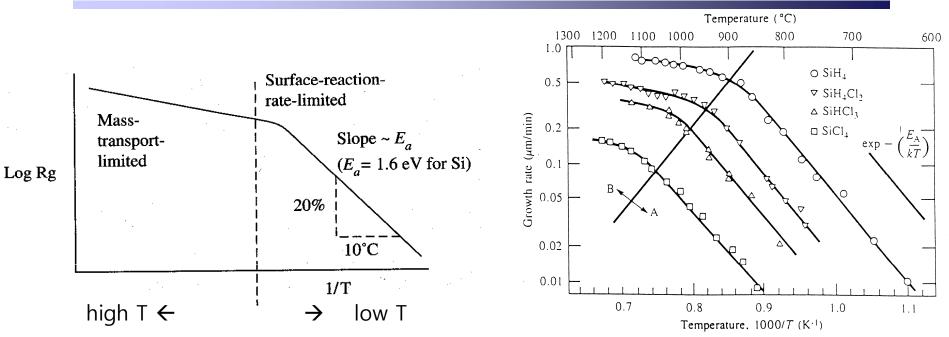
$$R_{G} = \frac{1}{N_{Si}}k_{S}C_{G}$$

If  $h_G << K_{S'}$ , then we have the mass transfer, or gas phase 2. diffusion controlled case:

$$R_{G} = \frac{1}{N_{Si}} h_{G} C_{G}$$



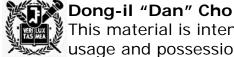
#### **Deposition rate versus Temp**



- K<sub>s</sub> limited deposition is **VERY temp sensitive**.
- h<sub>G</sub> limited deposition is **VERY geometry sensitive**.
- Si epi deposition often done at high T to get high quality single crystal growth.

 $\therefore$  h<sub>G</sub> controlled.

• Polysilicon is usually deposited at lower temperature surface reaction regime.

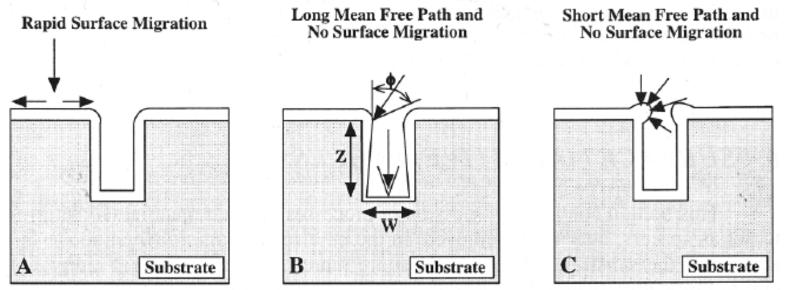


Dong-il "Dan" ChoNano/Micro Systems & Controls Lab.This material is intended for students in 4541.844 class in the Spring of 2009. Any other

usage and possession is in violation of copyright laws

## **Step Coverage Profile (1)**

Step coverage profile



- A: Rapid surface migration process (before reaction), yielding uniform coverage since reactants adsorb and move, then react
- B: Long mean free path process and no surface migration, with reactant molecule arrival angle determined location on features (local "field of view" effects are important)
- C: Short mean free path process with no surface migration, yielding nonconformal coating



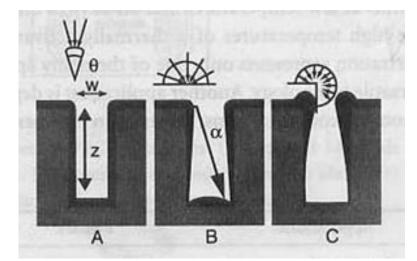
Dong-il "Dan" Cho This material is intended for students in 4541.844 class in the Spring of 2009. Any other

Nano/Micro Systems & Controls Lab.

usage and possession is in violation of copyright laws

## **Step Coverage Profile (2)**

- Key Parameters
  - Mean Free Path
  - Surface Migration Energy ( $E \propto Temperature$ )
  - Arrival angle
- For conformal step coverage
  - $-\alpha$  < I (mean free path)
  - $\alpha = \arctan(w/z)$
  - High Surface Mobility
- Process tendency
  - A: LPCVD
  - B: PFCVD



**Evaporated & Sputtered Metal** 



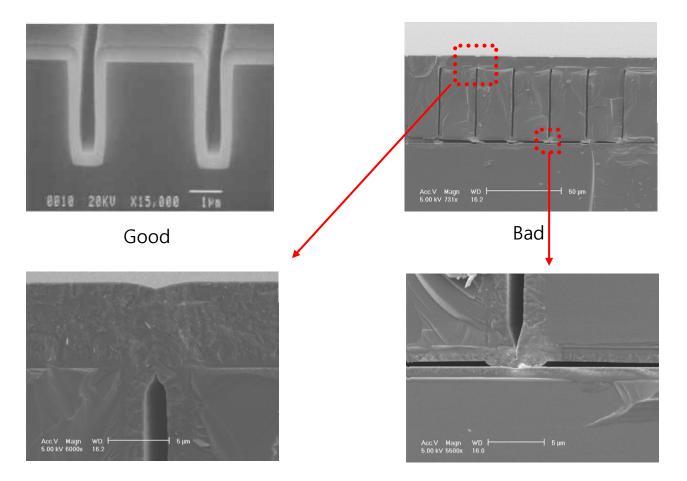
💥 Dong-il "Dan" Cho

Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

#### **Step Coverage Profile (3)**

Step coverage profile example ٠

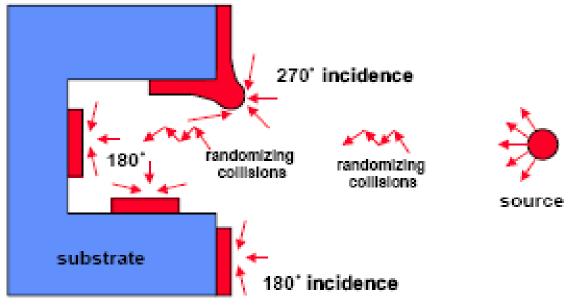




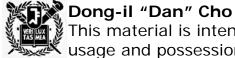
Dong-il "Dan" Cho Nano/Micro Systems & Controls Lab. This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

# Impact of pressure on deposition conditions (1)

- Material arrival angular distribution
  - Depends on mean free path compared to both size of system and size of wafer "steps"
- Case I: "atmospheric pressure": 760 Torr  $\rightarrow \lambda = 0.07 \ \mu m$ 
  - Isotropic arrival on ALL surfaces



Assume material does not migrate after arrival.

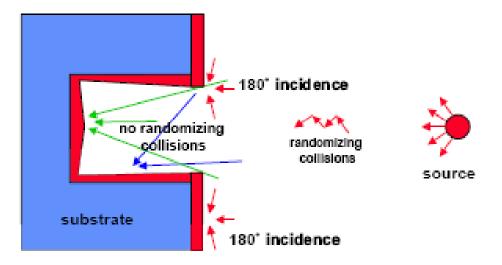


Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

## Impact of pressure on deposition conditions (2)

- Case II: 10<sup>-1</sup> Torr  $\rightarrow \lambda = 0.5$  mm
  - Small compared to system, large compared to wafer features
  - Isotropic arrival at "flat" surface
- But no scattering inside "hole"
  - Shadowing by corners of features
  - "anisotropic" deposition



Assume material does not migrate after arrival.

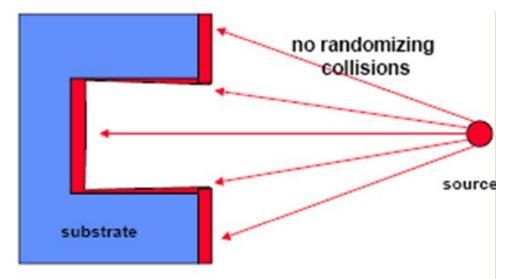


Nano/Micro Systems & Controls Lab.

Dong-il "Dan" Cho This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

## Impact of pressure on deposition conditions (3)

- Case II: 10<sup>-5</sup> Torr  $\rightarrow \lambda = 5$  m
  - Long compared to almost everything
- Anisotropic arrival at all surfaces
  - Very thin on "side walls"
  - Very dependent on source configuration relative to sample surface



Assume material does not migrate after arrival.

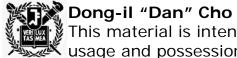


Nano/Micro Systems & Controls Lab.

Dong-il "Dan" Cho This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

### **Dielectric deposition applications summary**

Application	Film	Requirements	System
Shallow Trench Isolation polish stop layer.	Si <sub>3</sub> N <sub>4</sub>	High density film to resist oxidation during trench corner rounding oxidation step.	CVD
Shallow Trench Isolation trench fill.	SiO <sub>2</sub>	High density film with good gap filling properties.	HDP
Gate polysilicon anti-reflective coating.	Si <sub>3</sub> N <sub>4</sub>	Optical properties.	CVD
Sidewall spacers.	Si <sub>3</sub> N <sub>4</sub>	Etch rate difference relative to SiO <sub>2</sub>	CVD
Intermetal Dielectric layer 0 etch stop.	Si <sub>3</sub> N <sub>4</sub>	High density film with good barrier properties and etch rate difference relative to SiO <sub>2</sub> .	HDP
Intermetal Dielectric layer 0.	Doped SiO <sub>2</sub>	Thick film without cracking. Typically phosphorus doped or borophosphorous doped SiO <sub>2</sub> .	PECVD
Intermetal Dielectric layer 1+ with aluminum lines.	SiO <sub>2</sub>	Good gap fill.	HDP
Intermetal Dielectric film 1+ with	FSG or SiOC	Low-k films such as fluorine doped oxide or car-	HDP or
damascene copper.		bon doped oxide. Can be deposited with HDP or PECVD. PECVD is preferred due to lower com- plexity although many FSG films were deposited in HDP system already installed in fabs from pre- vious generation products.	PECVD.
Intermetal Dielectric film 1+ etch stop layer.	Si <sub>3</sub> N <sub>4</sub> or SiC	Etch rate difference relative to FSG or SiOC. Low- est k value possible also desired.	PECVD
Passivation	Si <sub>3</sub> N <sub>4</sub>	Good barrier properties	PECVD



Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

## **Common CVD deposition reactants**

Film	Reactants	System	Composition	Step coverage	Temperature (°C)
Al	TIBA, DIBAH, DMAH	LPCVD		Conformal	<250
Cu	Cu(hfac) <sub>2</sub> + H <sub>2</sub> or Cu <sup>1</sup> (hfac)L	LPCVD		Conformal	350-450
Si	SiH4	APCVD	Crystalline		950-1,050
	SiCl <sub>2</sub> H <sub>2</sub>	APCVD	Crystalline		1,050-1,150
	SiHCl <sub>3</sub>	APCVD	Crystalline		1,100-1,200
	SiCl <sub>4</sub>	APCVD	Crystalline		1,150-1,250
	SiH4	LPCVD	Crystalline		550-700
	SiH4	LPCVD	Polycrystalline	Conformal	580-650
Si <sub>3</sub> N <sub>4</sub>		PHCVD			50-250
	$SiH_4 + NH_3$	PECVD	Si <sub>x</sub> N <sub>y</sub> H <sub>z</sub>	Non Conformal?-	250-350
	SiH <sub>4</sub> + NH <sub>3</sub> + N <sub>2</sub> O	PECVD	Si <sub>x</sub> O <sub>y</sub> N <sub>z</sub>	Non Conformal?	250-350
	SiCl <sub>2</sub> H <sub>2</sub> + NH <sub>3</sub>	LPCVD	Si <sub>3</sub> N <sub>4</sub> (H)	Conformal	700-800
SiO <sub>2</sub>	SiH <sub>4</sub> +N <sub>2</sub> O	PHCVD	SiO <sub>2</sub>		50-200
	$SiH_4 + O_2$ or $SiH_4 + N_2O$	PECVD	SiO <sub>1.9</sub> (H)	Non Conformal	250
	TEOS + O <sub>2</sub>	PECVD	SiO <sub>x</sub>	Conformal	400
	TEOS + O <sub>2</sub>	APCVD	SiO <sub>2</sub> (-OH)	Isotropic flow	400
	SiH <sub>4</sub> + O <sub>2</sub>	LPCVD	SiO <sub>2</sub> (H)	Non conformal	450
	TEOS + O <sub>2</sub>	LPCVD	SiO <sub>2</sub> (-OH)	Conformal	700
	SiCl <sub>2</sub> H <sub>2</sub> + N <sub>2</sub> O	LPCVD	SiO <sub>2</sub> (CI)	Conformal	900
	O <sub>2</sub> or H <sub>2</sub> O	Thermal	SiO <sub>2</sub>	Conformal	700-1,200
TiN	TiCl <sub>2</sub> + NH <sub>3</sub> or TiCl <sub>3</sub> + H <sub>2</sub> /N <sub>2</sub> or	LPCVD		Conformal	400-700, or
	TDMAT + NH <sub>3</sub>				>700
W	$WF_6 + SiH_4$ or $WF_6 + H_2$	LPCVD		Conformal	400-500

#### **CVD** Hazards

 Many gases used in CVD systems are toxic (hazardous to humans), corrosive (causes corrosion to stainless steel and other metals), flammable (burns when exposed to an ignition source and an oxygen source), explosive and/or pyrophoric (spontaneously burn or explode in air, moisture or when exposed to oxygen)

Gas	Formula	Hazard	Flammable limits in air (%vol)	Exposure limit (ppm)
Ammonia	NH <sub>3</sub>	toxic, corrosive	16–25	25
Argon	Ar	inert		
Arsine	$AsH_3$	toxic		0.05
Diborane	B2H6	toxic, flammable	1–98	0.1
Dichlorosilane	$\mathrm{SiH}_{2}\mathrm{Cl}_{2}$	flammable, toxic	4–99	5
Hydrogen	$H_2$	flammable	4–74	
Hydrogen chloride	HCI	corrosive, toxic		5
Nitrogen	$N_2$	inert		
Nitrogen oxide	$N_2O$	oxidizer		
Oxygen	<b>O</b> <sub>2</sub>	oxidizer		
Phoshpine	$PH_3$	toxic, flammable	pyrophoric	0.3
Silane	$SiH_4$	flammable, toxic	pyrophoric	0.5

# Reference

- R. C. Jaeger, "Introduction to Microelectronic Fabrication," 2<sup>nd</sup> edition
- http://www.dowcorning.co.jp
- M. Madou, "Fundamentals of Microfabrication," 2<sup>nd</sup> edition
- C. Liu, "Foundations of MEMS," 1<sup>st</sup> edition
- J.M. Bustillo, R. T. Howe, and R. S. Muller, "Surface micromachining for microelectromechanical systems ," Proceedings of the IEEE, Vol. 86, No. 8, pp. 1552-1574, 1998
- Marc J. Madou, "Fundamentals of MICROFABICATION," 2nd edition
- S. Lee, C. Cho, J. Kim, S. Park, S. Yi, J. Kim, and D. Cho, "The Effects of Post-deposition Processes on Polysilicon Young's Modulus," IOP J. of Micromechanics and Microengineering, Vol. 8, No. 4, pp. 330-337, 1998
- S. Lee, C. Cho, J. Kim, S. Park, S. Yi, J. Kim, and D. Cho, "Mechanical Properties of Phosphorus-doped Polysilicon Films", Journal of the Korean Physical Society, Vol. 33, pp. 392-395, 1998
- S. Lee, and D. Cho. "The Effects of Texture on the Young's Modulus of Polysilicon", 1998 MRS Spring Meeting, 1998.



Dong-il "Dan" Cho Nano/Micro Systems & Controls Lab. This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

## Reference

- K. Lee, and Y Kim, "Uniformity Improvement of Micromirror Array for Reliable Working Performance as an Optical Modulator in the Maskless Photolithography System," Journal of Semiconductor Technology and Science, Vol. 1, No. 2, 2001
- G. Li, and A. A. Tseng, "Low stress packaging of a micromachined accelerometer," Electronics Packaging Manufacturing, IEEE Transactions on, Vol. 24, No. 1, pp. 18-25, 2001
- P. Melvas, E. Kalvesten, and G. Stemme, "A surface-micromachined resonant-beam pressure-sensing structure," Microelectromechanical Systems, Journal of , Vol. 10, No. 4, pp. 498-502, 2001
- K. Meng-Hsiung, O. Solgaard, R. S. Muller, and K. Lau, "Siliconmicromachined micromirrors with integrated high-precision actuators for external-cavity semiconductor lasers," Photonics Technology Letters, IEEE, Vol. 8, No. 1, pp. 95-97, 1996
- P. J. French and P. M. Sarro, "Surface versus bulk micromachining:the contest for suitable applications", IOP J. of Micromechanics and Microengineering, Vol. 8, pp. 45-53, 1998
- Gregory T. A. Kovacs, "Micromachined Trensducers Sourcebook," 1st edition
- J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition



Dong-il "Dan" Cho

Nano/Micro Systems & Controls Lab.

This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws

# Reference

- http://chiuserv.ac.nctu.edu.tw/~htchiu/cvd/home.html
- http://www.plasmas.org
- Brian Chapman, "Glow Discharge Processes: Sputtering and Plasma Etching", John Wiley & Sons, 1980.
- Lieberman, "Principles of plasma discharges and materials processing" John Wiley & Sons, 1994



Dong-il "Dan" Cho Nano/Micro Systems & Controls Lab. This material is intended for students in 4541.844 class in the Spring of 2009. Any other usage and possession is in violation of copyright laws