Embedded System Application

4190.303C

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History of Microprocessors for Embedded Systems

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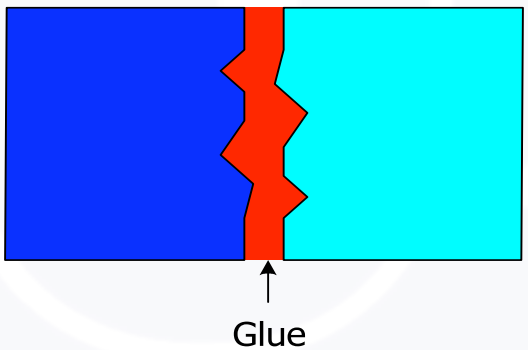
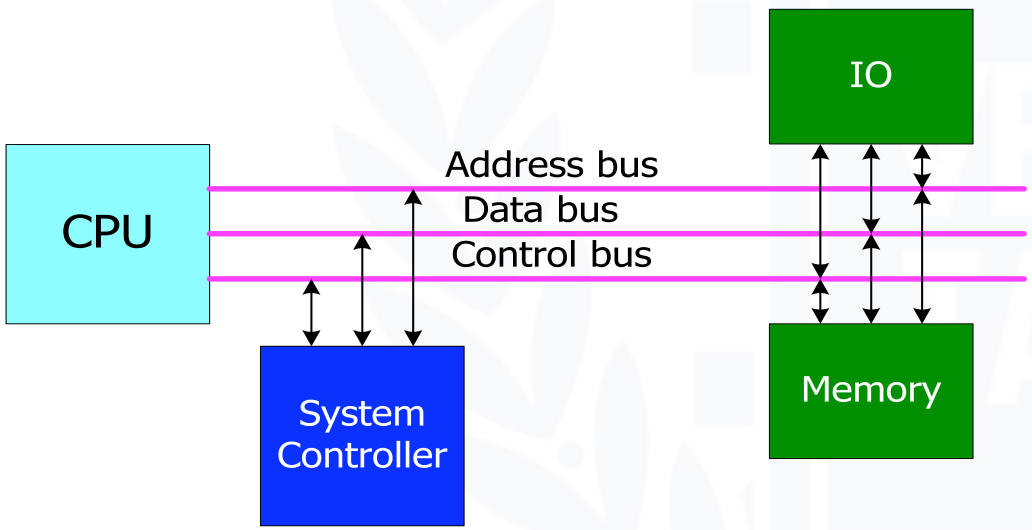
Computer System Architecture

- Conceptual configuration
  - Central processing unit
  - Memory
  - Inputs and outputs
  - System controller
    - Wrapper or glue





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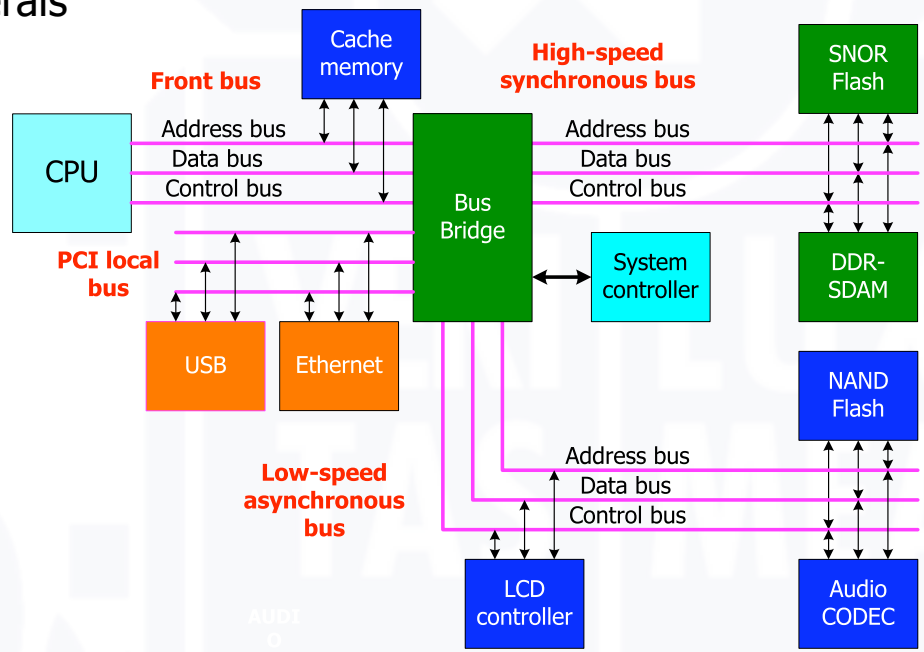
Computer Architecture

- Practical configuration
  - Multiprocessors or coprocessors
  - Memory hierarchy
  - Bus hierarchy
  - Types of memory devices: RAM, ROM, etc.
  - High-speed and low-speed peripherals



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2010년 3월 5일 금요일

Embedded System Architecture

- Embedded (computer) systems are computers
  - Have all the necessary components
    - CPU, memory, IO, etc.
- Embedded systems have specific dedicated applications
  - May have imbalanced architecture
    - Small RAM and big ROM
    - Slow CPU but fast memory
    - 8 bit CPU but with a 32 bit graphics accelerator
  - May have special peripherals
    - A/D converters
    - Special sensors
    - Special communication adapters
    - Special hardware support
- Embedded systems are optimized
  - May not have peripherals for development
    - No keyboard, no mouse, no display, etc.
    - Not enough memory for compliers, etc.

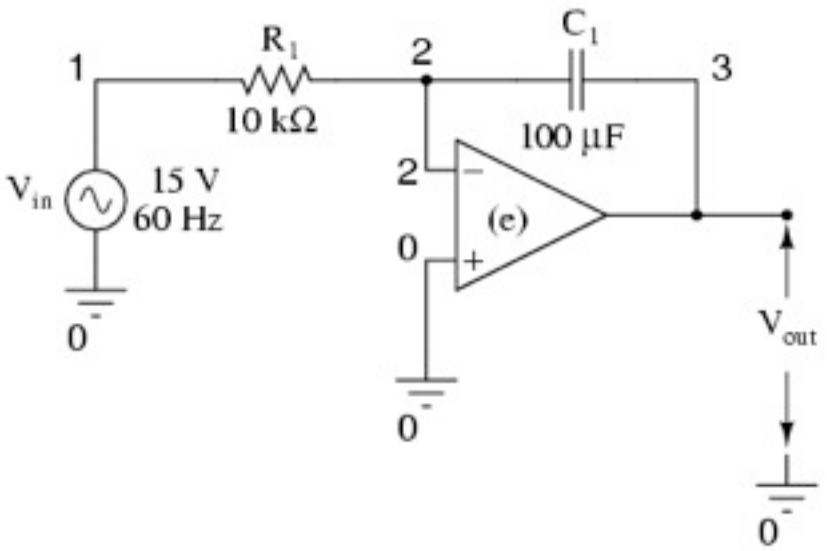
Rule of Thumb

- Better embedded system architecture design
  - Need to understand computer system architecture
  - Need to understand system software
  - Need to understand application
    - Domain knowledge
  - Need to understand hardware to application
    - Vertical optimization
  - Need to understand technology

Analog Computers

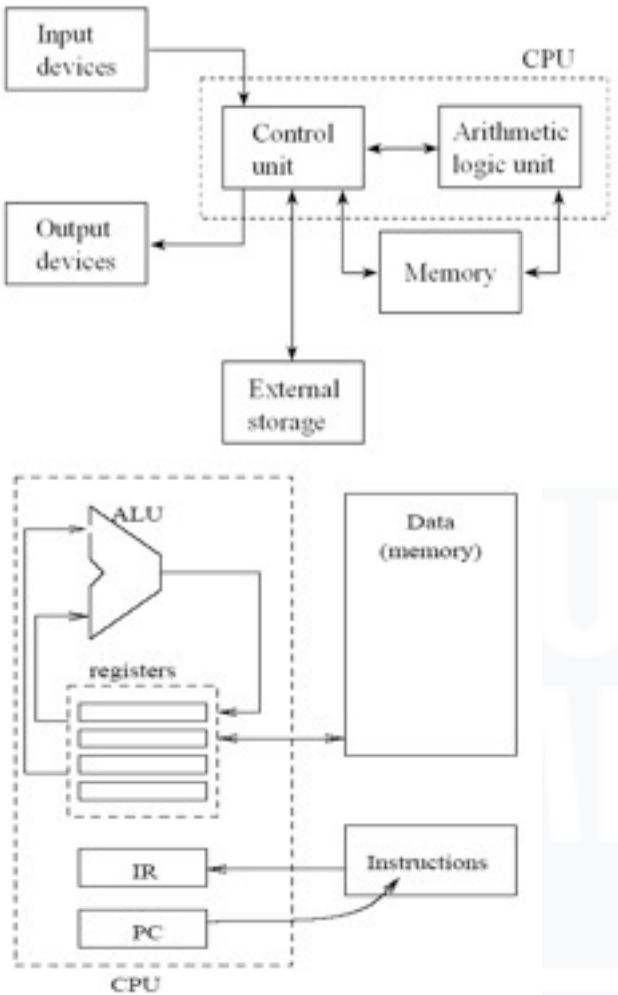
- Integration

$$V_{out} = \int_0^t 15\sin(2\pi \times 60t)dt$$



Stored Program Control by Von Neumann

- Register
  - A memory location in the CPU
- PC
  - Program counter that holds the memory address of the next instruction
- IR
  - Instruction register that holds the current instruction
- Acc
  - Accumulator that holds the result of an operation performed by the ALU
- Register File
  - A collection of several registers



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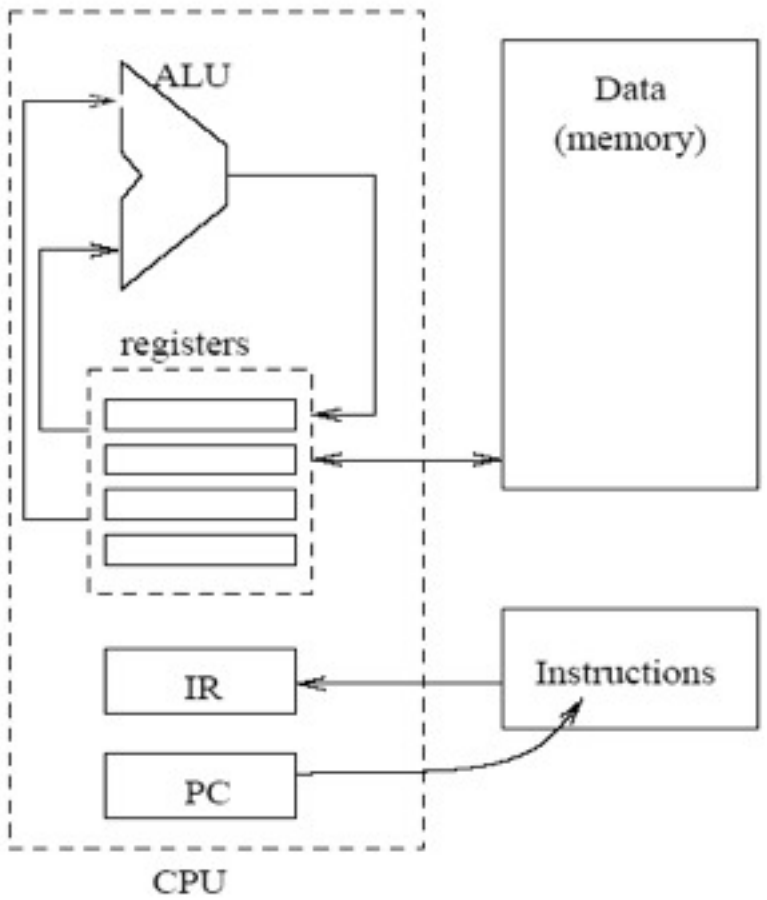
2010년 3월 5일 금요일

Hardwired Logic versus Microprocessor

- Hardwired logic
  - Parallel architecture for the next state forming and the output forming logic
  - Fast but complicated
  - Not good scalability
- Microprocessor
  - Sequential execution for the next state forming and the output forming logic
  - Slow but simple structure
  - Good scalability with an expense of speed

Stored Program Control by Von Neumann

```
pc= 0;
do {
    instruction = memory[pc++];
    decode( instruction );
    fetch( operands );
    execute;
    store( results );
} while( instruction != halt );
```



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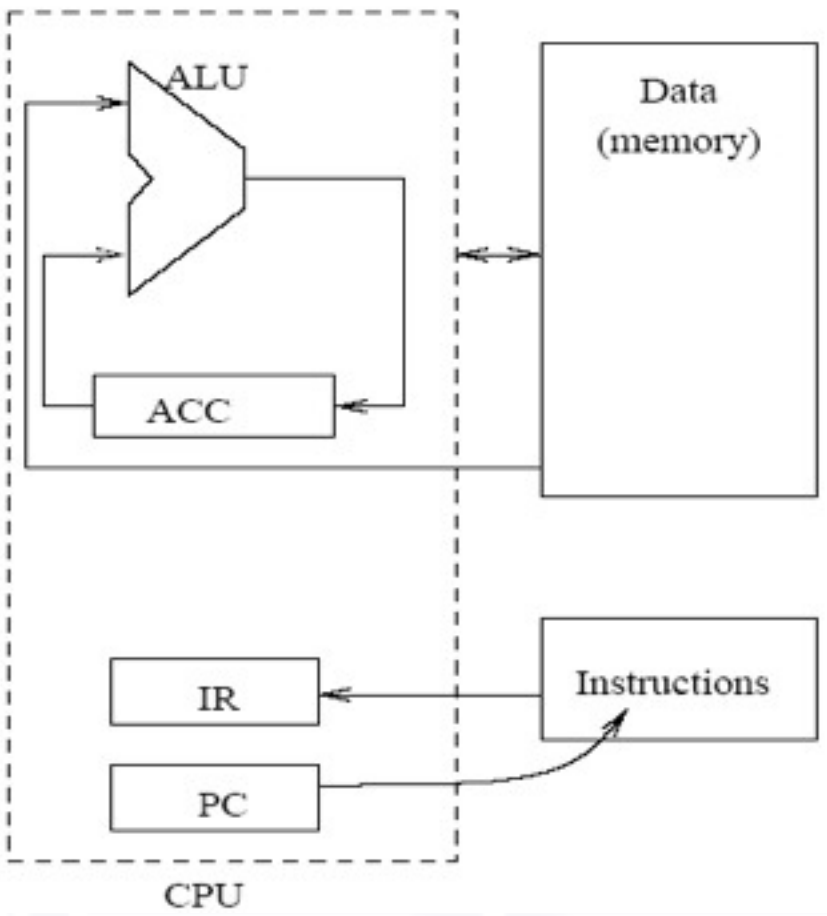
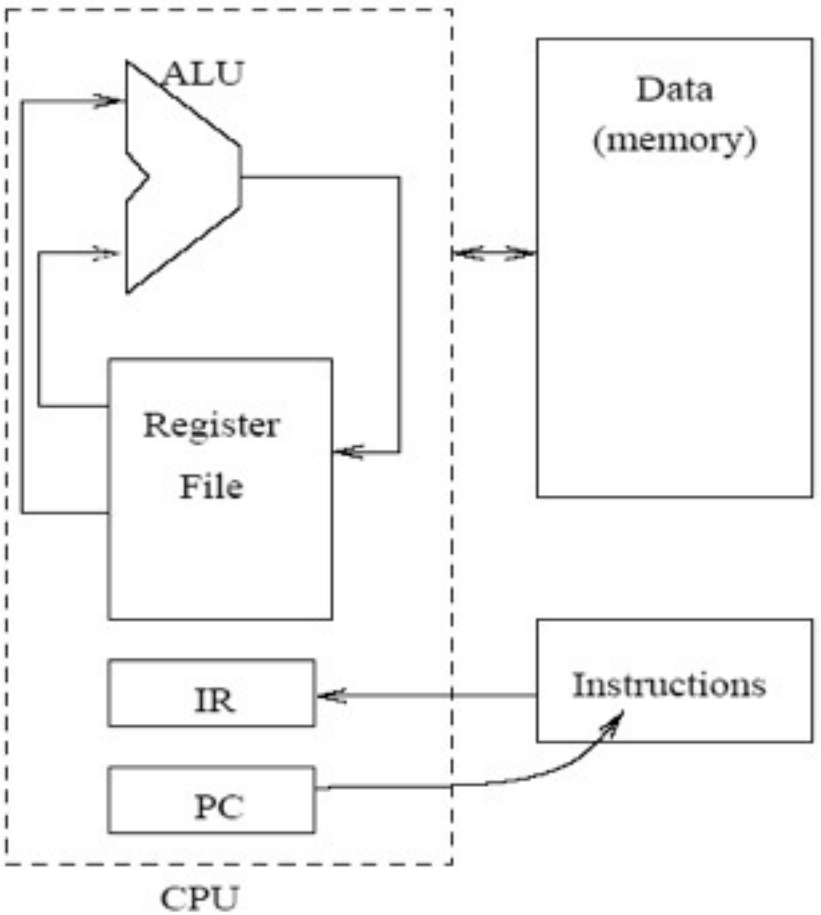
Accumulator Architecture

- Has a special register, called an accumulator
- Combined with another operand as input to the ALU, with the result of the operation replacing the contents of the accumulator
- Operation
  - Place one of the numbers into the accumulator (load operand)
  - Execute the add instruction
  - Store the contents of the accumulator back into memory (store operand)



Load/store (Register) Architecture

- Registers
  - Faster access but are expensive
  - For frequently accessed data
- Memory
  - Slower but less expensive
- Principle of "locality"
  - At a given time, a program typically accesses a small number of variables much more frequently than others
- Loads and stores the registers from memory
- Arithmetic and logic instructions operate with registers, not main memory, for the location of operands



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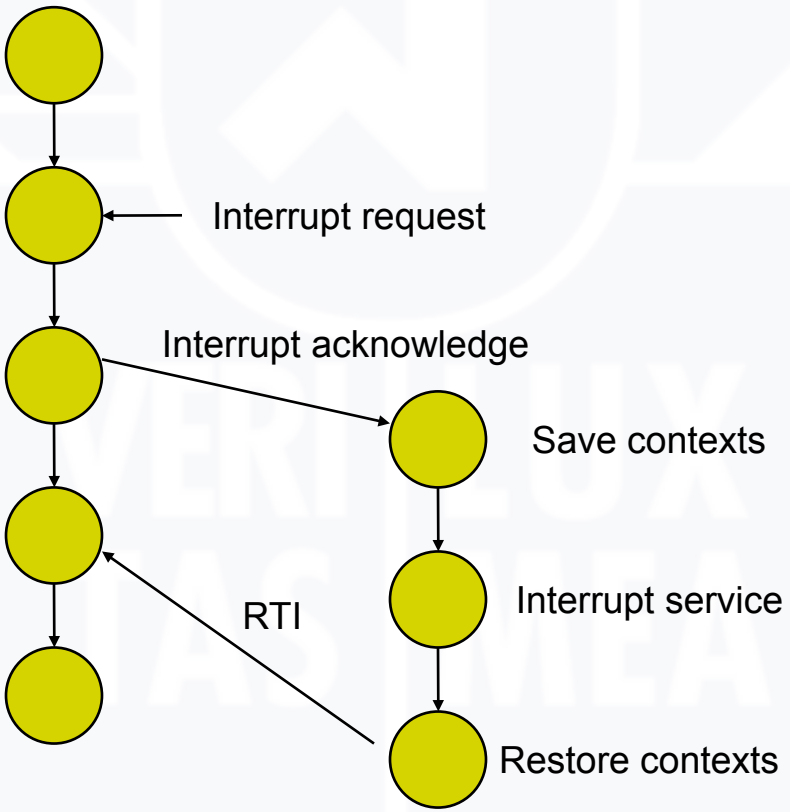
Before Microprocessors (Prehistory)

- Central processing unit is composed of discrete components
  - Vacuum tubes
  - Transistors
  - Computer systems are too expensive to be embedded in a system
- Central processing unit is composed of MSI (medium scale integrated circuits)
  - Westinghouse 2500 computer
  - One to four 19” lacks compose of a CPU
  - Magnetic core main memory
  - Power plant control
  - Equipped with most user interface components
  - Imbalanced architecture
    - 16-bit CPU architecture with intelligent IO controller
      - Thousands of sensors and actuators
    - Many monitors
    - Special hardware support for SOE (sequence of event)
  - Special software feature
    - Real-time operating system

Exception and Interrupt Processing

- Program is for sequential execution
- Types of exception and interrupts
  - Reset
  - Hardware interrupt
  - Software interrupt
  - Exception
    - Overflow
    - Divide by zero

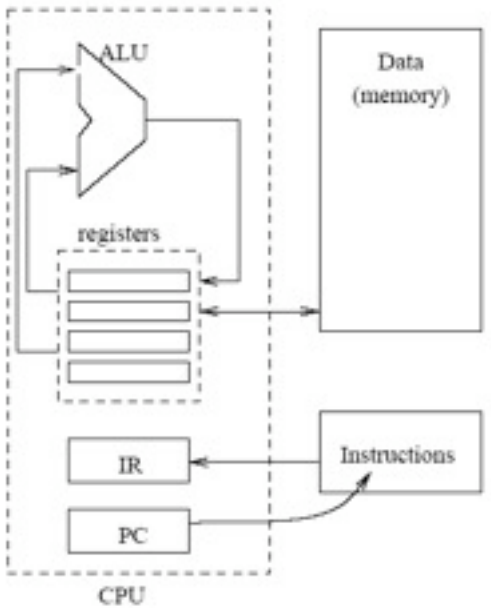


Exception and Interrupt Processing

- Essential for handling of errors and asynchronous events
  - Polling and interrupt
- Context
  - Microprocessor has long-term memory problem
  - Problematic long-term memory: relies on external storage
  - Remember only short-term memory contents
- Precision interrupt for embedded systems

4 bit Microprocessors

- All the microprocessors are for embedded systems
  - CPU core only
  - No peripherals, no memory
- Intel 4004 was a 4-bit CPU designed for usage in calculators
  - Clocked at 740 KHz
  - 4 KB of program memory and 640 bytes of RAM
  - Perfect fit for calculators but not very suitable for microcomputer use due to limited architecture
    - No interrupt support
    - 3-level deep stack
    - Complicated method of accessing the RAM



4 bit Microprocessors

- Intel D4040: a practical successor of i4004

Features	4004	4040
Program memory	4 KB	8 KB (two 4 KB banks)
Stack memory	3 levels	7 levels
Registers	16 index registers	24 index registers (two banks - 16 and 8 registers)
Instructions		16 additional instructions (see below) AND and OR logical instructions Interrupt-related instructions ROM and index bank selection instructions Two new load accumulator instructions
Interrupts	None	Program can be interrupted by external signal
Pins/signals		STP - switch processor to STOP mode STP ACK - processor is in STOP mode INT - interrupt input INT ACK - interrupt acknowledge CM-ROM$_1$ - ROM bank selection output
Other features		Single step operation
Package	16-pin DIP	24-pin DIP

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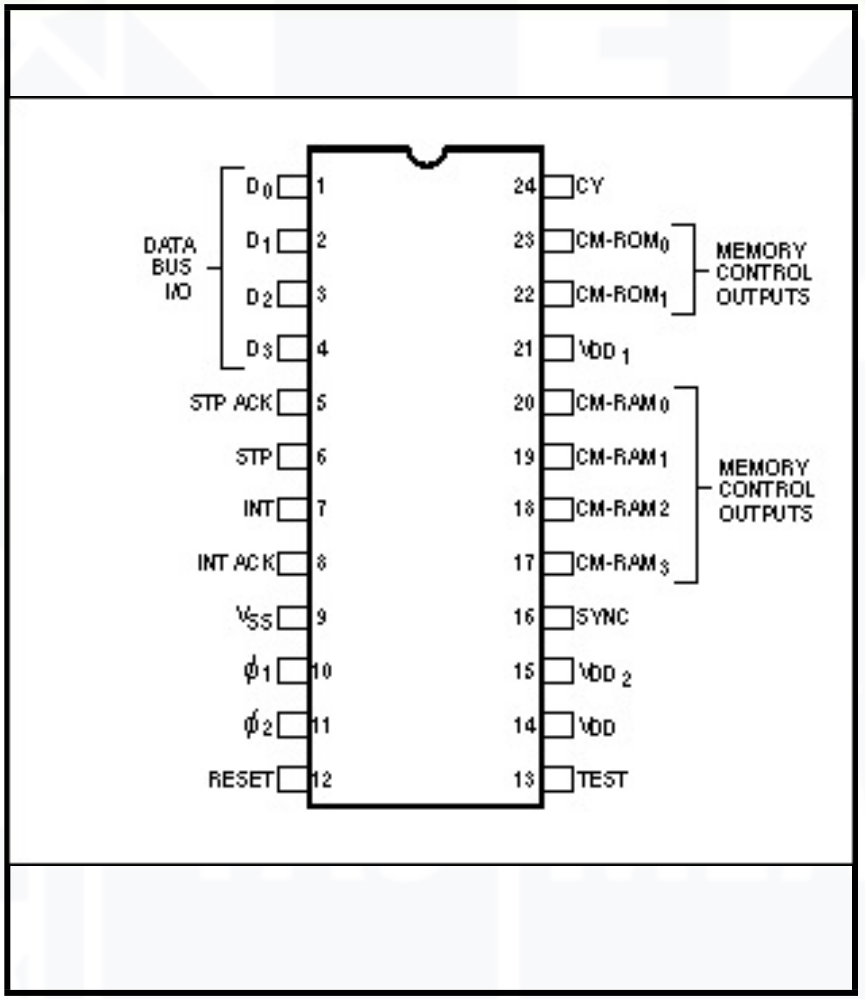
4 bit Microprocessors

- MCS-40 family

4008/4009	standard memory and I/O interface set
4040	4-bit Central Processor Unit with 60 instructions
4101	256 x 4 RAM
4201	clock generator
4265	programmable general purpose I/O device
4269	programmable keyboard display device
4289	standard memory interface
4308	1024-bit mask programmable ROM and four 4-bit I/O Ports
4316/2316	2048-bit ROM
4702/1702	2048-bit Erasable and Electrically Reprogrammable MOS ROM (Static)

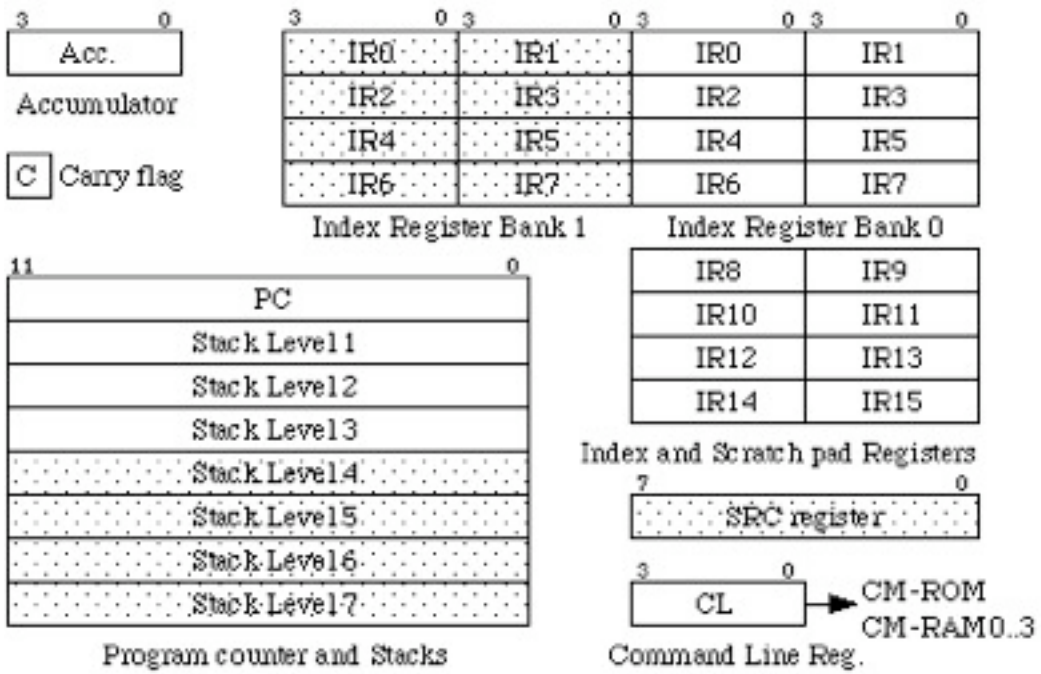
4 bit Microprocessors

- Intel 4040 microarchitecture
  - 8 KB program memory
    - Two 4 KB banks
    - Jump to any address within currently selected bank
  - 640 B data memory
    - RAM access is same to I/O port access
    - A SRC instruction specify address
    - WRM or RDM writes or reads accumulator data to memory
    - Data memory is separate from program memory



4 bit Microprocessors

- Stack is 7-level deep
  - Separate from program memory and data memory
- Interrupts
  - One maskable interrupt can be enabled or disabled by DIN and EIN instructions



4 bit Microprocessors

- Intel 4040 microarchitecture
  - 4-bit accumulator
    - Arithmetic and logic operations, reading and writing data from/to RAM and I/O ports
  - 24 4-bit Index registers
    - 16 registers in bank 0 and 8 registers in bank 1
    - Lower 8 registers can be selected from bank 0 or 1 using SB0 and SB1 instructions
    - Memory access is not convenient due to short bit width
  - 60 instructions
    - Data moving instructions
    - Arithmetic - add, subtract, increment and decrement
    - Logic - rotate, AND and OR
    - Control transfer - conditional (limited to current ROM), unconditional, call subroutine and return from subroutine
    - Input/Output instructions
    - Interrupt-related instructions - halt, enable, disable, and return from subroutine
    - Other - carry flag operations, decimal adjust, bank selection for ROM and index registers, etc.
    - Instruction length can be one or two bytes

8 bit Microprocessors

- 8 bit microprocessors
  - Beginning of microprocessor-based system era
  - No distinguish between general purpose processors and embedded processors
  - CPU core only and dedicated peripherals
    - Serial communication ports, parallel IO ports, timers and interrupts controllers
  - Assembly programming and later C programming
  - No memory and bus hierarchies
  - Representative processors
    - Intel 8080 series
    - Motorola 6800 series
    - Zilog Z80
    - MOS Technology 6502

8 bit Microprocessors

- Architecture
  - Accumulator, Register and memory
    - Arithmetic and logical operation
      - ADD Acc, ($1000)
      - ADD D0, D1
      - ADD ($1000), ($1001)
  - Addressing mode
    - CPU was not faster than memory
    - Both accumulator and register architectures were feasible
      - LD D0, ($1000
ADD D1, D0
      - ADD A, ($1000)

8 bit Microprocessors

- CISC type
  - Complex instructions are added
    - Non-pipelined
    - Block transfer, etc.
- 1 to 8MHz operation
- Usually SRAM is used for embedded applications
  - CPU is capable of 64KB addressing
  - Commonly 1 to 16KB memory

8 bit Microprocessors

- Motorola 6800 series
  - Accumulator architecture
    - Accumulator A (ACCA) and Accumulator B (ACCB)
    - 8-bit register used for arithmetic and logic operations
    - Memory devices are faster than CPUs
  - Index (IX) register
    - 6-bit register for temporary storage or as an index when indexed addressing is used
      - ss
  - 16-bit Program counter (PC) for 64KB addressing
  - 16-bit Stack pointer (SP)
  - Condition code register
    - Half carry (H) - set if there was a carry from bit 3 to bit 4 of the result when the result was calculated
    - Interrupt mask (I) - set if the IRQ interrupt is disabled
    - Negative (N) - set if the most significant bit of the result is set
    - Zero (Z) - set if the result is zero
    - Overflow (V) - set if there was an overflow during last result calculation
    - Carry (C) - set if there was a carry from the bit 7 during last result calculation

8 bit Microprocessors

- Addressing mode
  - Implied
    - Data value/data address is implicitly associated with the instruction
    - Accumulator - the instruction implies that the data is one of the accumulator registers
    - Immediate
    - 8-bit or 16-bit data is provided in the instruction
  - Direct
    - One-byte operand provided in the instruction specifies the memory address in page zero (0000h - 00FFh) where data is located
  - Extended
    - Two-byte operand provided in the instruction specifies the memory address where data is located
  - Relative
    - One byte offset is added to the address of the next instruction (the contents of the program counter register + 2)
    - The offset is a signed number in the range -127 - +127
  - Indexed
    - One byte operand is added to the contents of the IX register
    - The resulting 16-bit value is a pointer to memory where data is located

8 bit Microprocessors

- Exception processing
  - IRQ
    - Maskable interrupt
    - Program counter, index register, accumulators and condition code registers are stored in the stack
    - Further interrupts are disabled
    - Processor jumps to memory location address of which is stored in memory FFF8h - FFF9h
    - Return from the interrupt the processing routine with RTI instruction
    - IRQ can be enabled/disabled using CLI/SEI instructions
  - NMI
    - Non-maskable interrupt that cannot be disabled
    - Program counter, index register, accumulators and condition code registers are stored in the stack
    - Further interrupts are disabled
    - Processor jumps to memory location address of which is stored in memory FFFCh – FFFDh
    - Return from the interrupt the processing routine with RTI instruction
  - SWI
    - Software interrupt
    - Invoked from the program
    - Program counter, index register, accumulators and condition code registers are stored in the stack
    - Disables the further interrupts
    - Jumps to memory location address of which is stored in memory FFFAh – FFFBh
    - Return from the interrupt the processing routine should use RTI instruction
    - This interrupt can not be disabled.

8 bit Microprocessors

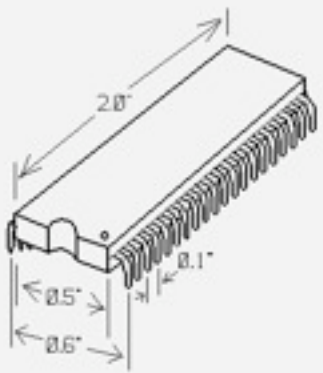
- MOS Technology 6502
  - Apple Computer
  - Competitor MOS Technology cloned and upgraded the 6800 with its 6502
    - 8-bit accumulator register (A)
    - Two 8-bit index registers (X and Y)
    - 8-bit status register (SR)
    - 8-bit stack pointer (SP)
    - 16-bit program counter (PC)
  - Zero page
    - Subroutine call/scratchpad stack's address space is hardwired to memory page $01 ($0100–$01FF)
    - Scratchpad memory
      - LDA $00 ; zero page
        LDA $0000 ; non-zero page

8 bit Microprocessors

- Intel 8080
  - Combination of accumulator and register architecture
    - Accumulator and six 8 bit registers
      - A, B, C, D, E, H, L
      - Pairs BC, DE and HL could be combined as 16 bit registers
      - Data moving instructions
    - 16 bit stack pointer
      - 8 level internal stack of the 8008
    - 6 bit program counter
    - Register addressing
      - Register - references the data in a register or in a register pair
      - Register indirect - instruction specifies register pair containing address, where the data is located
  - I/O mapped I/O
    - Separate 256 I/O port addressing with I/O commands
  - No zero page
    - processor always uses 16-bit addresses for data access
    - Zero page is reserved for vectors and RST instructions

8 bit Microprocessors

- Zilog Z80
  - Eight real improvements over the 8080:
    - An enhanced instruction set including new IX and IY index registers and instructions for them
    - Two separate register files, which could be quickly switched, to speed up response to interrupts
    - Block move, block I/O, and byte search instructions
    - Bit manipulation instructions
    - A built-in DRAM refresh address counter that would otherwise have to be provided by external circuitry
    - Single 5 Volt power supply
    - Fewer outboard support chips required for clock generation and interface to memory and I/O
    - A much lower price



16 bit Microprocessors

- Higher integration thanks to CMOS
- Embedded controllers
  - Peripherals are embedded
  - Dedicated peripherals disappeared
- No distinct memory hierarchy yet (10 to 16MHz operation)
- Bus hierarchy
  - ESA bus
  - S-bus
- C programming
- Protection
  - User mode and supervisory mode
- 24MB addressing
  - Dynamic memory is used

16 bit Microprocessors

- Motorola 68000 (68K)
  - Complete register architecture CISC
    - 8 general-purpose data registers (D0-D7)
    - 8 address registers (A0-A7)
    - A7 is the stack pointer
    - Arithmetic and logical operations are done by registers
    - Memory accesses are done by data move instructions between registers and memory
  - 16 bit data and 32 bit addressing
    - No page or segment registers
  - Orthogonal instruction set architecture
    - Instructions were divided into operations and address modes
    - Almost all address modes are available for almost all instructions

16 bit Microprocessors

- Motorola 68000 (68K)
  - Privilege levels
    - Two levels of privilege: user and supervisor modes
  - Interrupts
    - 8 levels, strictly prioritized
    - Fully programmable exception table at fixed location permitting 256 vectors
  - CPU is getting faster than memory
    - No more accumulator architecture and zero page
  - Big-endian processor
    - Higher order bytes first
  - No backward compatibility with 8 bit 6800 series
  - Continue to 68020, 68030 and 68040 before PowerPC

16 bit Microprocessors

- Intel 8086
  - Source code compatible with i8080
    - Segment register for 24 bit addressing
    - 16 bit general purpose registers
      - Often used by implicit addressing
        → complicated register allocation of temporary variables
    - Poor hardware architecture but better chance for software
  - Mathematical floating point coprocessor: i8087
  - 8 bit bus version: i8088
  - Major change occurred in i80286
  - Continue to 80386, 80486 and Pentium

32 bit and 64 bit Microprocessors

- Distinct different between general purpose microprocessor and embedded processor
  - Operation speed
  - Memory hierarchy
  - Embedded peripherals
  - Bus hierarchy
  - Operating systems
  - Networking
  - Development environment

32 bit and 64 bit Microprocessors

- Many powerful processors
  - Intel 80386 and 80486
  - Motorola PowerPC
  - ARM RISC series
  - Intel XScale
  - MIPS RISC series
- This course covers ARM9 architecture with Motorola Dragonball

Current Embedded Processors

- Embedded processors rather than embedded controllers
  - Containing more general purpose peripherals
- Market division
  - Powerful 32 bit RISC cores
    - MIPS, ARM, PowerPC, XScale, etc.
  - Low-cost small size RISC/CISC cores
    - i8051, PIC, etc.
  - Reconfigurable CPU cores
  - Soft-microprocessors
- Cache and high-speed main memory (266 DDR SDRAM)
- PCI or equivalent local bus expansion

Homework (due: One week later)

- Survey and summarize the following terms:
  - Accumulator architecture
  - Register architecture
  - Zero page
  - Addressing modes
  - Interrupt and NMI
  - Software interrupt
  - I/O mapped I/O vs. memory mapped I/O
  - Little and Big endians
  - Segment registers
  - Orthogonal instructions vs. implicit addressing
  - Register allocation