



## Chapter 19.

# MODERN FET STRUCTURES

Sung June Kim

[kimsj@snu.ac.kr](mailto:kimsj@snu.ac.kr)

<http://helios.snu.ac.kr>

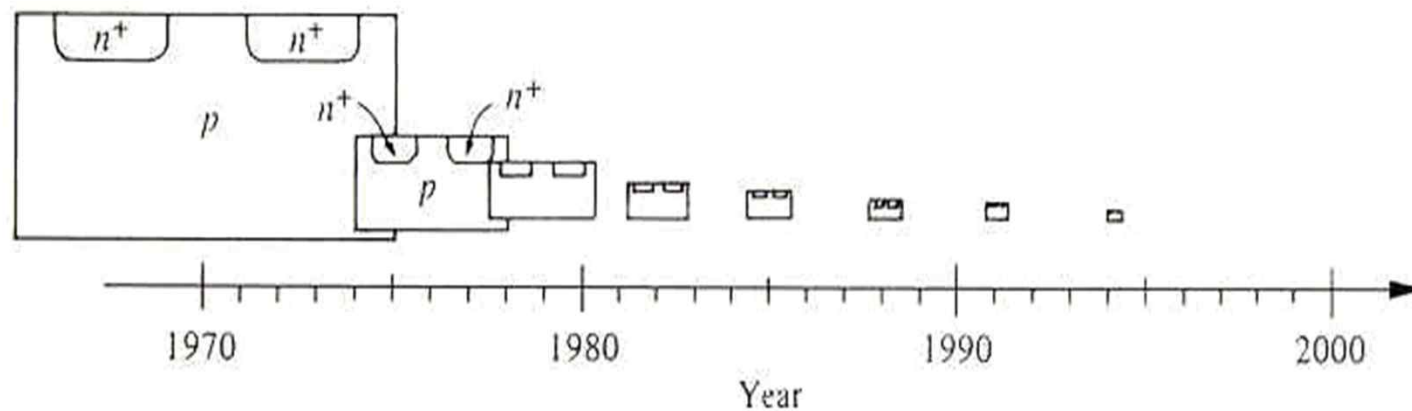


# CONTENTS

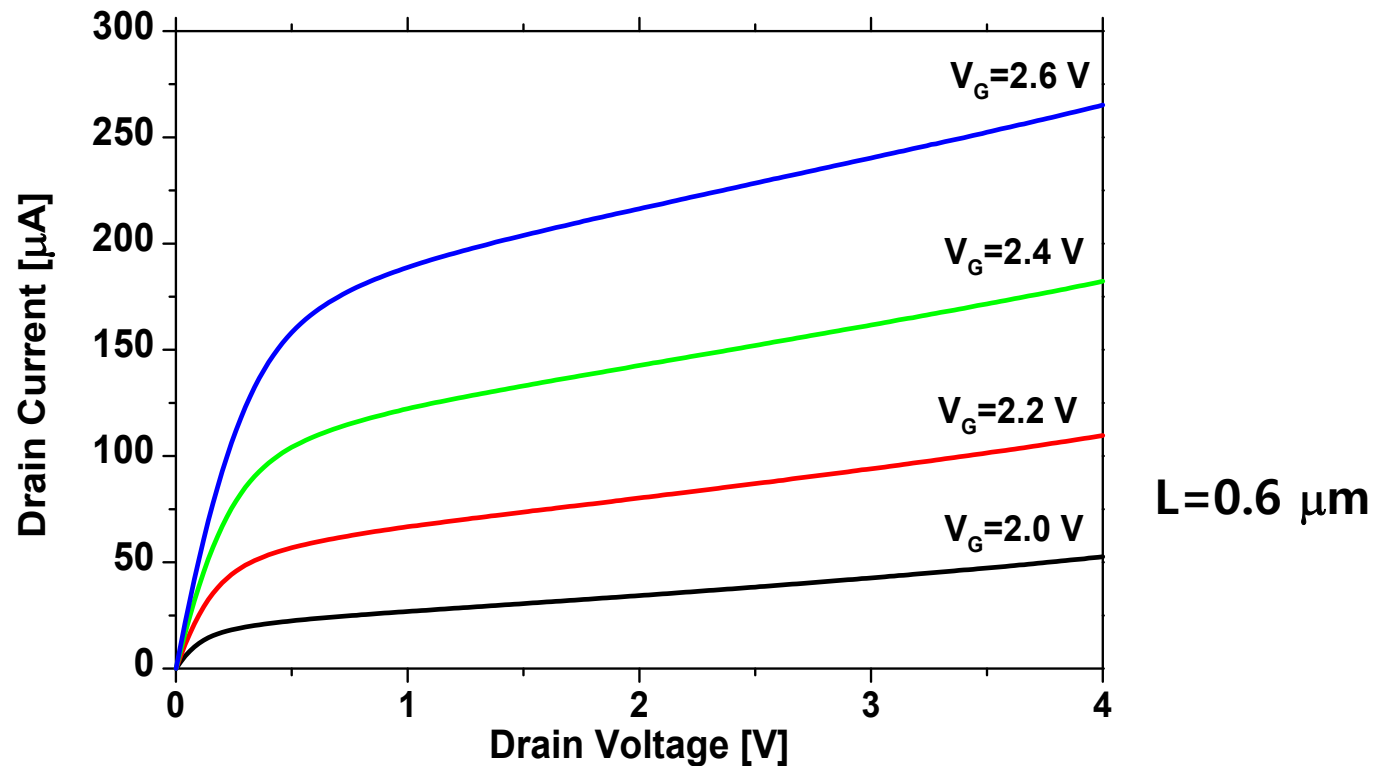
- **Small-Dimension Effects**
- **Select Structure Survey**

## Small-Dimension Effects

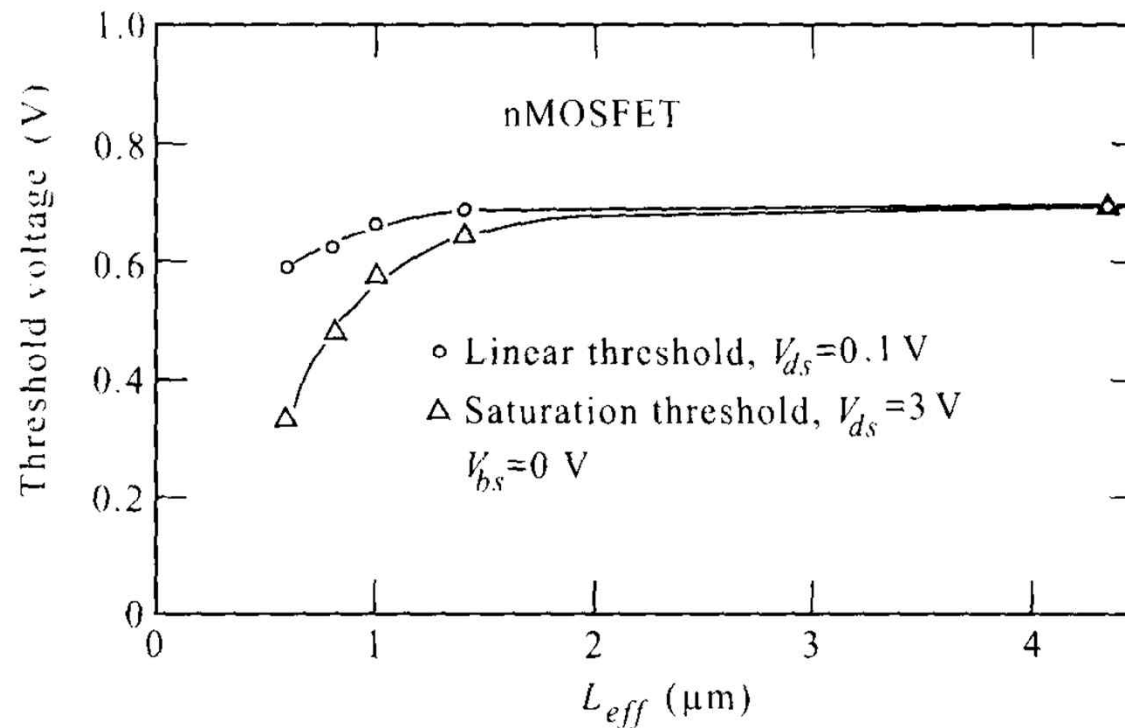
- **To achieve higher speeds and increased packing densities, FET device structures have become smaller and smaller.**



- **Departure from long-channel behavior**
  - Significant upward slant in the post pinch-off portions of the  $I_D - V_D$



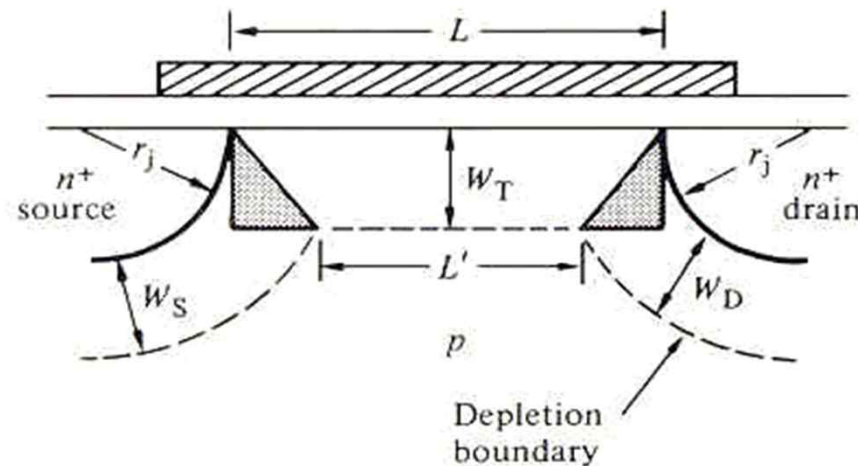
- In short-channel devices,  $V_T$  becomes a function of the gate dimension and the applied biases.



# Threshold Voltage Modification

## • Short-channel

- $|V_T|$  monotonically decreases with decreasing  $L$ .
- The source and drain assist in depleting the region under the gate.  $\boxtimes$  less gate charge for inversion  $\boxtimes V_T \downarrow$



– **First order quantitative expression**

$$\Delta V_T = V_T(\text{short channel}) - V_T(\text{long channel})$$

$$= -\frac{1}{C_o} (Q_{BS} - Q_{BL}), \quad Q_{BS} : Q_B \text{ for short-channel}$$

$$Q_{BL} : Q_B \text{ for long-channel}$$

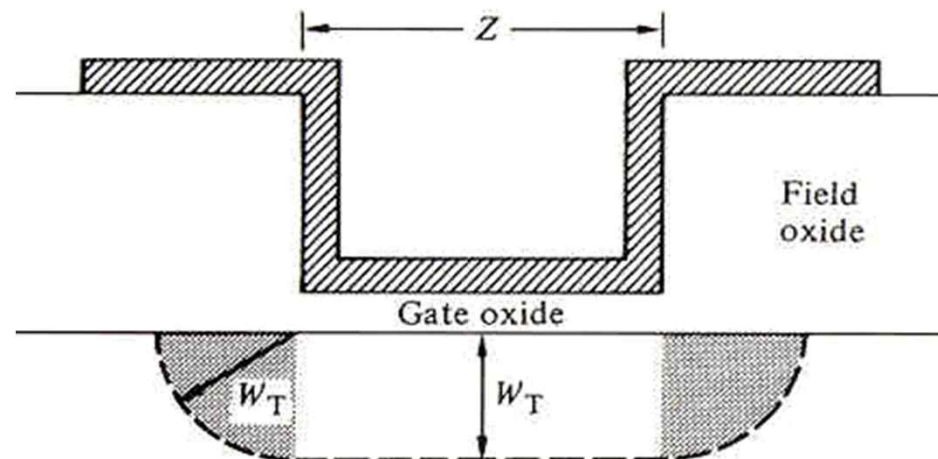
$$= -\frac{qN_A W_T r_j}{C_o L} \left( \sqrt{1 + \frac{2W_T}{r_j}} - 1 \right) \quad [\text{homework}]$$

- Examining  $\Delta V_T / V_T(\text{long channel})$ , short-channel effects are decreased by reducing  $x_o$ , reducing  $r_j$ , and increasing  $N_A$ .

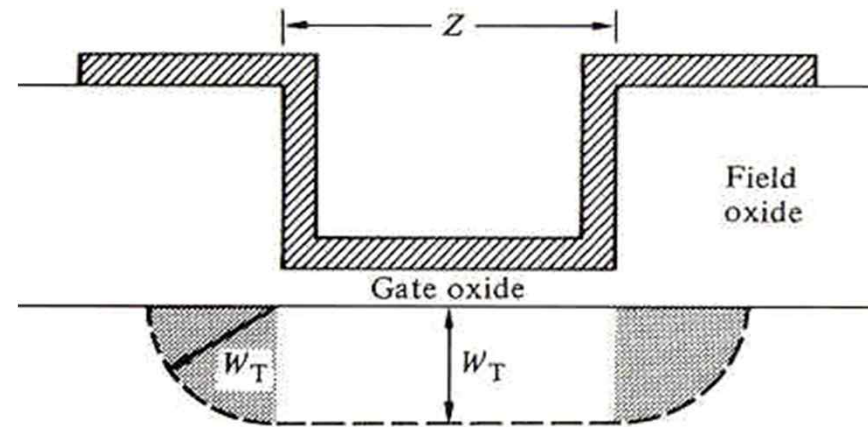


- **Narrow channel (skip)**

- $|V_T|$  monotonically increases with decreasing  $Z$ . ( Opposite to the  $L$ -dependence)
- The gate-controlled depletion region extends to the side, lying in part outside the  $Z$ -width of the gate; that is, the effective charge /cm<sup>2</sup> being balanced by the gate charge  $\uparrow \boxtimes V_T \downarrow$







- If the lateral regions are assumed to be quarter-cylinders of radius  $W_T$

$$Q_B(\text{*narrow width*}) = -\frac{qN_A \left( ZLW_T + \frac{\pi}{2} W_T^2 L \right)}{ZL}$$

$$= -qN_A W_T \left( 1 + \frac{\pi W_T}{2Z} \right)$$

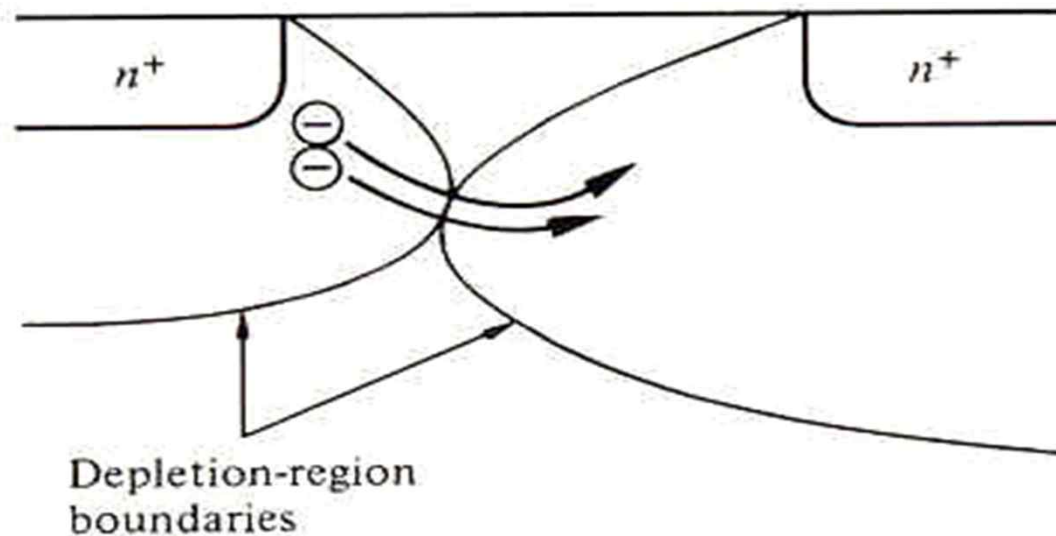
$$\therefore \Delta V_T(\text{*narrow width*}) = \frac{qN_A W_T \pi W_T}{C_o 2Z}$$



## Parasitic BJT Action

- **MOSFET bears a physical resemblance to a lateral BJT**
- **Punch-through**
  - The depletion regions around the source and drain to touch.
  - The gate loses control of the subgate region and the  $I_D$  flows beneath the surface through the touching depletion regions.

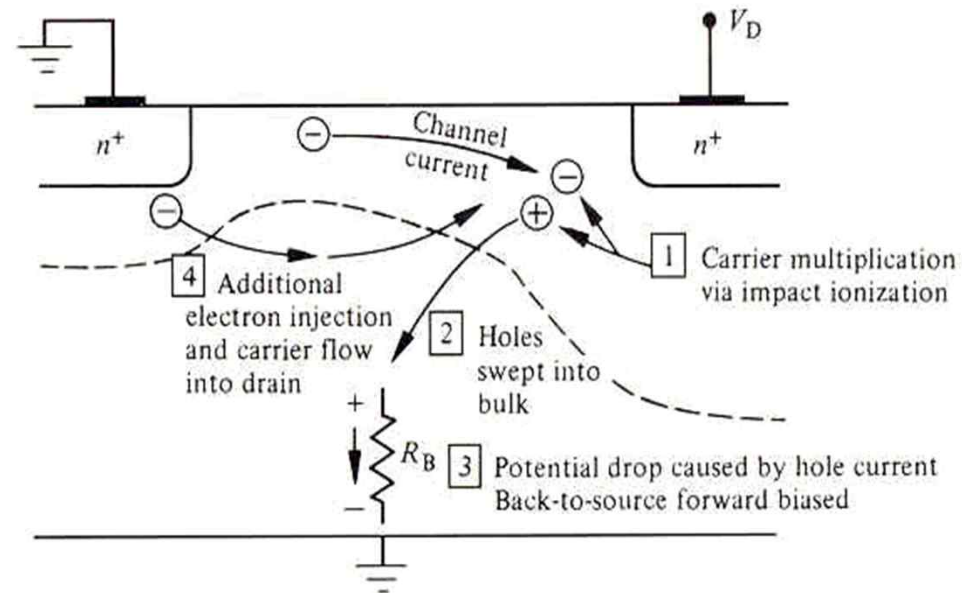




- Punch-through can be suppressed by increasing  $N_A$  and decreasing the depletion widths.
- ❌ increasing parasitic capacitances.
- ❌ perform a deep-ion implantation to selectively increase the doping of the subgate region.



- **Carrier multiplication and regenerative feedback**
  - In short-channel devices, the carrier multiplication coupled with regenerative feedback can dramatically increase  $I_D$  and places a reduced limit on the maximum  $V_D$ .



- The added electrons drift into the drain. The source PN junction is forward biased.



## Hot-Carrier Effects

- **Oxide charging ( charge injection and trapping in the oxide )**
  - In the vicinity of the drain, some of carriers gain a sufficient amount of energy to surmount the Si-SiO<sub>2</sub> barrier.→ A charge build-up within the oxide
  - A larger percentage of the gated region is affected in the smaller devices.
  - Significant changes in  $V_T$  and  $g_m$ .
  - Oxide charging limits the useful “life” of a device.
  - To minimize hot-carrier effects, the LDD ( Lightly Doped Drain ) structure is used.



- **Velocity saturation**

- The carrier drift velocities inside Si at  $T=300K$  approach a maximum value of  $v_{dsat} \cong 10^7 \text{ cm/sec}$  when the electric fields are large.
- $I_{Dsat}$  is significantly reduced. Approximately,

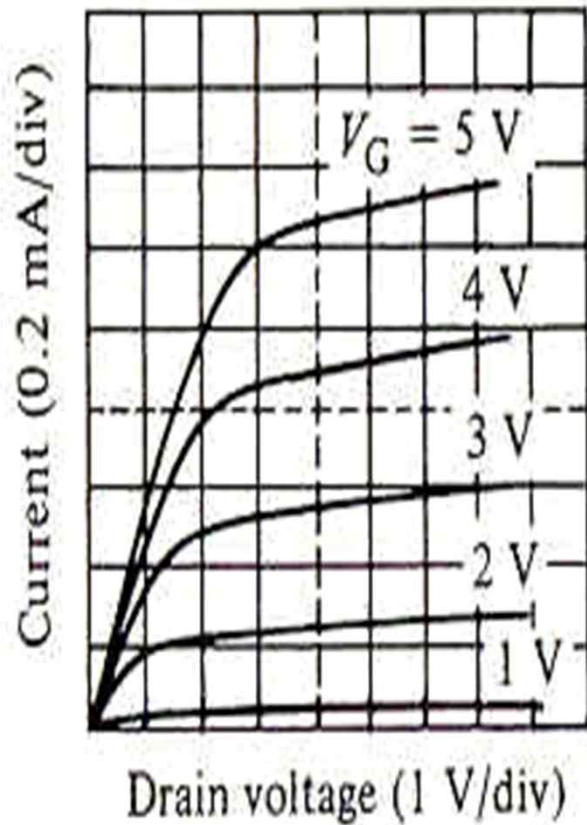
$$I_{Dsat} \cong ZC_o(V_G - V_T)v_{dsat}$$

$$I_{Dsat} \propto (V_G - V_T); \text{ short - channel}$$

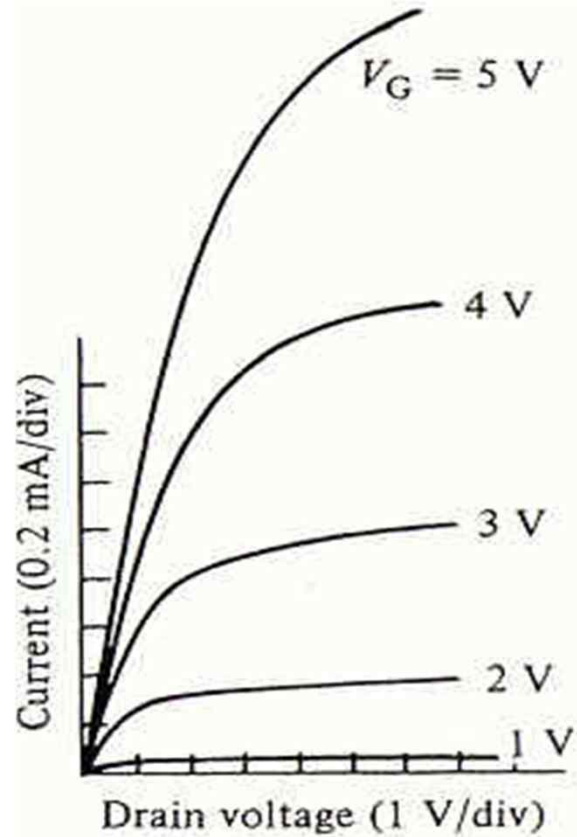
$$I_{Dsat} \propto (V_G - V_T)^2 ; \text{ long - channel}$$



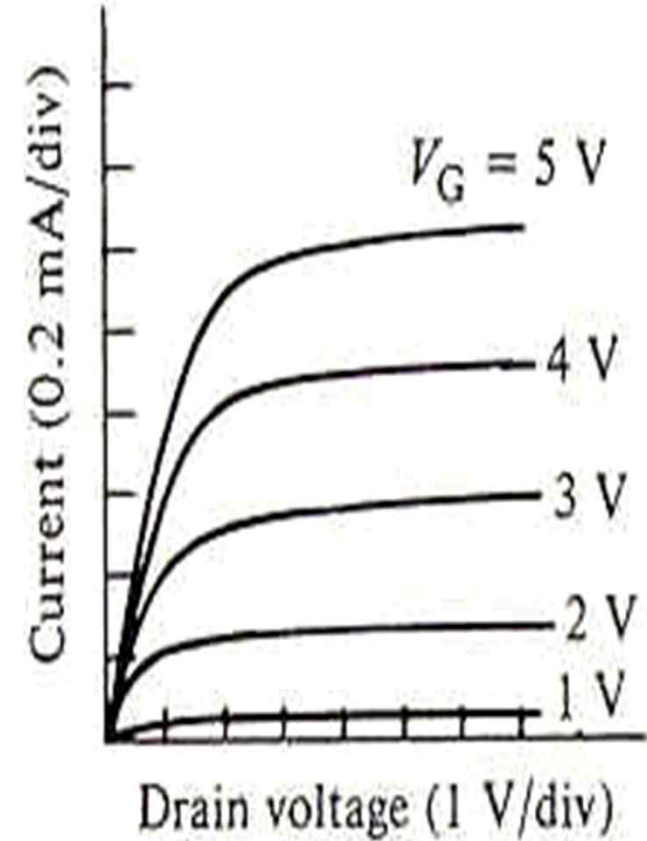
(a) Experimental characteristics



(b) Theoretical characteristics including velocity saturation



(c) Theoretical characteristics ignoring velocity saturation



- **Ballistic Transport**

- If very small dimension structures have  $L < l$  ( the average distance between scattering events ), a large percentage of the carriers travel from the source to the drain without experiencing a single scattering event.
- It can lead to super-fast devices.

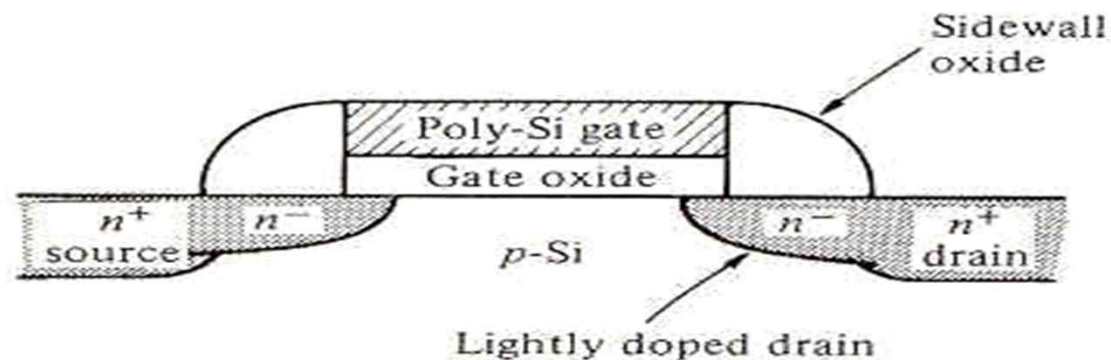
$\therefore$  the average velocity of carriers  $> v_{dsat}$





## Select Structure Survey

- **LDD (Lightly Doped Drain) Transistors**
  - The reduced dimension devices are more susceptible to hot-carrier effects.
  - Lightly doped drain region ( $n^-$  region) between the end of the channel and the drain
  - Electric field ← The voltage drop in the  $n^-$  region lowers the maximum  
→ Carrier injection into the oxide  
→ Oxide charging



Ch 19  
~~19~~ Modern FOT

scales down.

P692 Table 19.1.

Short channel effect

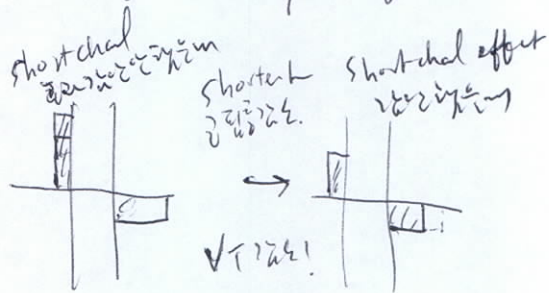
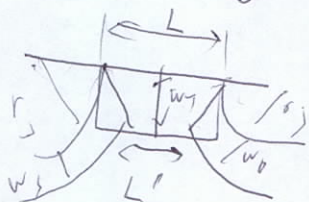
$$I_D \propto \frac{W}{L}$$

$V_T$  function of  $L$  ~~is~~

$L \downarrow \rightarrow (V_T) \downarrow$  (causes S-D amount in depletion gate region)

so less charge is required for inversion

Quantitatively,



$$\Delta V_T = V_T(\text{short-ch}) - V_T(\text{long-ch})$$

with regular region at threshold

$$= -\frac{1}{C_0} (Q_{BS1} - Q_{BS2}) = -\frac{q N_A W_T}{C_0} \frac{r_j}{L} \left( \sqrt{1 + \frac{2W_T}{r_j}} - 1 \right)$$

depletion region charge for short channel  
 depletion region charge for long channel

$$\frac{\Delta V_T}{V_T} = -\frac{r_j}{L} \left( \sqrt{1 + \frac{2W_T}{r_j}} - 1 \right)$$

To reduce,  $r_j$ ,  $\frac{W_T}{r_j}$  needs to be reduced

min. channel below which short-ch. effects occur.

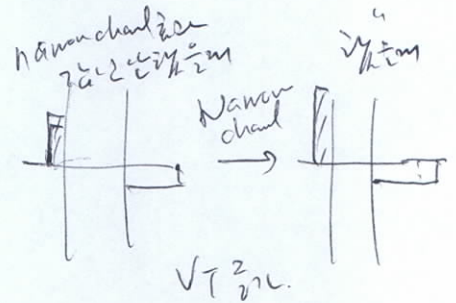
Also by empirical relation  $L_{min} = 0.4 [r_j x_0 (W_T + W_D)]^{1/3}$

smaller  $x_0$  is required (oxide thickness)

smaller  $r_j$  layer NA smaller  $x_0$

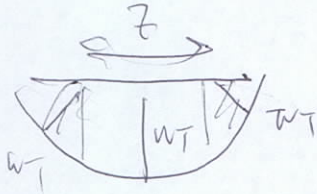
# Narrow channel

$|V_T| \uparrow$  as  $z \downarrow$



depletion ~~is~~  $V_G$  is wasted (?)

in regions ~~out~~ of gate.  
side

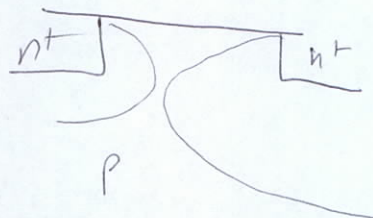
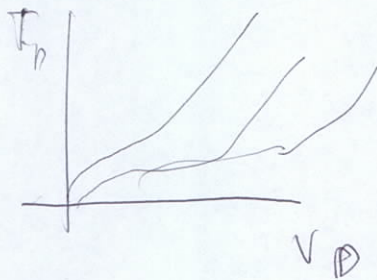


$z \downarrow$  More charge required to achieve balance  $|V_T| \uparrow$ .

$$\Delta V_T = \frac{q N_A w_T}{C_0} \cdot \frac{\pi w_T}{2z}$$

If  $z \sim w_T$ , ~~is~~ problematic

## punch-through (punch through ~~is~~ $z \sim w_T$ )



as  $V_D \uparrow$   
 $S, D$  depletion regions meet!  $\rightarrow$  punch-through current (gate loses control)  
 like in BJT  
 $I_D \propto V_D^2$

Solution:  $N_A \uparrow \rightarrow$  ~~is~~  $w_s, w_d \downarrow$

also increase  $C_T$

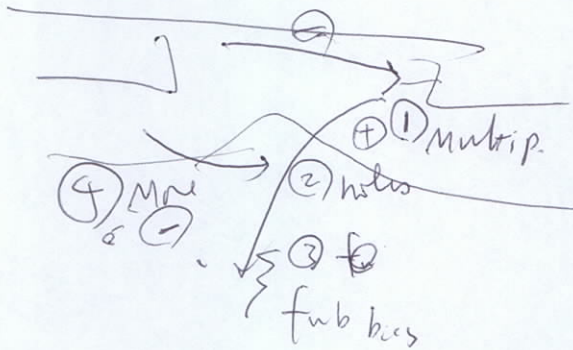
channel ~~is~~ ~~gate~~ ~~control~~ ~~is~~ ~~lost~~ ~~due~~ ~~to~~ ~~depletion~~ ~~regions~~ ~~meeting~~ ~~in~~ ~~the~~ ~~channel~~  
 (only under gate)



Cannon Multiplex & Regenerative Effect (positive feedback)

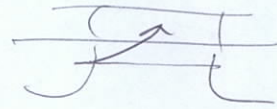
See picture in Fig 19.7

$V_D \rightarrow$   $e^-$  accelerated

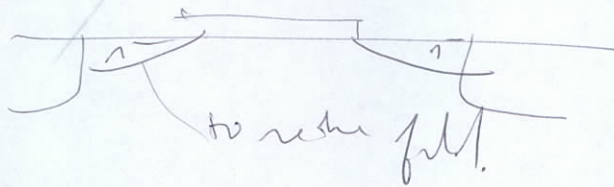


$V_D \rightarrow$  Hot carrier effect  
energy  $\uparrow$   $e^-$   
oxide charge  $\rightarrow$  changes  $V_T$  & gain

Also reliability.



Solution LDD for short ch. devices



Vel. saturation (soft delivery)

$$V_{set, sat} \sim \sqrt{W/L} \text{ or } \mu E$$

Then  $I_D$  is linked to

$$I_{D, sat} = Z C_{ox} (V_G - V_T) V_{d, sat}$$

$$\approx I_D \propto (V_G - V_T)^2$$

not  $(V_G - V_T)^2 \approx I_D$  - ideal

This saturation can be avoided if  $L \ll \lambda$  (avg dist between scattering events)  
 $\rightarrow$  Super fast, Ballistic Transport