Lecture 3. Understanding Transistors: Technology Characterization

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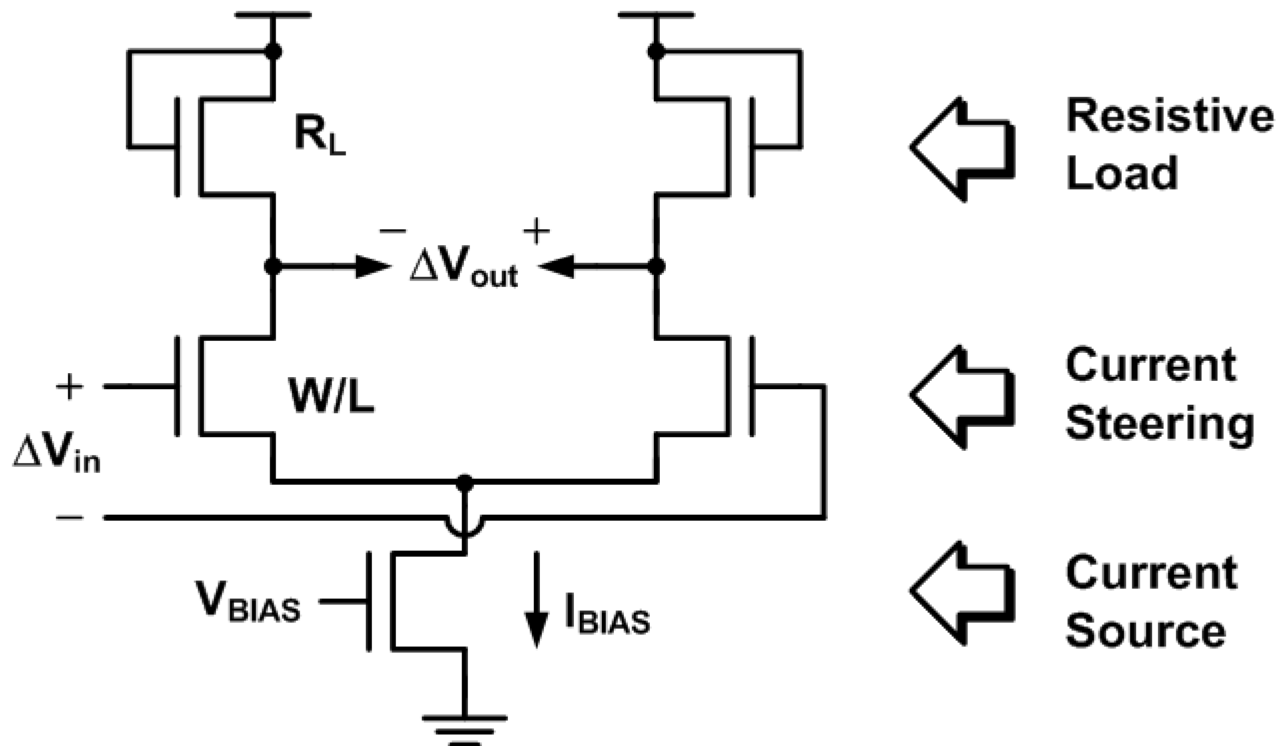
Motivations

- Good circuit design starts with understanding transistors that you build circuits with
- In a sense, you are asking the following questions:
  - What can I use these transistors for (intent; usage)?
  - For each intent, what are the metrics that describe its quality?

- Acknowledgements:
  - Prof. Boris Murmann at Stanford
  - Ref: Willy M.C. Sansen, "Analog Design Essentials", Ch. 1.

Every Device Has a Purpose

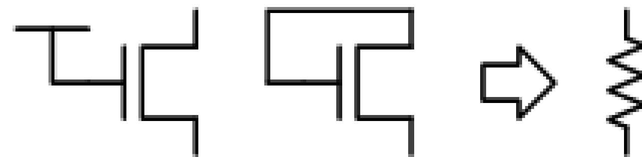
- When building a circuit, the designer utilize a different property for each device (it is the “design intent”)
  - What are the possible ways to use transistors?



Ways to Utilize MOS Transistors

- Current source

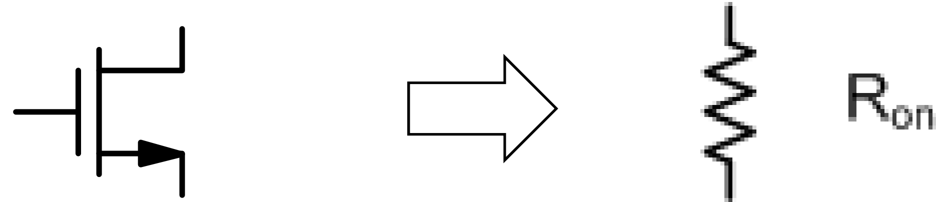
- Resistor



- VCCS

- Switch

MOS as a Resistor



- MOS transistor operating in linear region acts as a resistor
- Linear region: $V_{GS} > V_{th}$ and $V_{DS} < V_{DS,sat}$
- According to the long-channel model:

$$I_D = \mu C_{ox} \frac{W}{L} (V_{GS} - V_{th} - \frac{1}{2} V_{DS}) \cdot V_{DS}$$

- And if $V_{DS} << V_{GS} - V_{th}$ ($= V_{DS,sat}$)

$$R_{on} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})}$$

R_{on} vs. Technology

$$R_{on} \approx \frac{1}{\mu C_{ox} \frac{W}{L} (V_{GS} - V_{th})}$$

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \qquad t_{ox} \approx \frac{L_{min}}{50}$$

- For constant gate overdrive ($V_{ov} = V_{GS}\text{-}V_{th}$), the on-resistance per square decreases with technology
- But, the maximum available $V_{GS}\text{-}V_{th}$ has been scaling down (e.g. $V_{DD} \propto L_{min}$ from 0.35um down to 90nm)
  - As a result, the minimum Ron stayed roughly constant
  - Then what about below 65nm?

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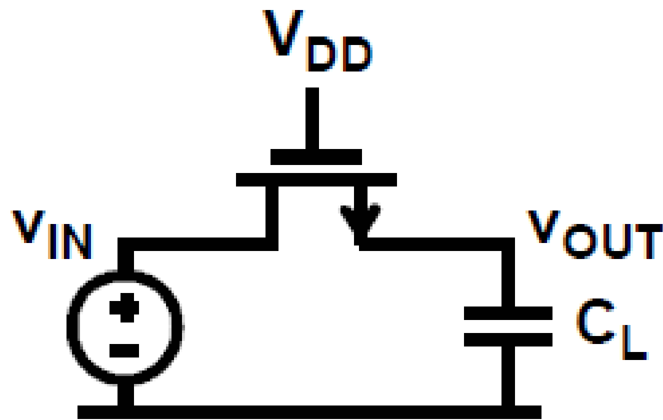
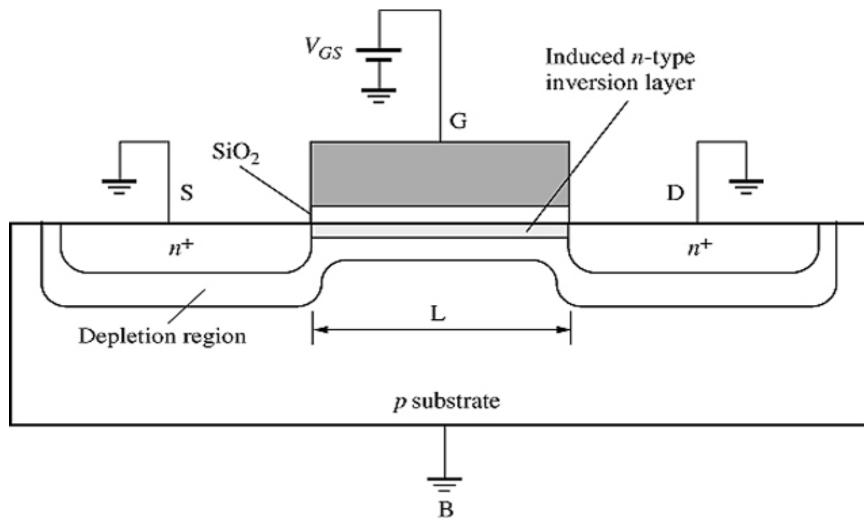
Exercise: Analog Switch on C_L



We want to switch 0.6 V to a load capacitance C_L of 4 pF.
We want to do this fast, with time constant 0.5 ns.
Supply voltage V_{DD} = 2.5 V
V_T = 0.5 V
Use standard 0.35 μm CMOS.

- Required Ron < 0.5ns / 4pF = 125-ohms
- Ron varies V_{GS}-Vth (≅ avg. of 2.0V and 1.4V)
- Calculate the minimum W/L required
- Actual Ron is found higher than predicted – can you guess why?

Body Effect



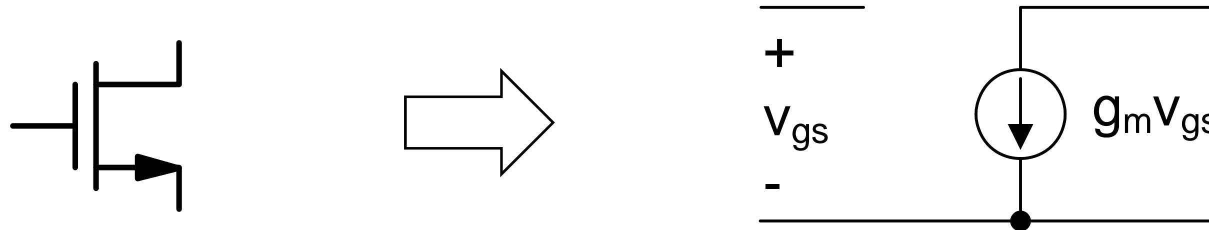
- As bulk voltage (V_{BS}) drops, the increased reverse-bias increases the depletion charge to be inverted

→ Vth increases!

$$V_{th} = V_{th,0} + \gamma \left[\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|} \right]$$

- The parameter γ is technology dependent
  - Check out how body effect is scaling with technology

MOS as a VCCS

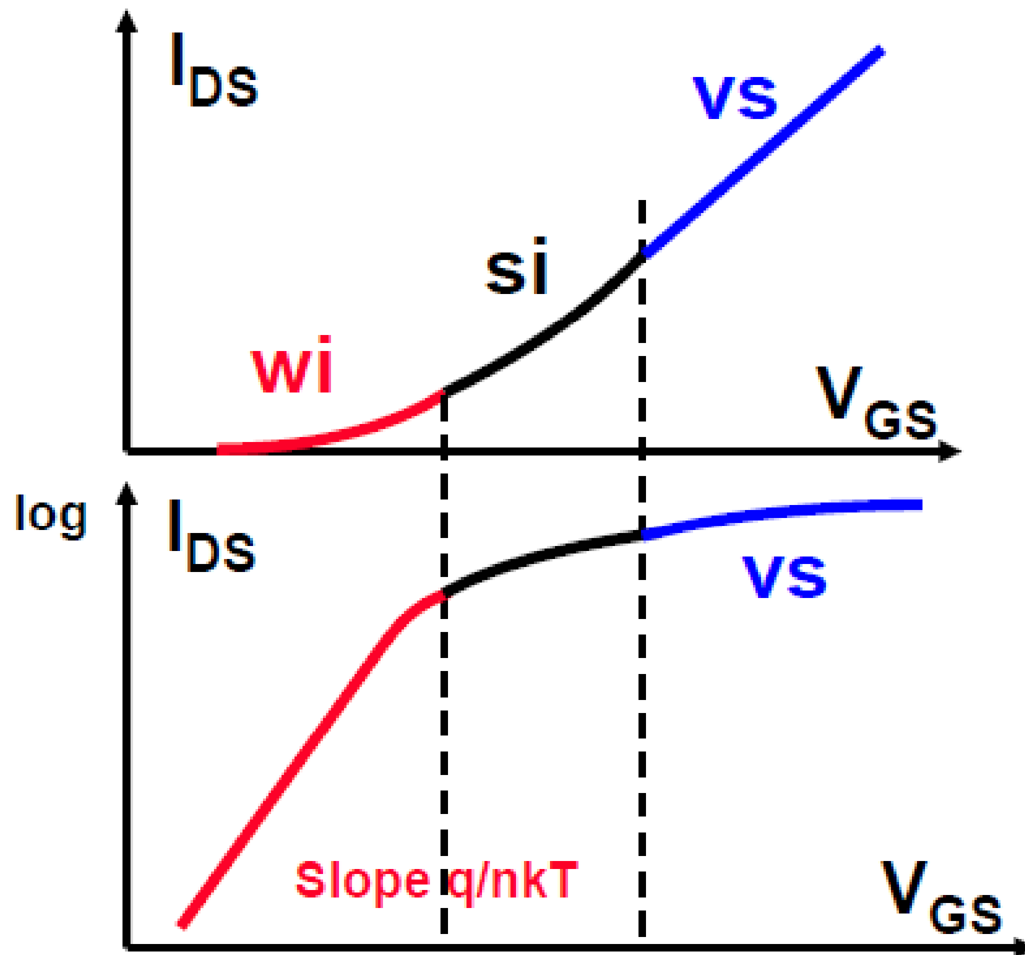


- MOS transistor operating in saturation region can be approximated as a VCCS
- Long-channel model (square-law model) states:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2$$

$$g_m = \sqrt{2I_D\mu C_{ox}\frac{W}{L}} = \frac{2I_D}{V_{GS} - V_{th}} = \frac{2I_D}{V_{OV}}$$

Closer Look at G_m: I_{DS} vs. V_{GS}



- Weak inversion:

$$I_{DS} \propto exp^{\frac{V_{GS}}{nkT/q}}$$

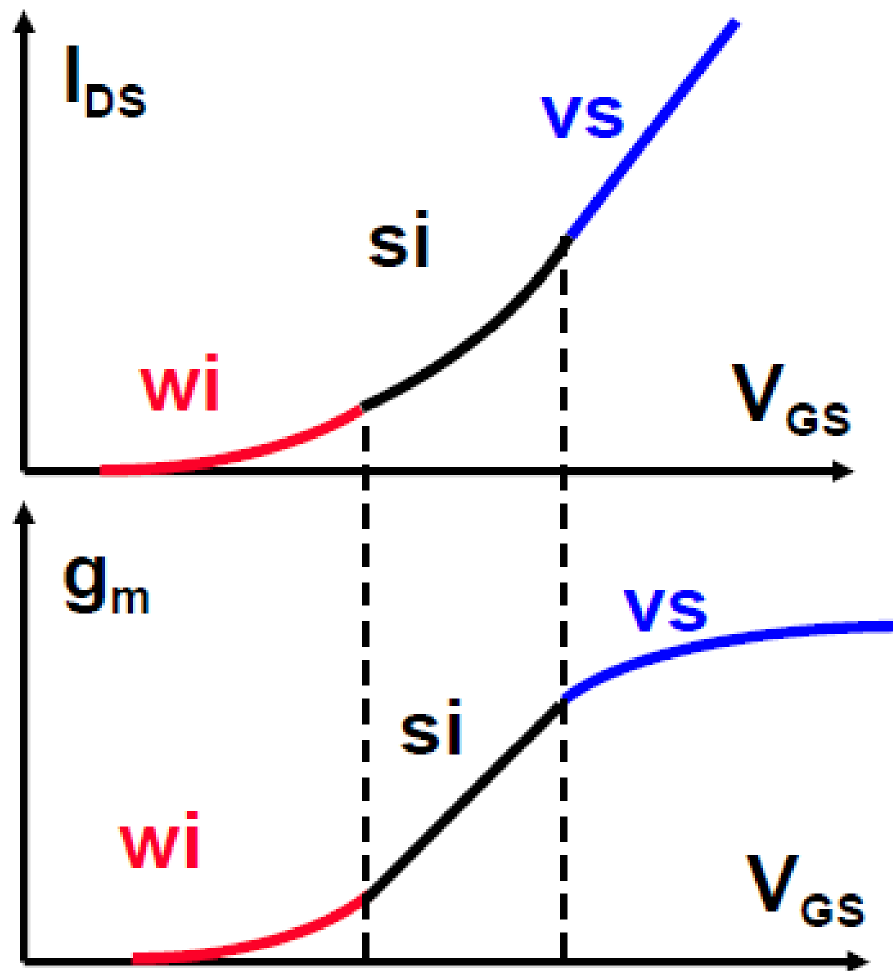
- Strong inversion:

$$I_{DS} \propto (V_{GS} - V_{th})^2$$

- Velocity saturation:

$$I_{DS} \propto (V_{GS} - V_{th})$$

Closer Look at G_m: G_m vs. V_{GS}



- Weak inversion:

$$g_m = \frac{I_{DS}}{nkT/q}$$

- Strong inversion:

$$g_m \propto V_{GS} - V_{th}$$

- Velocity saturation:

$$g_m \propto const$$

Transition Between Weak & Strong Inversion

- By equating the g_m-expressions for weak and strong inversion regions, we can find where the transition occurs

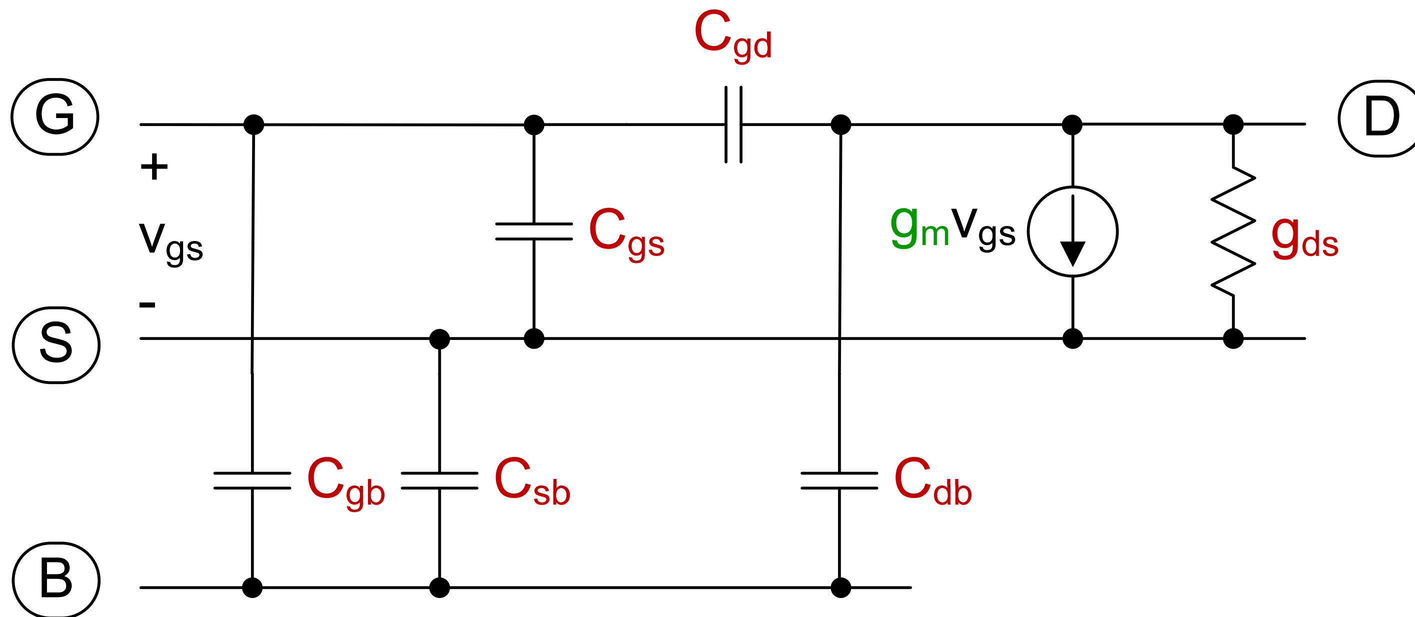
$$g_m = \frac{I_{DS}}{nkT/q} \qquad g_m = \frac{2I_{DS}}{V_{GS} - V_{th}}$$

- Transition point is:

$$V_{GS} - V_{th} = 2nkT/q \approx 70mV$$

  - It means, to operate transistors in strong-inversion, gate-overdrive must be at least 70mV
  - Note this is independent of the channel length L

MOSFET Small-Signal Model



$$C_{gg} \stackrel{!}{=} C_{gs} + C_{gb} + C_{gd} \qquad C_{dd} \stackrel{!}{=} C_{db} + C_{gd}$$

Note: body effect (gmb) term is not included

Output Resistance ($r_o = 1/g_{ds}$)

- Non-zero g_{ds} (= dI_{DS}/dV_{DS}) is caused by two main effects
  - Channel length modulation (CLM)
  - Threshold voltage variation (DIBL)
  - Typically modeled as $I_{DS} \propto (1+\lambda \cdot V_{DS})$ or $(1+V_{DS}/V_E L)$
- CLM: the effective channel length decreases as VDS ↑
  - $L_{eff} = L - \Delta L \qquad \Delta L = \zeta (V_D - V_{Dsat})$
- DIBL: drain voltage can influence the field at the source of short-channel devices and therefore change Vth
  - $V_{TH} = V_{TH0} - \eta V_{DS}$
- g_{ds} is not a good parameter for your designs to rely on

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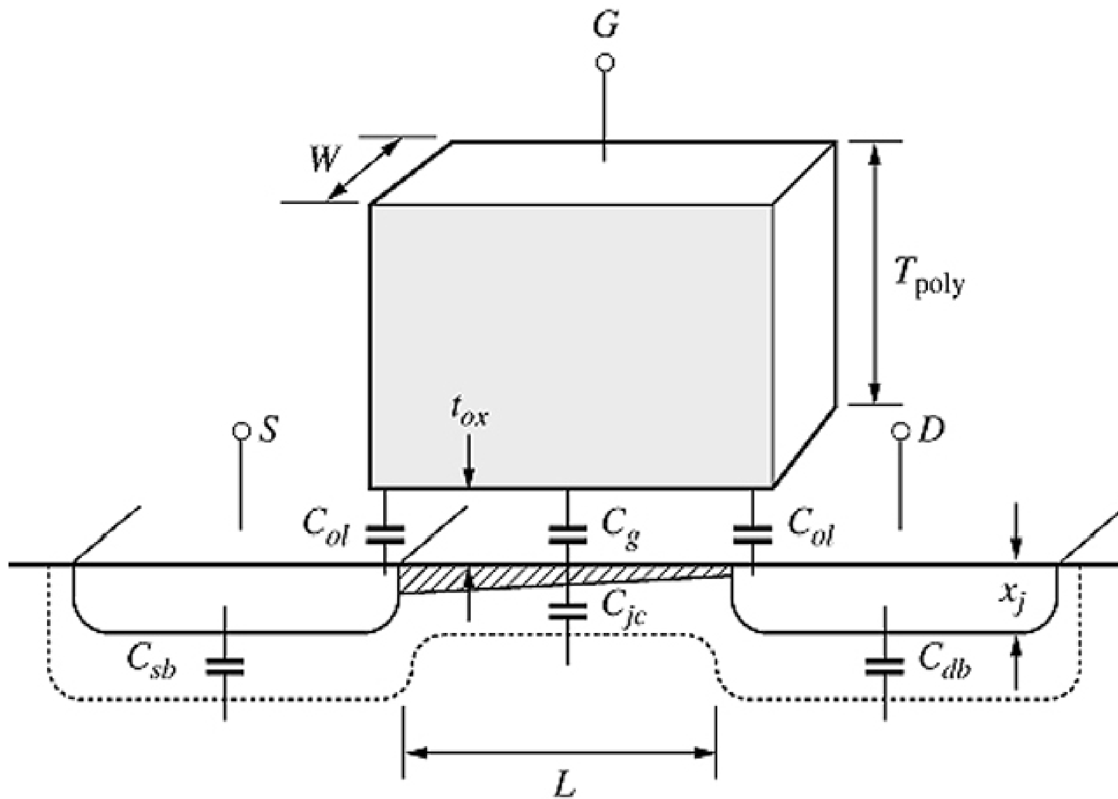
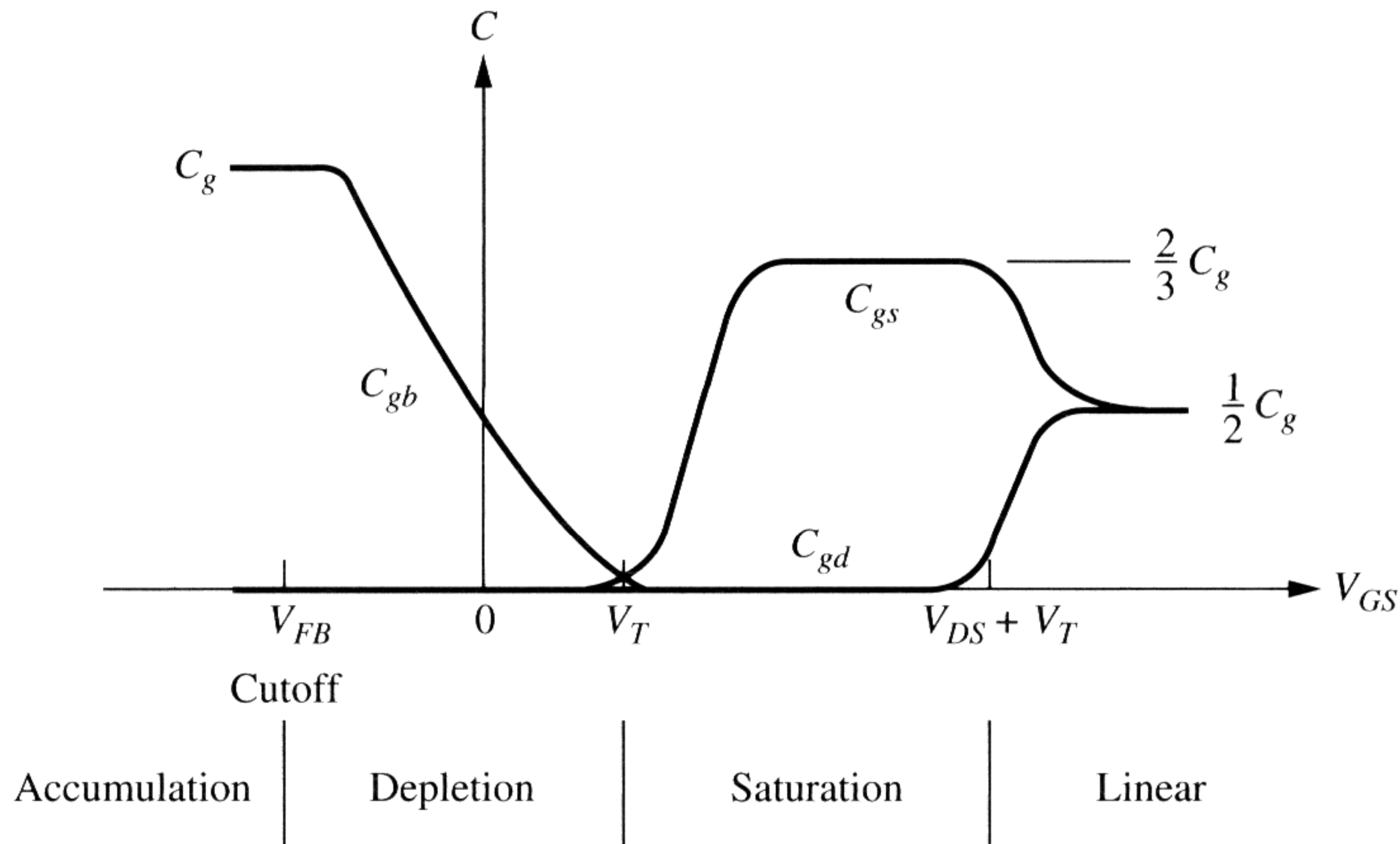
MOS Capacitance Model



- C_g - gate capacitance
- C_{jc} – depletion layer
- C_{sb}, C_{db} junction caps
- C_{ol} "overlap capacitance"

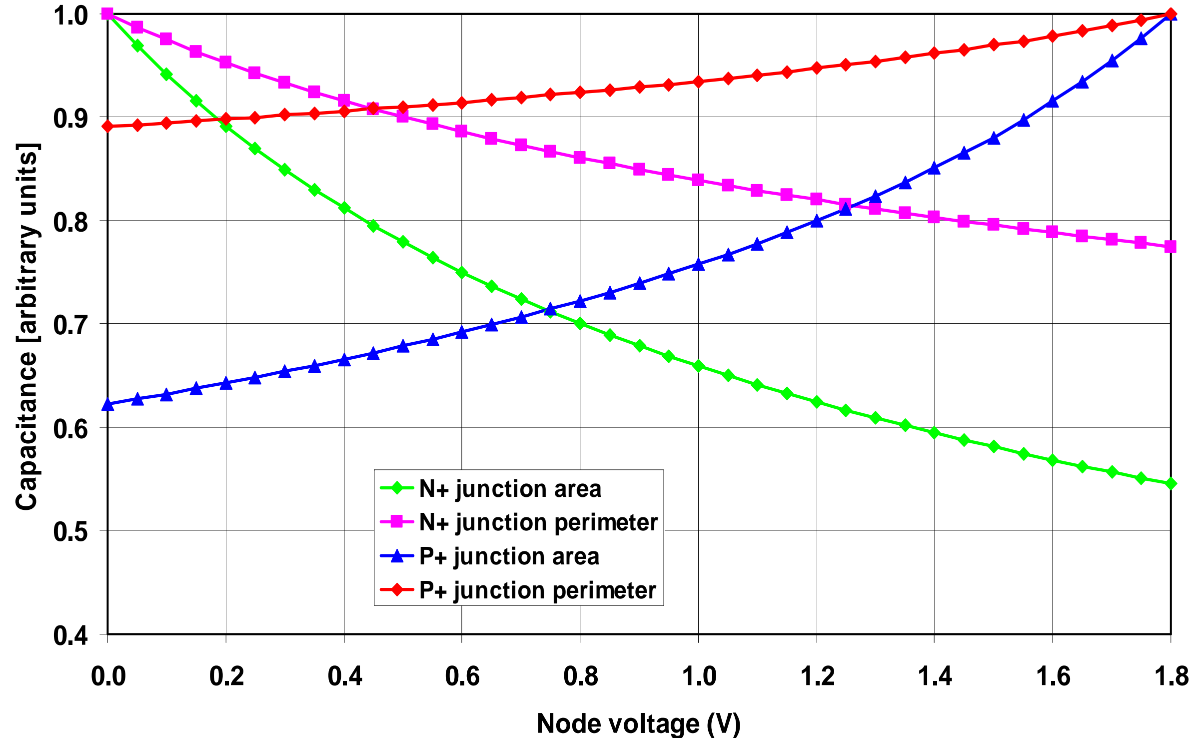
Gate Capacitance vs. V_{GS}



- Note: this picture ignores overlap and fringing components

Junction Capacitance at Source/Drain

- Junction capacitances are nonlinear, too
  - C_J is a function of junction bias



Basic Figures of Merit

Square Law

- Current efficiency
  - Want large g_m, for as little current as possible

$$\boxed{\frac{g_m}{I_D}} = \frac{2}{V_{OV}}$$

- Transit frequency
  - Want large g_m, without large C_{gg}

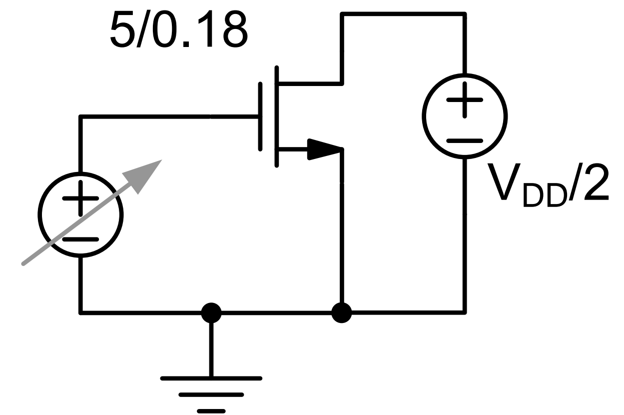
$$\boxed{\frac{g_m}{C_{gg}}} = \frac{3}{2}\frac{\mu V_{OV}}{L^2}$$

- Intrinsic gain
  - Want large g_m, but no g_{ds}

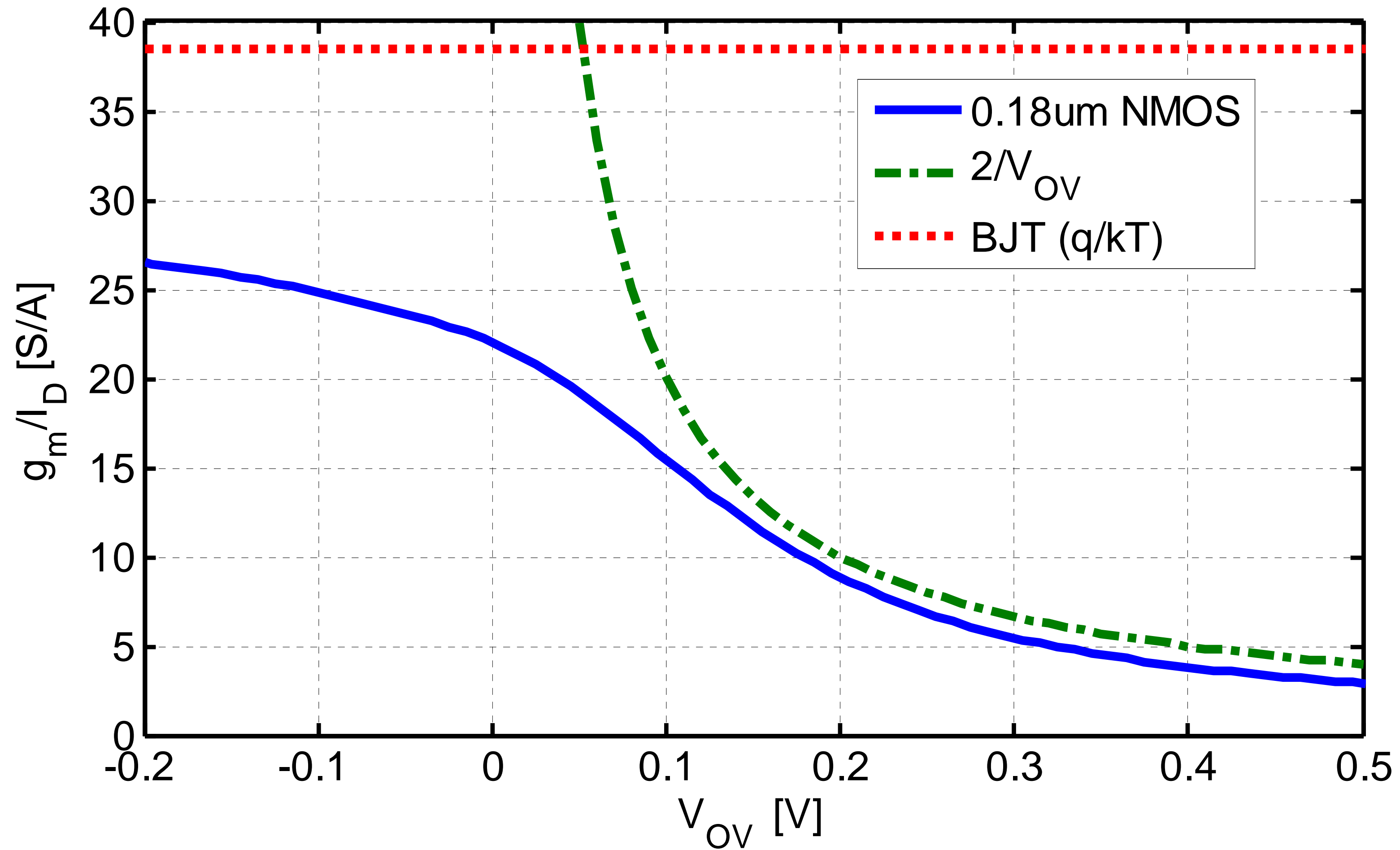
$$\boxed{\frac{g_m}{g_{ds}}} \cong \frac{2}{\lambda V_{OV}}$$

Device Characterization

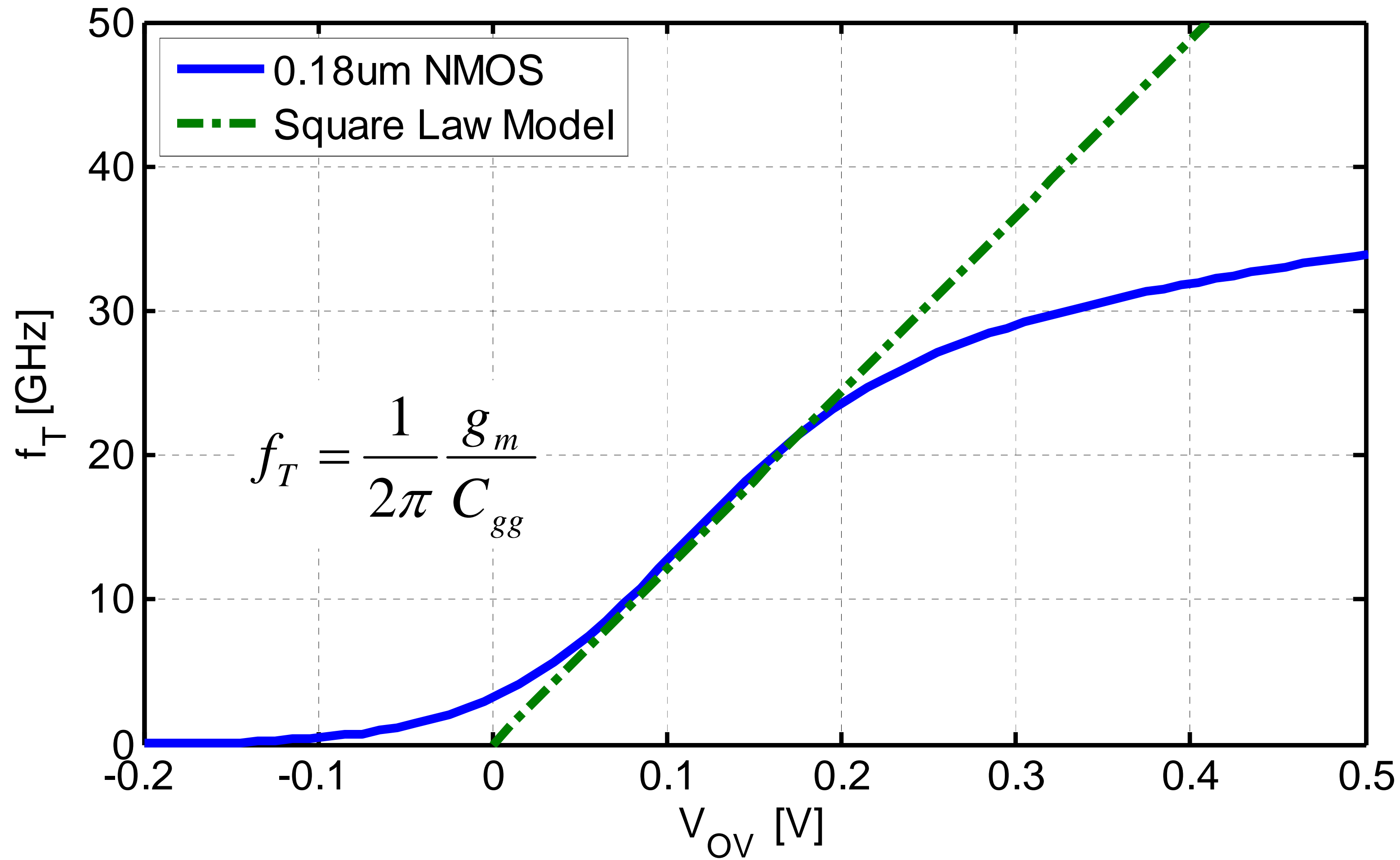
```
* gmid.sp
* NMOS characterization, L=0.18um

.param  gs=0.7
.param  dd=1.8
vds     d 0         dc   'dd/2'
vgs     g 0         dc   'gs'
mn      d g 0 0     nch  L=0.18um  W=5um

.op
.dc gs 0.2V 1V 10mV
.probe ov     = par('gs-vth(mn)')
.probe gm_id  = par('gmo(mn)/i(mn)')
* For BSIM4, use cggbm in the following line
.probe ft     = par('1/6.28*gmo(mn)/cggbo(mn)')
.probe gm_gds = par('gmo(mn)/gdso(mn)')

.options post brief dccap
.inc cmos018.sp
.end
```



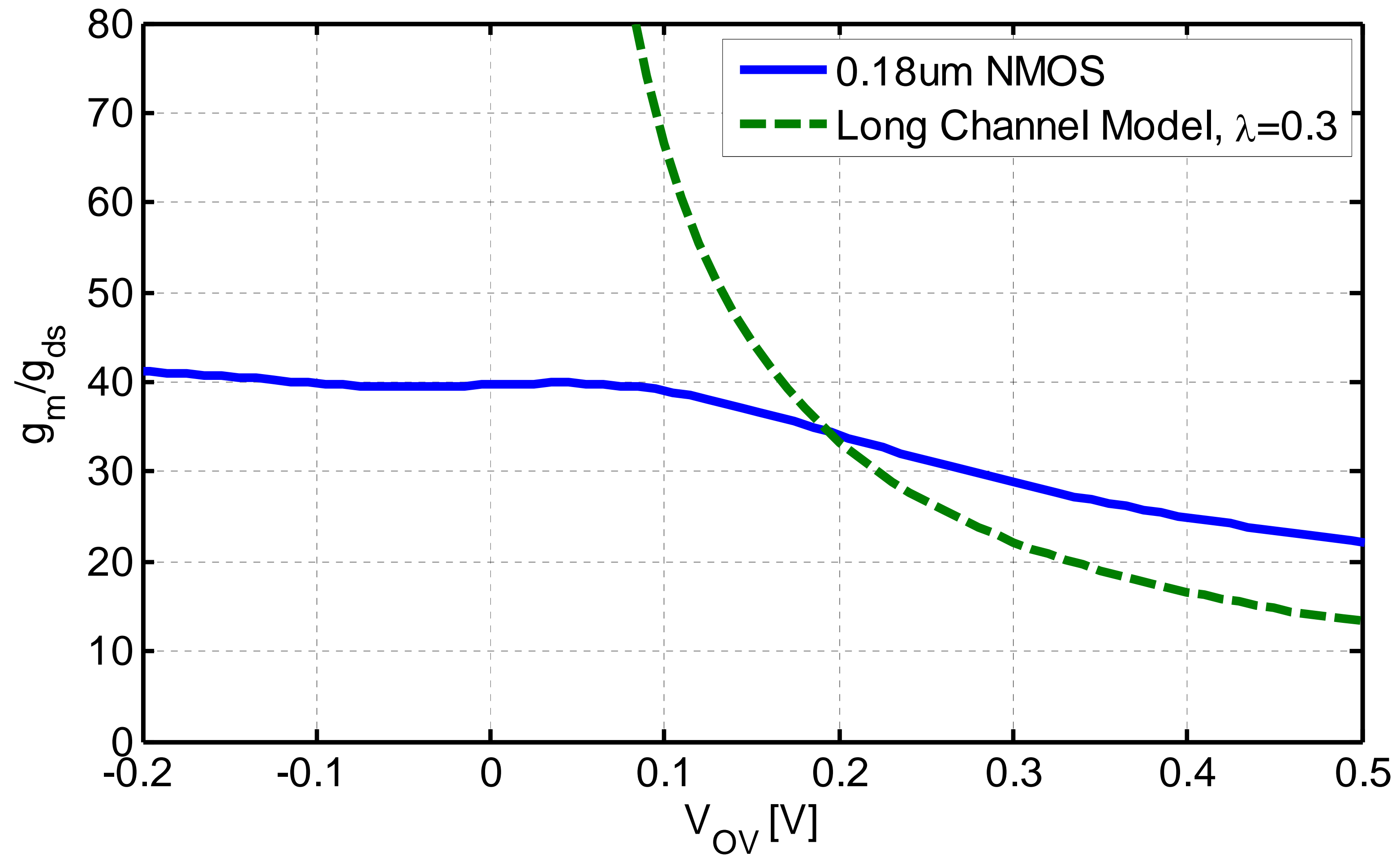
g_m/I_D Plot



Transit Frequency Plot



Intrinsic Gain Plot



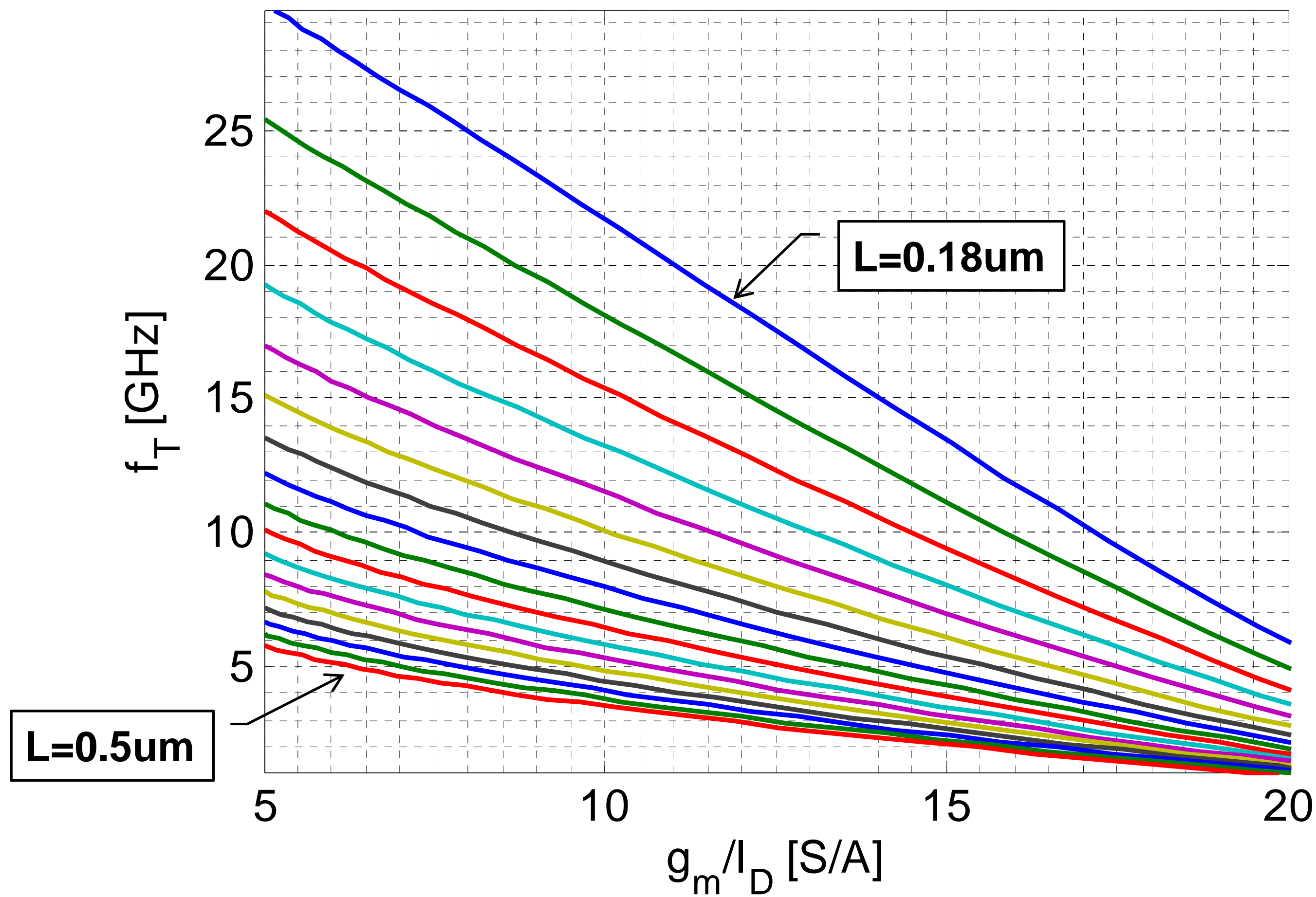
Assignment – Technology Characterization

- Plot the Id-Vds curves for W/L=20λ/2λ nMOS & pMOS
  - Characterize Ron (from linear region) for each V_{GS}
  - Characterize gm (from saturation region) for each V_{GS}
- Plot Id-Vgs curves for Vds=Vdd/2
  - Also plot as gm and gds as function Vgs
- Characterize the capacitance components
  - The components listed in slide 13 vs. Vds or Vgs
- Measure second-order effects such as:
  - Body effect: Vth vs. V_{BS}
  - Short-channel effect: Vth vs. L
  - Narrow-channel effect: Vth vs. W

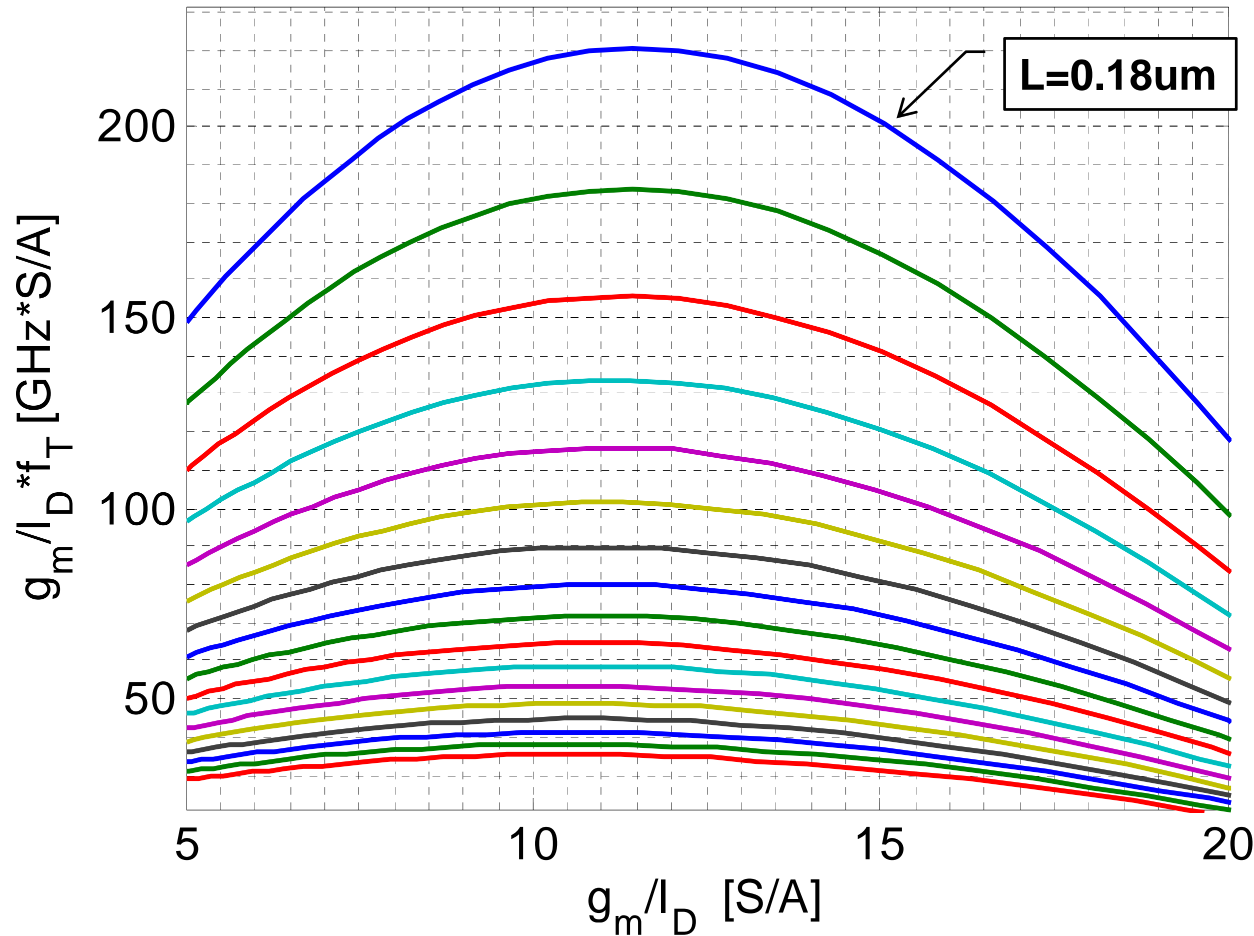
Assignment – cont'd

- Plot the following parameters for a reasonable range of g_m/I_D and channel lengths for various technologies
  - Transit frequency (f_T)
  - Intrinsic gain (g_m/g_{ds})
  - Current density (I_D/W)
- In addition, tabulate relative estimates of extrinsic capacitances
  - C_{gd}/C_{gg} and C_{dd}/C_{gg}
- Tip: try to automate the procedure as much as you can
  - Using mulan/simba script

Transit Frequency Plot

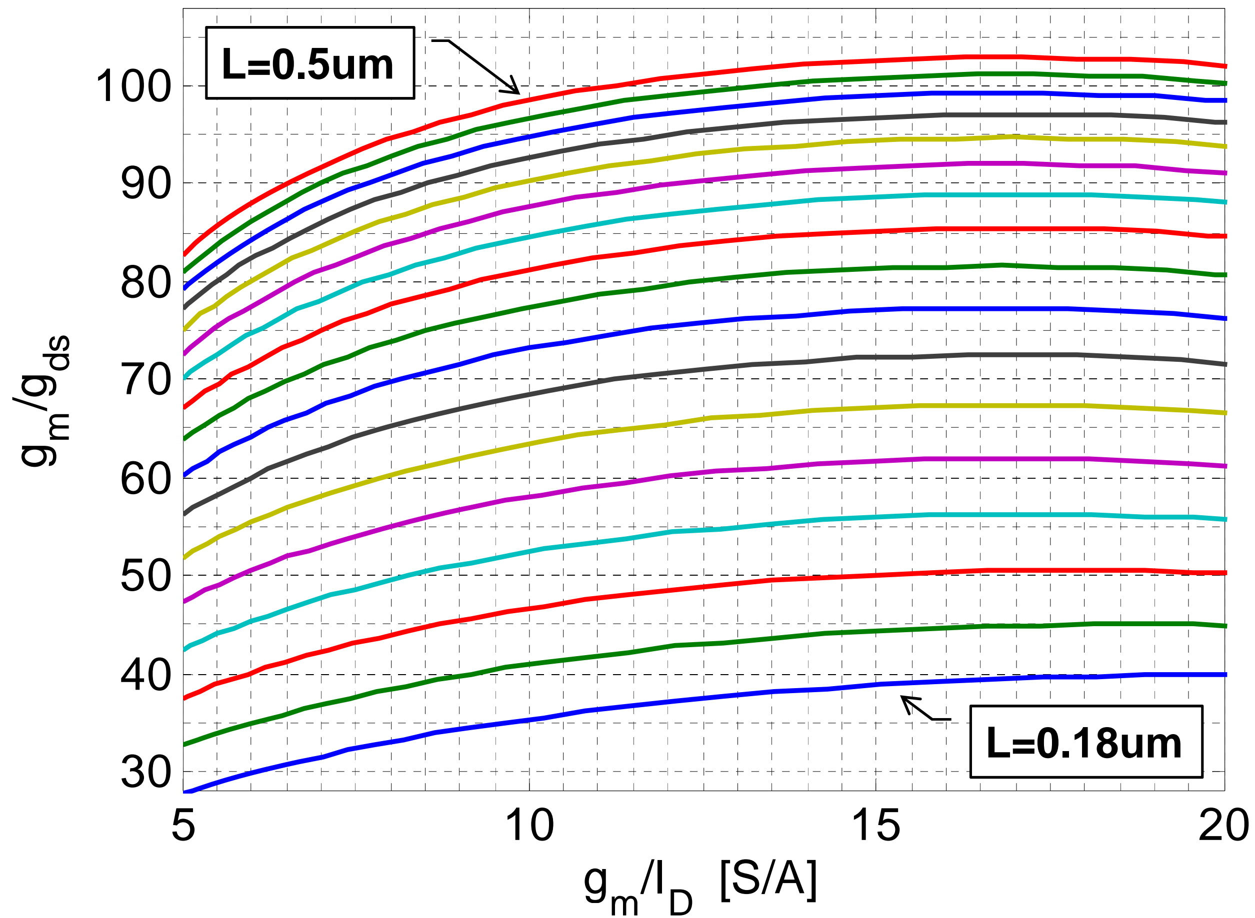


Sweet Spot



- g_m/I_D ~ 10..12 S/A can be a good choice for designs in which power and speed are equally important

Intrinsic Gain Plot



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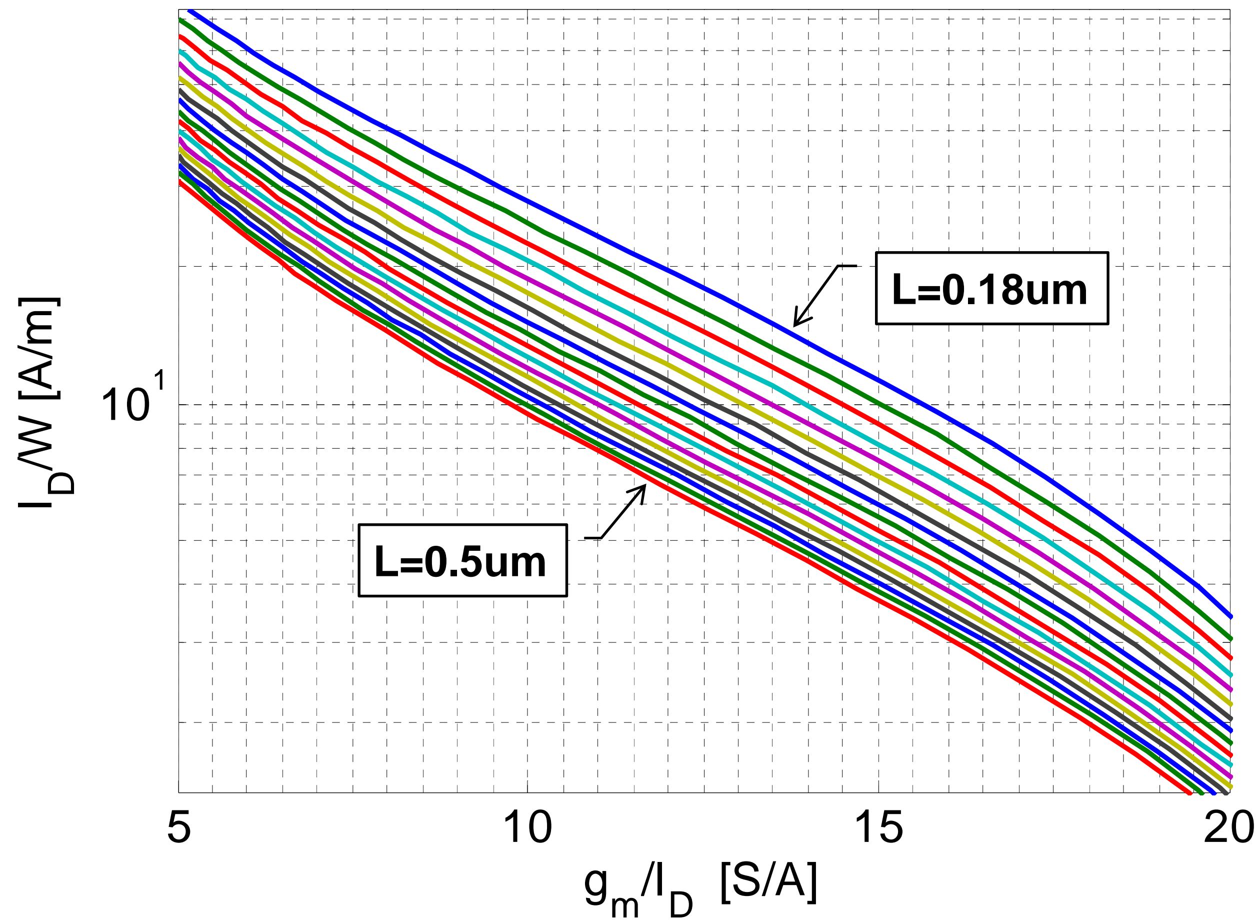
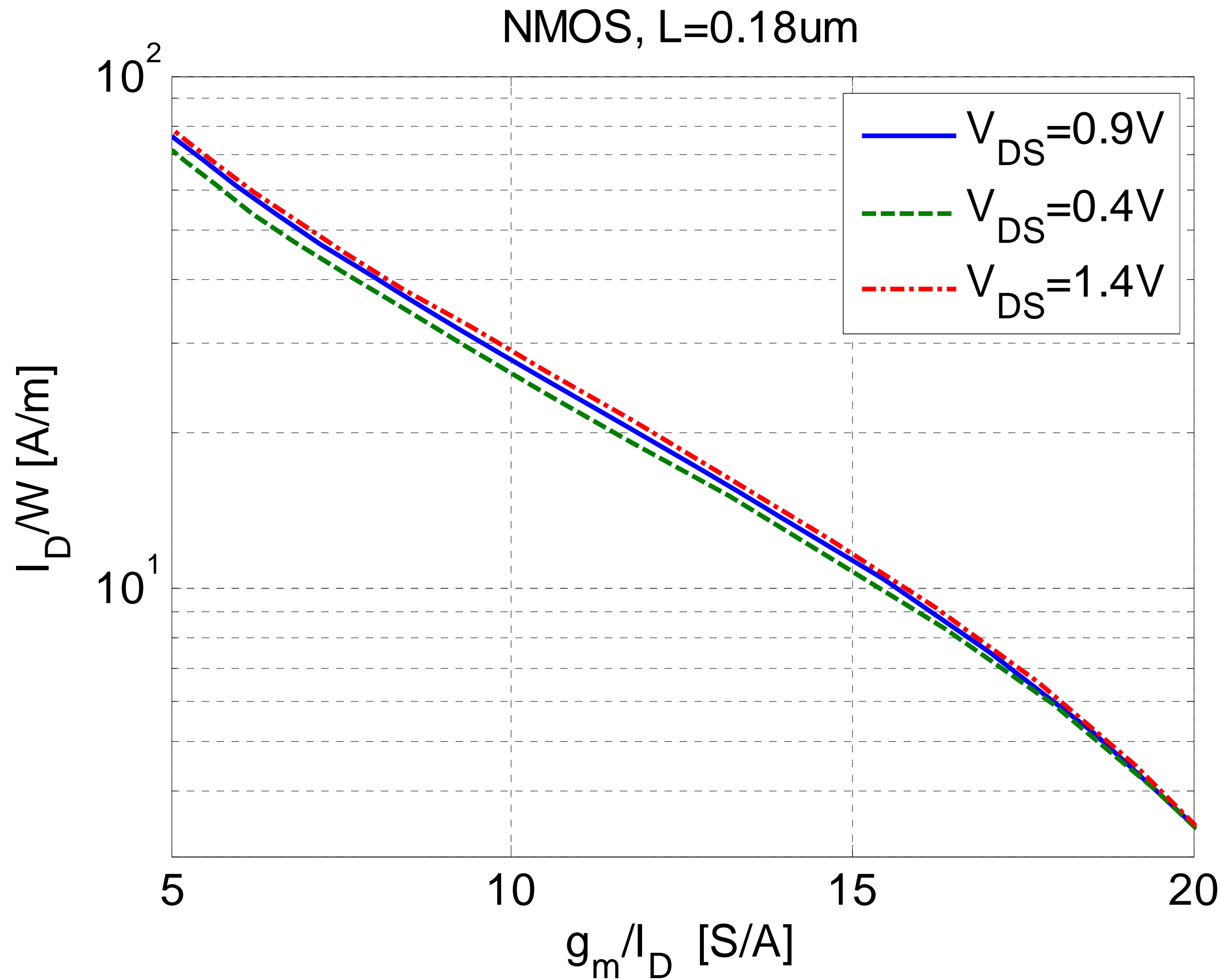
Current Density Plot (Sizing Chart)

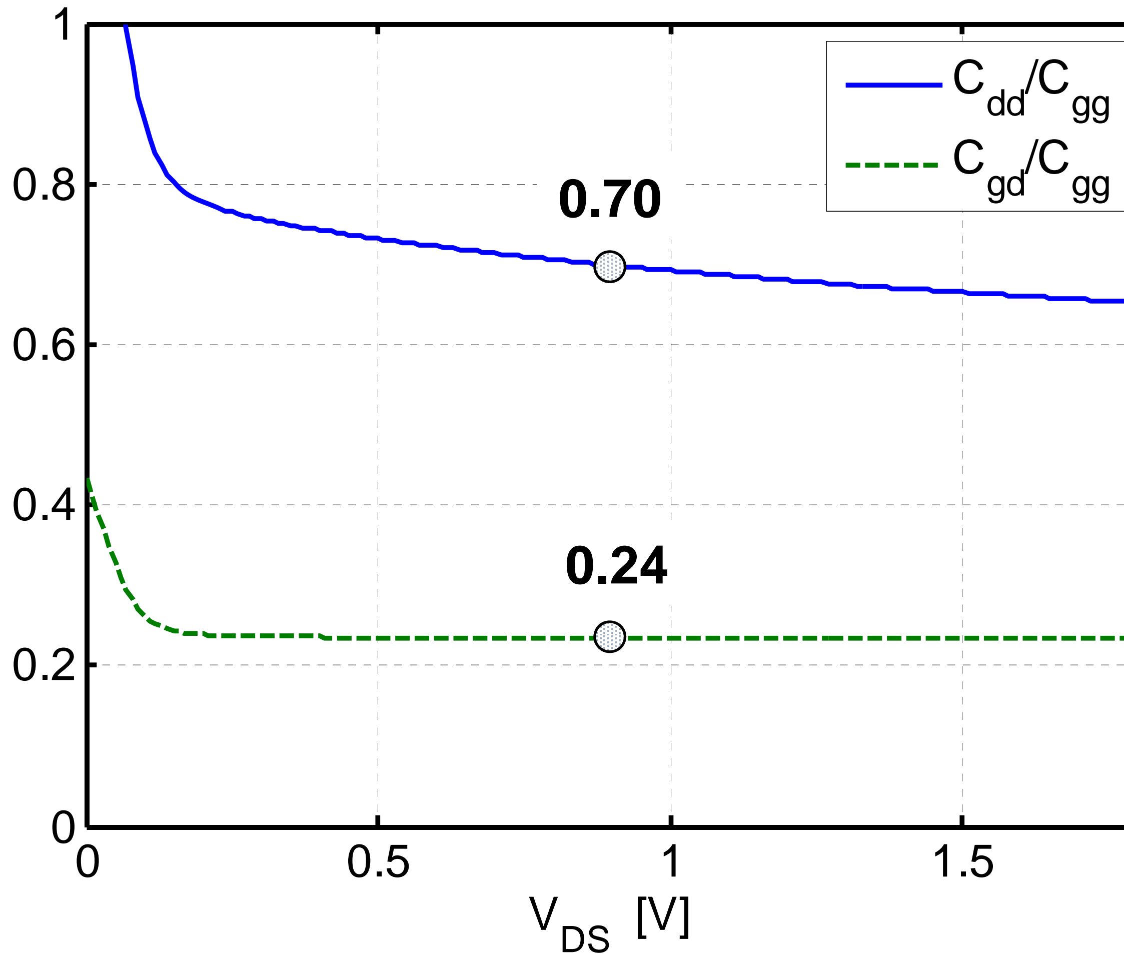


V_{DS} Dependence



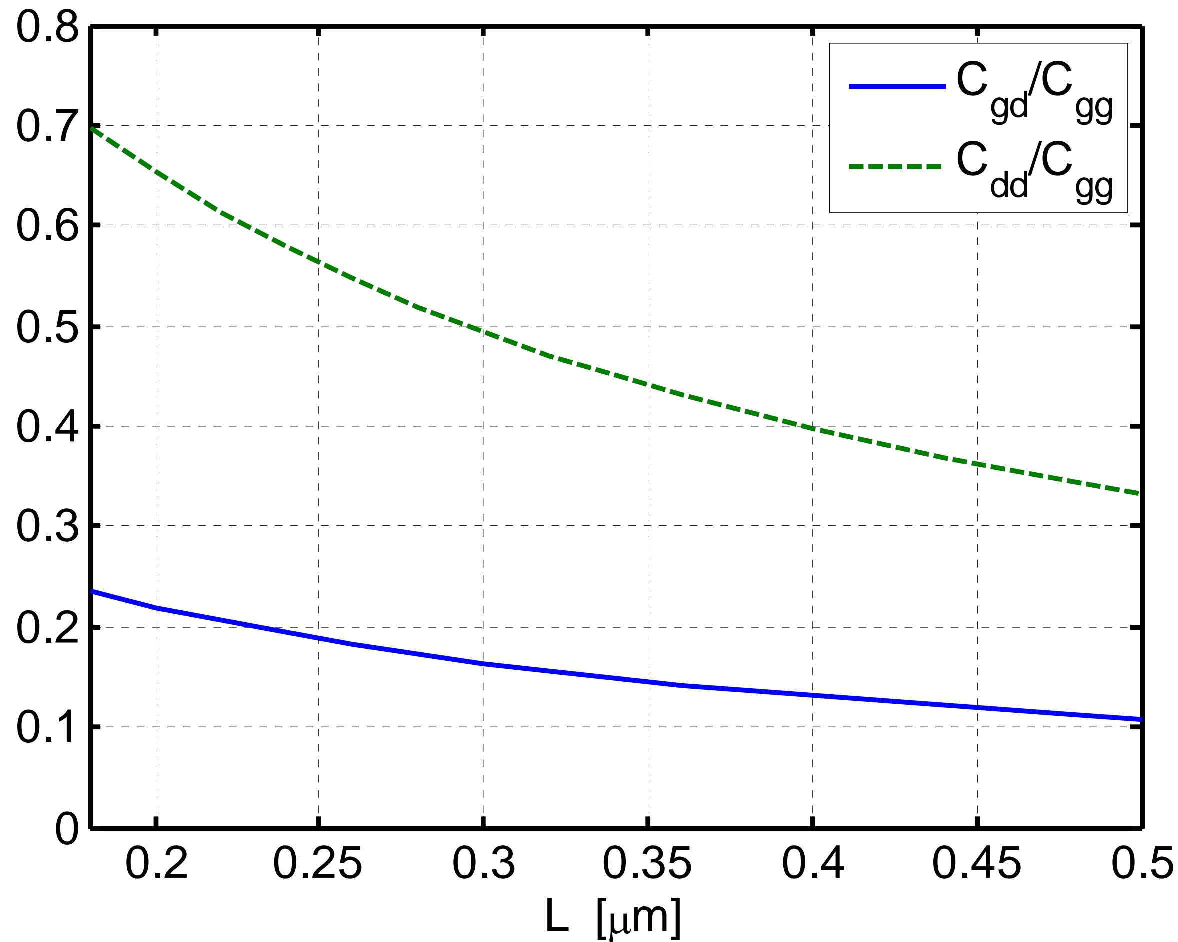
- V_{DS} dependence is relatively weak
- Typically OK to work with plots generated for $V_{DD}/2$

Extrinsic Capacitances (1)

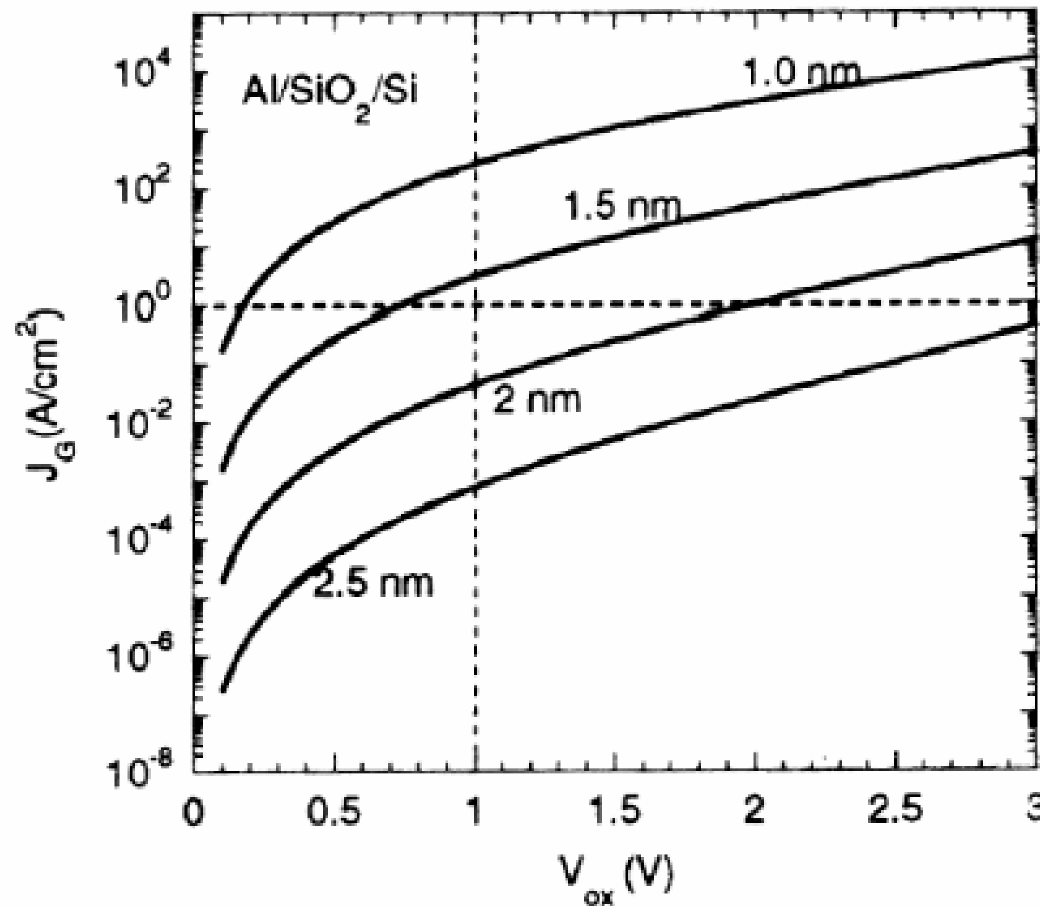


- Again, usually OK to work with estimates taken at $V_{DD}/2$

Extrinsic Capacitances (2)



Gate Leakage Current



For 0.1 µm CMOS :

$t_{ox} \approx 2$ nm

$J_G \approx 4\ 10^{-2}$ A/cm^2

For 10 x 0.5 µm

$I_G \approx 2$ nA

J_G (A/cm^2)

$\approx 4.5\ 10^5 \exp(-\frac{L}{6.5})$

L in nm

Ref. Koh, Tr ED 2001, 259-
Annema, JSSC Jan.05, 135.