Logic Design

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Before We Start ….
Passive vs. Active Learning

- After 2 weeks, we tend to remember

- Passive learning
  - 10% of what we read
  - 20% of what we hear
  - 30% of what we see (picture)
  - 50% of what we hear and see

- Active learning
  - 70% of what we say
  - 90% of what we say and do

Everybody! be an Active Learner

- recall prior material
- answer a question (say a lot!)
- guess the solution first (even guessing wrong will help you to remember the right approach)
- raise questions
- think of application
- imagine that you were the professor and think about how you would give a test on the subject material so that key concepts and results will be checked
- summarize a lecture, a set of homework or a lab in your own words concisely

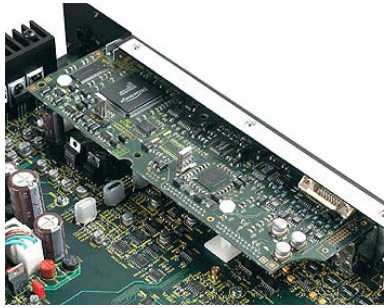
An Active Learner will become an Independent Researcher and Engineer

Course Information

- Class Meeting Times: Tue/Thur 4 - 5:15pm
- Office Hour: Tuesday 12 - 1pm at 301-409 (Lunch will be served by appointment)
  - come to me pretty often
- Textbook: Contemporary Logic Design, 2nd Edition: Randy H. Katz and Gaetano Borriello
- Contact:
  - Chang-Gun Lee (cglee@snu.ac.kr, 880-1862, 010-6549-5605)
  - TA: Kyung-soo Wee (we123456@naver.com)
- Grading (Tentative)
  - Attendance/Active participation: 10%
  - Homework & Projects: 15%
  - Midterm: 35%
  - Final: 40%

Course Philosophy

- Digital Logic Design is the base for many digital systems
  - Digital watch
  - DVD players
  - Cell Phones
  - Computers



- Students will be trained with
  - How to make digital systems from simple gates
  - How to optimize the design
  - How to validate your design
  - How to design digital systems just like SW programming

Topics

- **CMOS basics**
- **Simple Gates (AND, OR, NOT, NAND, NOR)**
- **Combinational Logic Design**
- **Sequential Logic Design**
- **Hardware Description Language**