

2007 Fall: Electronic Circuits 2

CHAPTER 10

DIGITAL CMOS LOGIC CIRCUITS

Y. Kwon

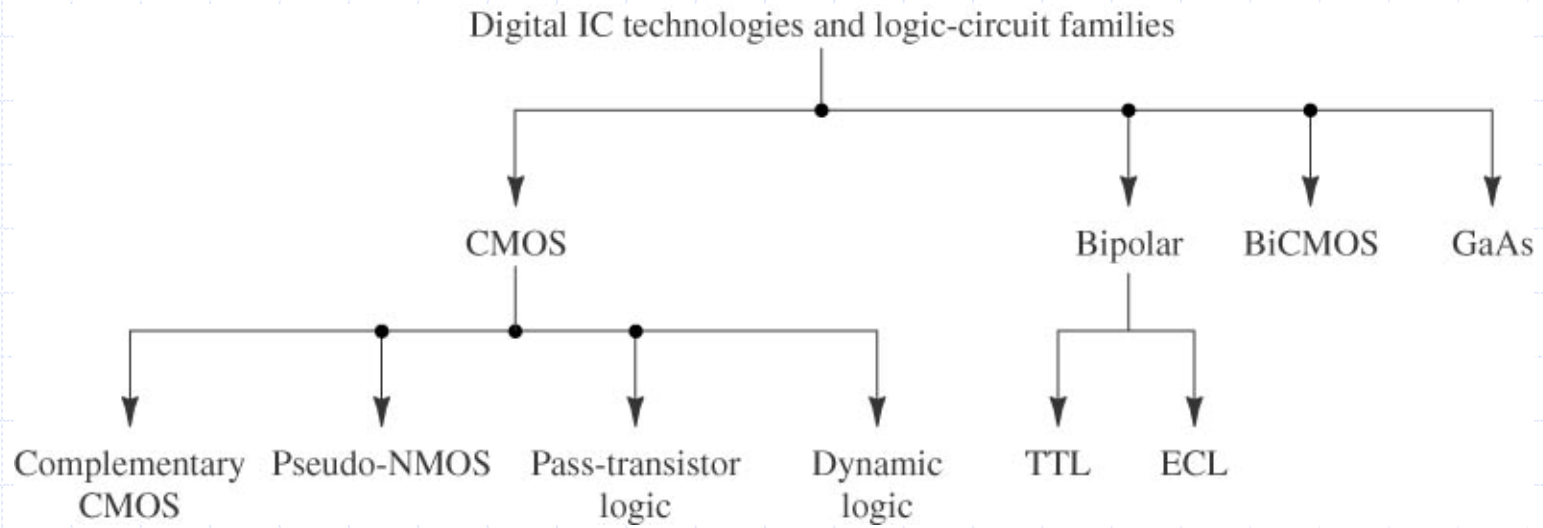
Introduction

◆ Chapter Outline

- 10.1 Digital Circuit Design
- 10.2 Design and Performance Analysis of the CMOS Inverter
- 10.3 CMOS Logic-Gate Circuits
- 10.4 Pseudo-NMOS Logic Circuits
- 10.5 Pass-Transistor Logic Circuits
- 10.6 Dynamic Logic

10.1 Digital Circuit Design

◆ Logic-Circuit Family



10.1.1 Digital IC Technologies and Logic-Circuit Families

◆ Brief remarks of four technology

■ CMOS

- ◆ Lower static power dissipation.
- ◆ High input impedance for temporary storage.
- ◆ Device scaling for higher level of integration.
- ◆ CMOS logic types: complementary CMOS, pseudo-NMOS, pass-transistor logic and dynamic CMOS logic.

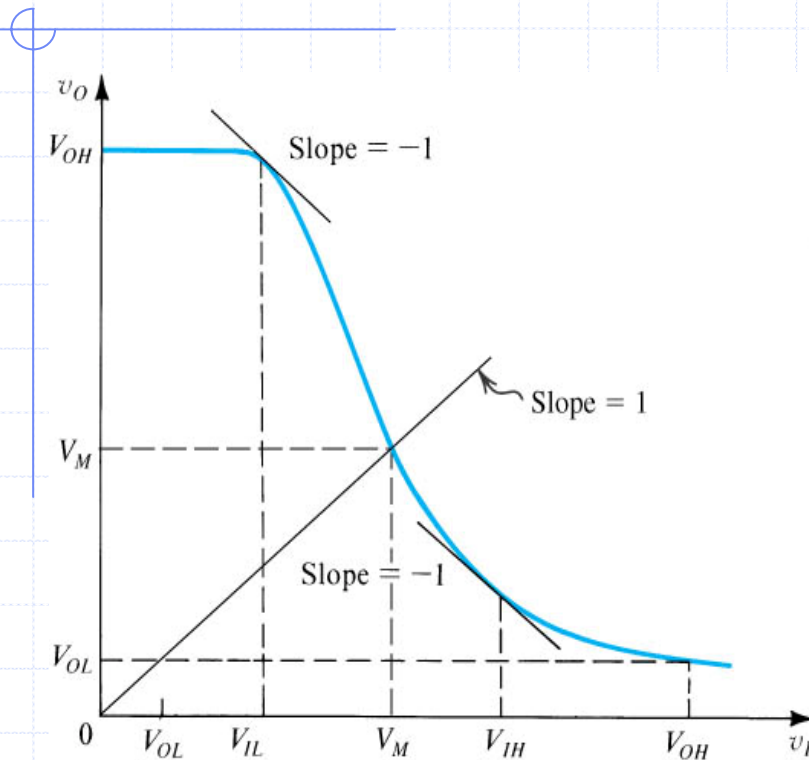
■ Bipolar

- ◆ Transistor-transistor logic (TTL or Schottky TTL)
- ◆ Emitter-coupled logic (ECL): suitable for high speed operation

■ BiCMOS

■ GaAs

10.1.2 Logic-Circuit Characterization



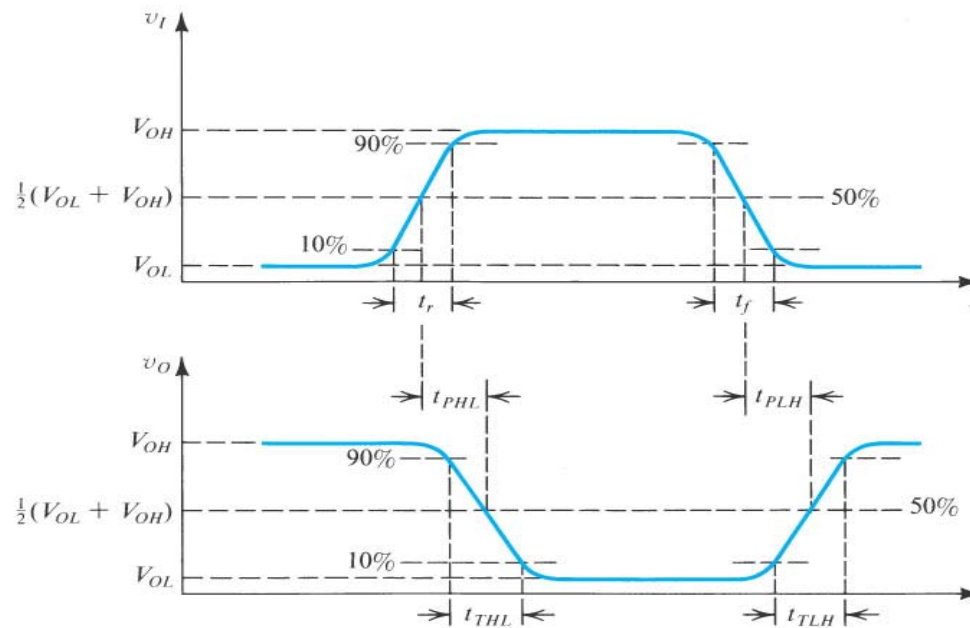
◆ Five parameters of VTC (voltage transfer characteristics)

- V_{OH} : maximum output voltage
- V_{OL} : minimum output voltage
- V_{IH} , V_{IL} : the point at the slope of VTC = -1
- V_M : (logic) the point of threshold voltage at $v_O = v_I$

$$◆ N_{MH} = V_{OH} - V_{IH}$$

$$◆ N_{ML} = V_{IL} - V_{OL}$$

10.1.2 Logic-Circuit Characterization



◆ Propagation Delay

- t_{PHL} : high-to-low propagation delay
- t_{PLH} : low-to-high propagation delay
- t_p (propagation delay) = $(t_{PLH} + t_{PHL})/2$

Logic-Circuit Characterization

◆ Power Dissipation

- Dynamic power dissipation happening during switching when both transistors are on.
- $P_D = fCV_{DD}^2$

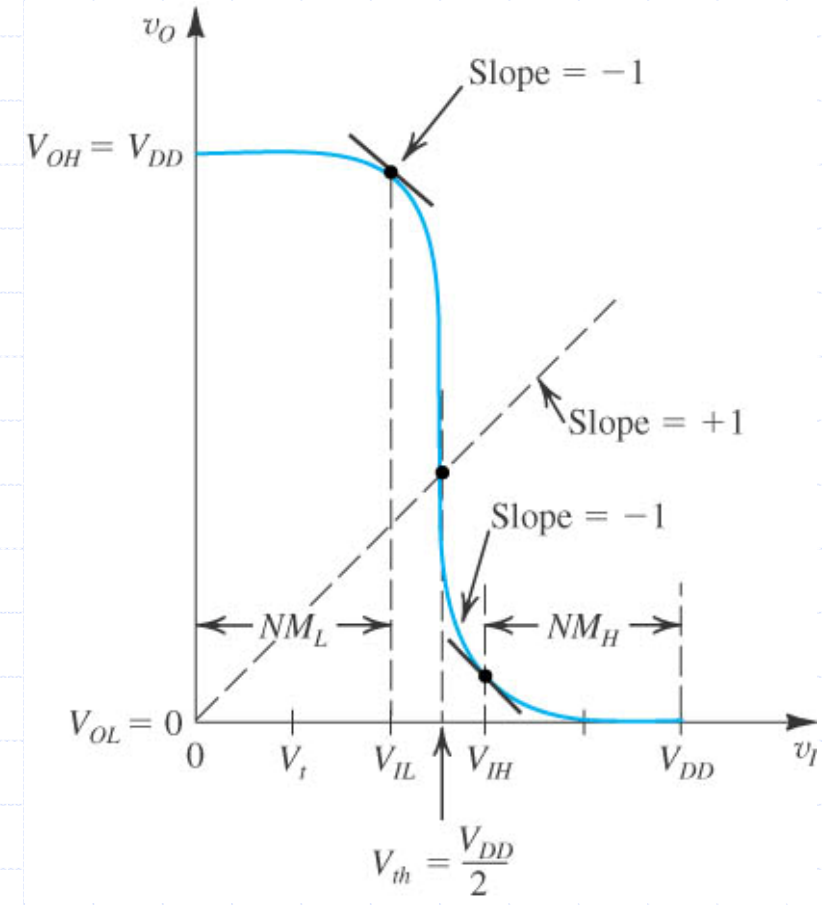
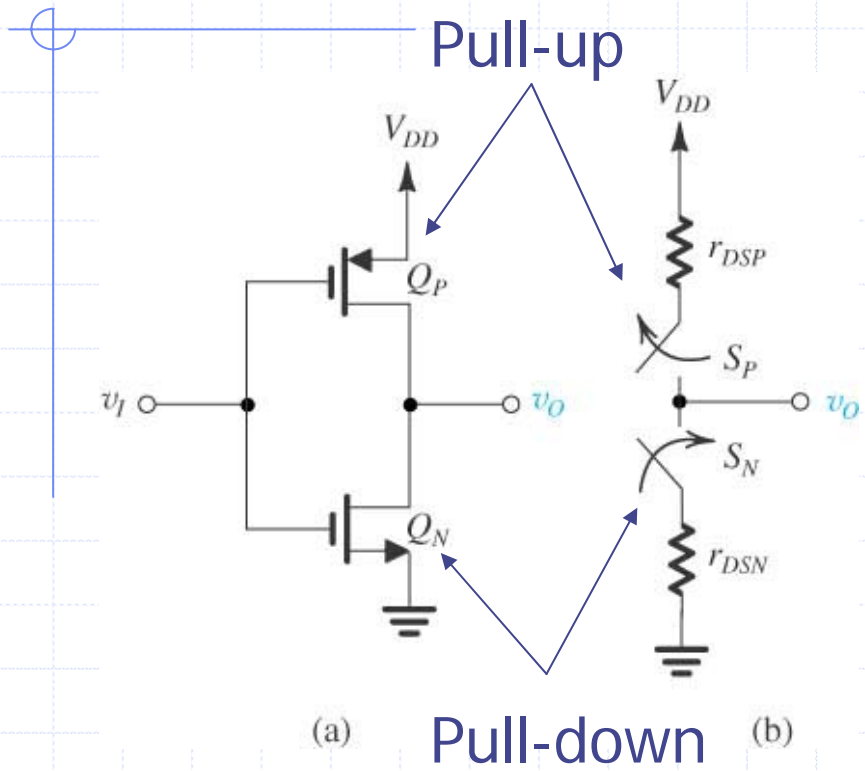
◆ Delay-Power Product

- Power reduction by reducing V_{DD} and current → takes more time to charge or discharge
- $DP = P_D t_P$

◆ Silicon Area

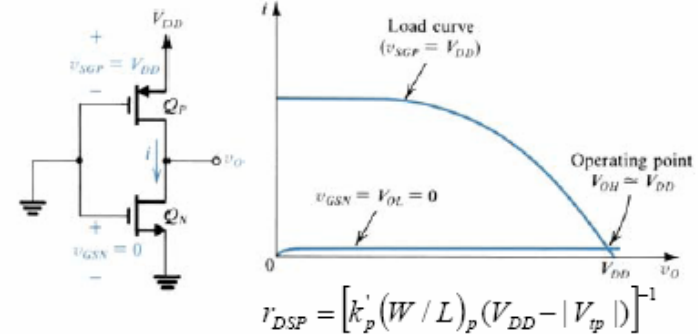
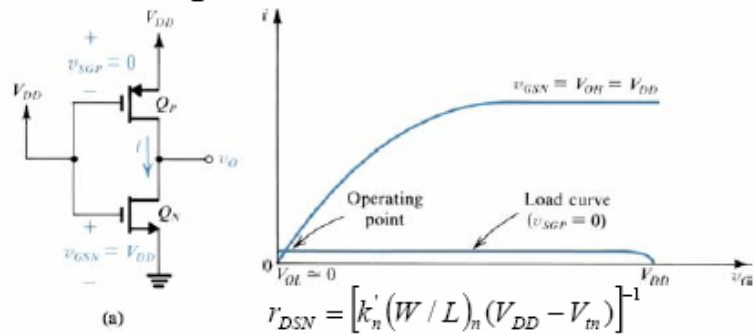
- Smaller transistors can reduce the silicon area, but current driving capability is limited → slow

10.2 Design and Performance Analysis

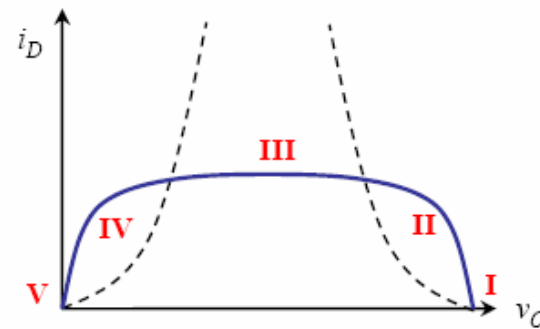
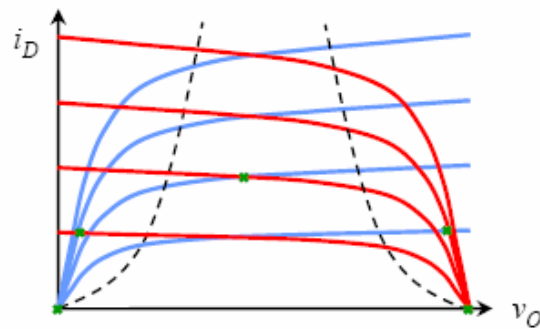
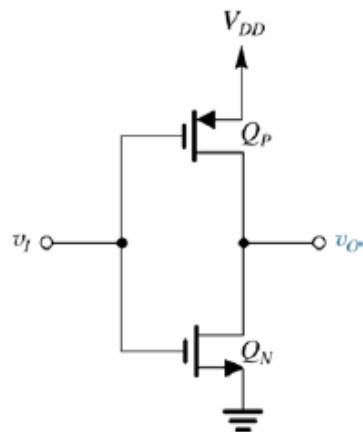


10.2.1 Circuit Structure

Circuit Operation



Voltage Transfer Characteristics



If Q_N and Q_P are matched:

$$\rightarrow k'_n \left(\frac{W}{L}\right)_n = k'_p \left(\frac{W}{L}\right)_p$$

$$\rightarrow V_m = -V_{tp} = V_t$$

Region	I	II	III	IV	V
Q_N	Cutoff	Sat	Sat	Triode	(Triode)
Q_P	(Triode)	Triode	Sat	Sat	cutoff

10.2.2 Static Operation

Static Operation

➤ Ratioless logic: V_{OH} and V_{OL} are independent of ratio of β_N and β_P .

$$\rightarrow V_{OH} = V_{DD}$$

$$\rightarrow V_{OL} = 0$$

➤ Static power dissipation is zero for both states.

➤ Switching threshold:
$$V_{th} = \frac{V_{DD} - |V_{tp}| + \sqrt{k_n/k_p} V_m}{1 + \sqrt{k_n/k_p}}$$

➤ Noise margins: $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$

➤ Matching: When both transistors have same transconductance parameters

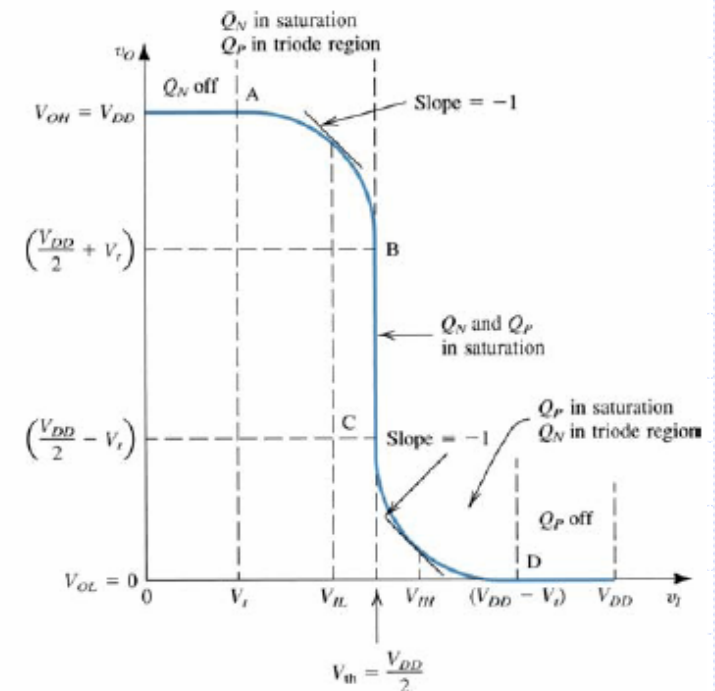
- $k_n'(W/L)_n = k_p'(W/L)_p$
- Equal driving capability for NMOS and PMOS.
- Switching threshold $V_{th} = V_{DD}/2$ in matched case.
- Noise margins in matched case:

$$V_{IH} = \frac{1}{8}(5V_{DD} - 2V_t)$$

$$NM_H = V_{OH} - V_{IH} = \frac{1}{8}(3V_{DD} + 2V_t)$$

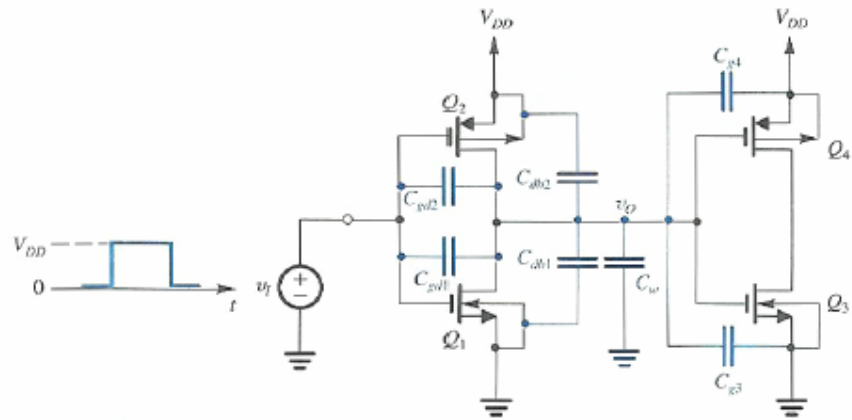
$$V_{IL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

$$NM_L = V_{IL} - V_{OL} = \frac{1}{8}(3V_{DD} + 2V_t)$$

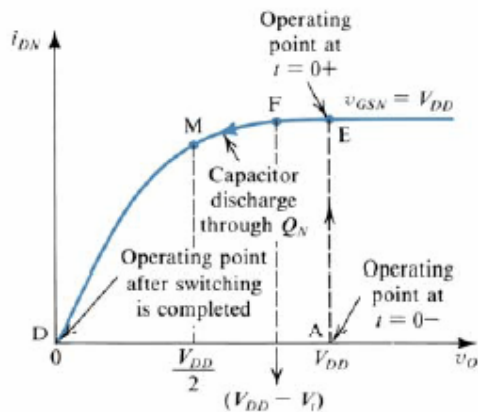
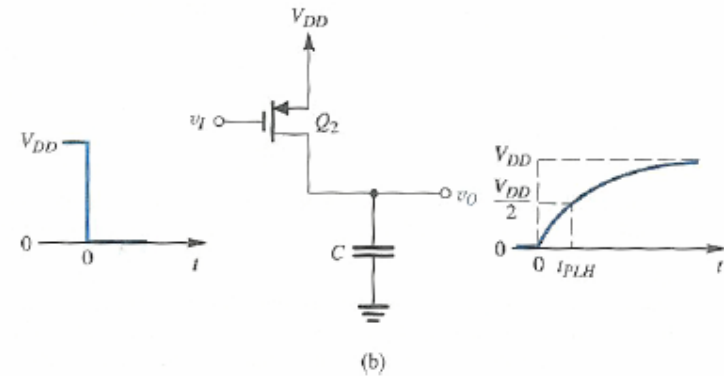
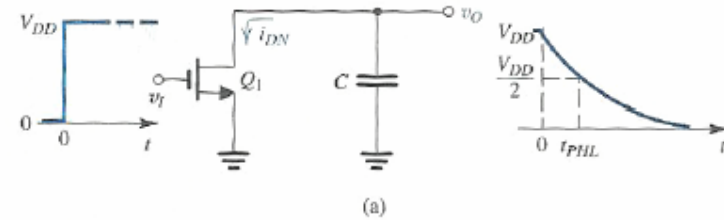


10.2.3 Dynamic Operation

Dynamic Operation



$$C = 2C_{gd1} + 2C_{gd2} + C_{db1} + C_{db2} + C_{g3} + C_{g4} + C_w$$



$$Q_N \text{ in saturation: } v_o = V_{DD} \sim V_{DD} - V_t \rightarrow t_{PHL1} = \frac{C[V_{DD} - (V_{DD} - V_t)]}{\frac{1}{2}k'_n \left(\frac{W}{L}\right)_n (V_{DD} - V_t)^2}$$

$$Q_N \text{ in triode: } v_o = V_{DD} - V_t \sim \frac{V_{DD}}{2} \rightarrow t_{PHL2} = \frac{C}{k'_n (W/L)_n (V_{DD} - V_t)} \ln\left(\frac{3V_{DD} - 4V_t}{V_{DD}}\right)$$

$$\rightarrow t_{PHL} = \frac{2C}{k'_n (W/L)_n (V_{DD} - V_t)} \left[\frac{V_t}{V_{DD} - V_t} + \frac{1}{2} \ln\left(\frac{3V_{DD} - 4V_t}{V_{DD}}\right) \right]$$

Propagation Delay

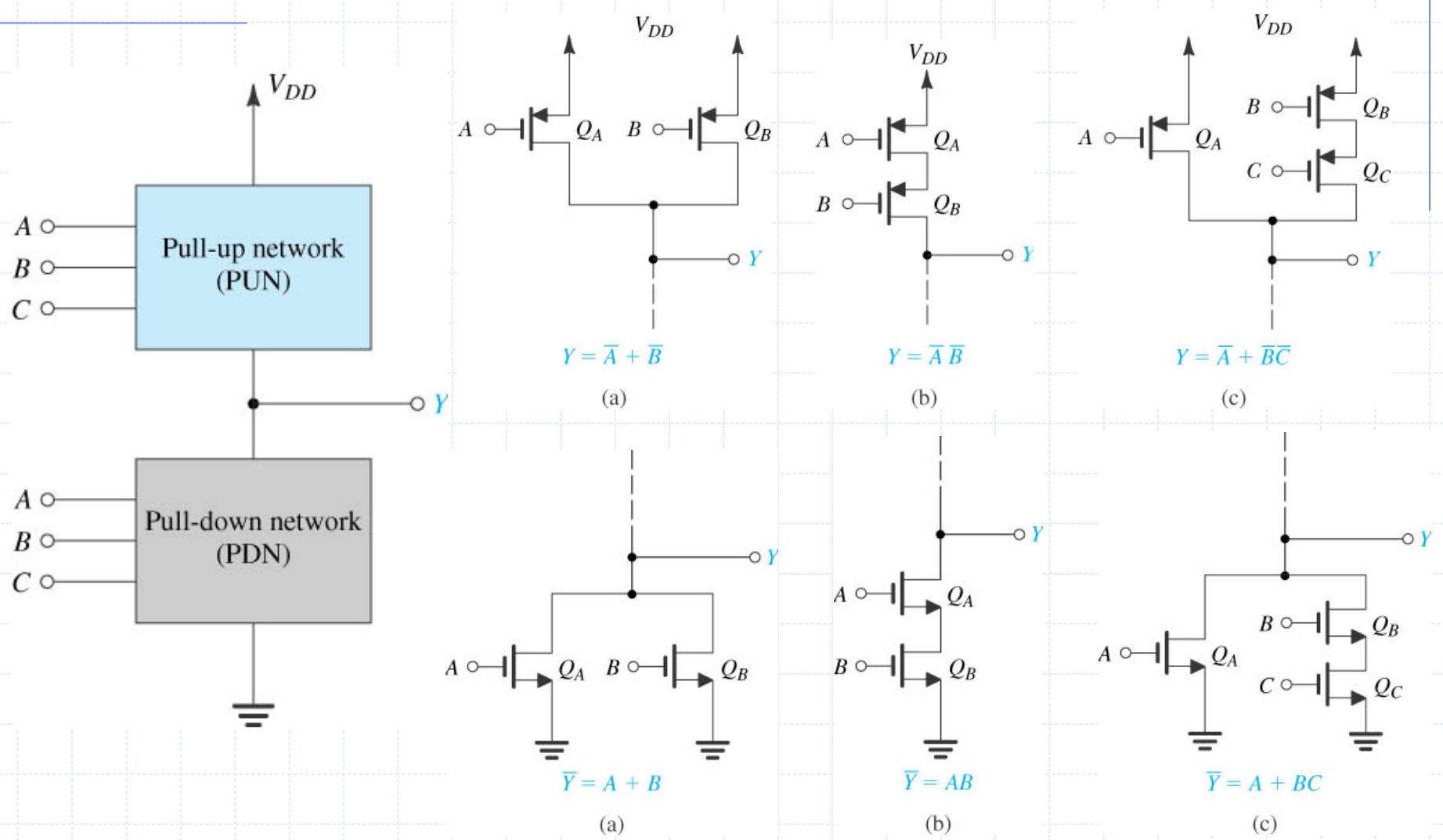
$$t_{PHL} = \frac{1.6C}{k'_n \left(\frac{W}{L}\right) V_{DD}}$$

- ◆ t_p can be equalized by matching
- ◆ Need to reduce C
- ◆ Need to use higher f_T device (G_m/C_g)
- ◆ Wider device (W/L) may help but C increase should be carefully gauged.
- ◆ V_{DD} increase, but limited by the process technology. Also, power dissipation should be considered.



Supplementary Material

10.3 CMOS Logic-gate Circuits



10.3 CMOS Logic-gate Circuits

A two-input CMOS NOR gate

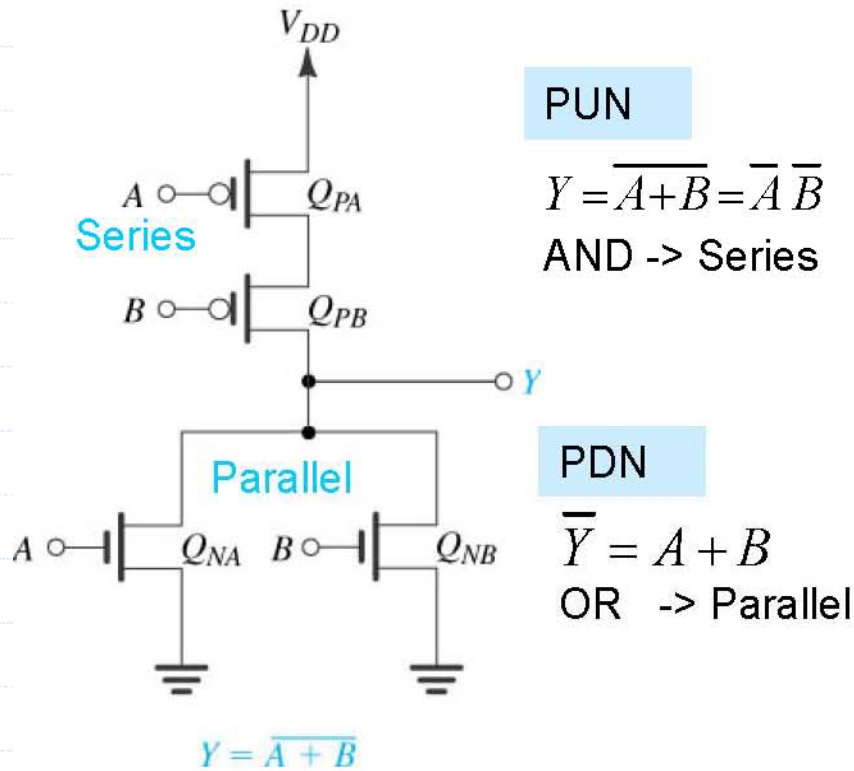


Figure 10.12 A two-input CMOS NOR gate.

$$Y = \overline{A+B} = \overline{A} \overline{B} \quad (10.21)$$

A two-input CMOS NAND gate

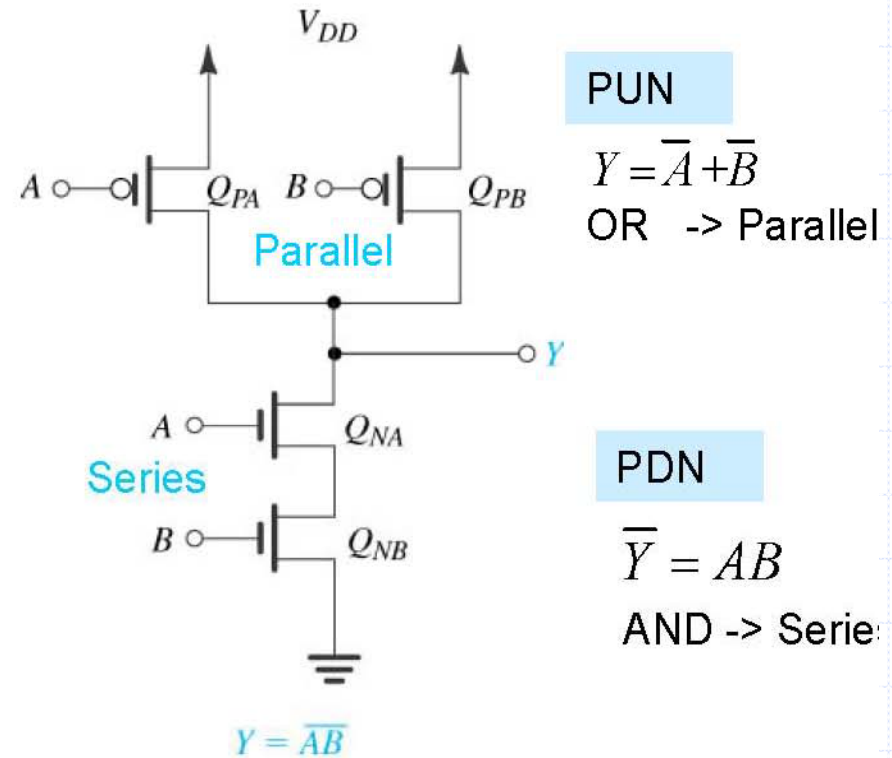
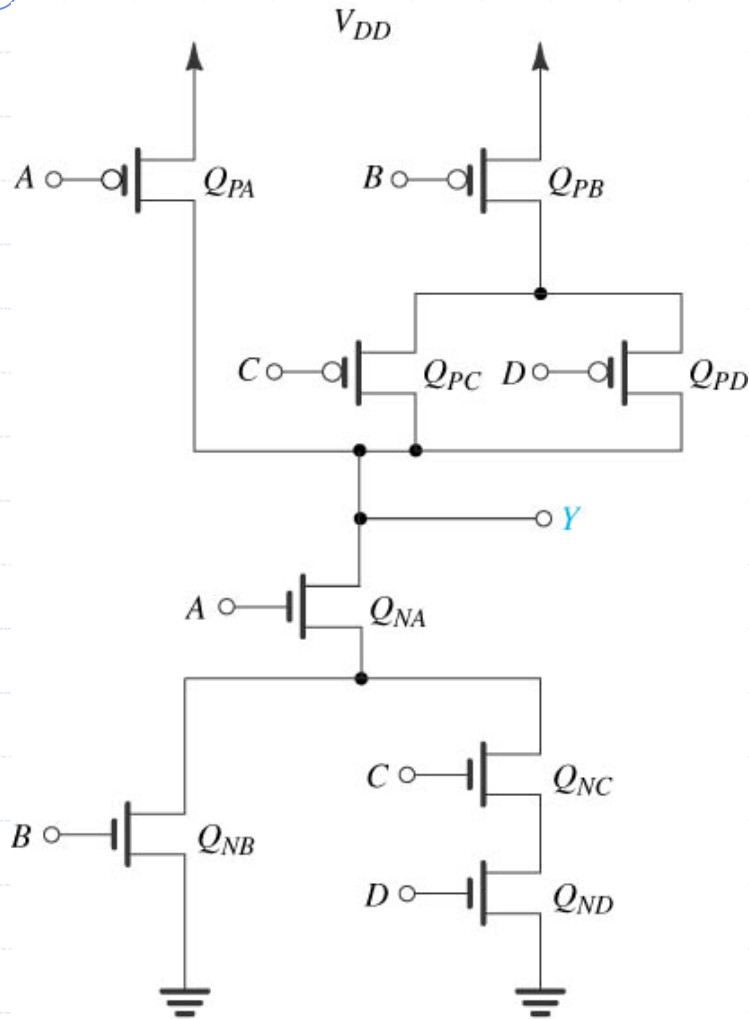


Figure 10.13 A two-input CMOS NAND gate.

$$Y = \overline{AB} = \overline{A} + \overline{B} \quad (10.22)$$

10.3.4 Complex Gate



$$Y = \overline{A(B + CD)}$$

$$Y = \overline{A(B + CD)} \quad (10.23) \Rightarrow \text{PDN}$$

$$= \overline{A + B + CD}$$

$$= \overline{A + BCD}$$

$$= \overline{A + B(\overline{C} + \overline{D})}$$

(10.23) \Rightarrow PDN

DeMorgan's theor

$$\overline{A + B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

(10.24) \Rightarrow PUN

10.3.6 The Exclusive-OR Function

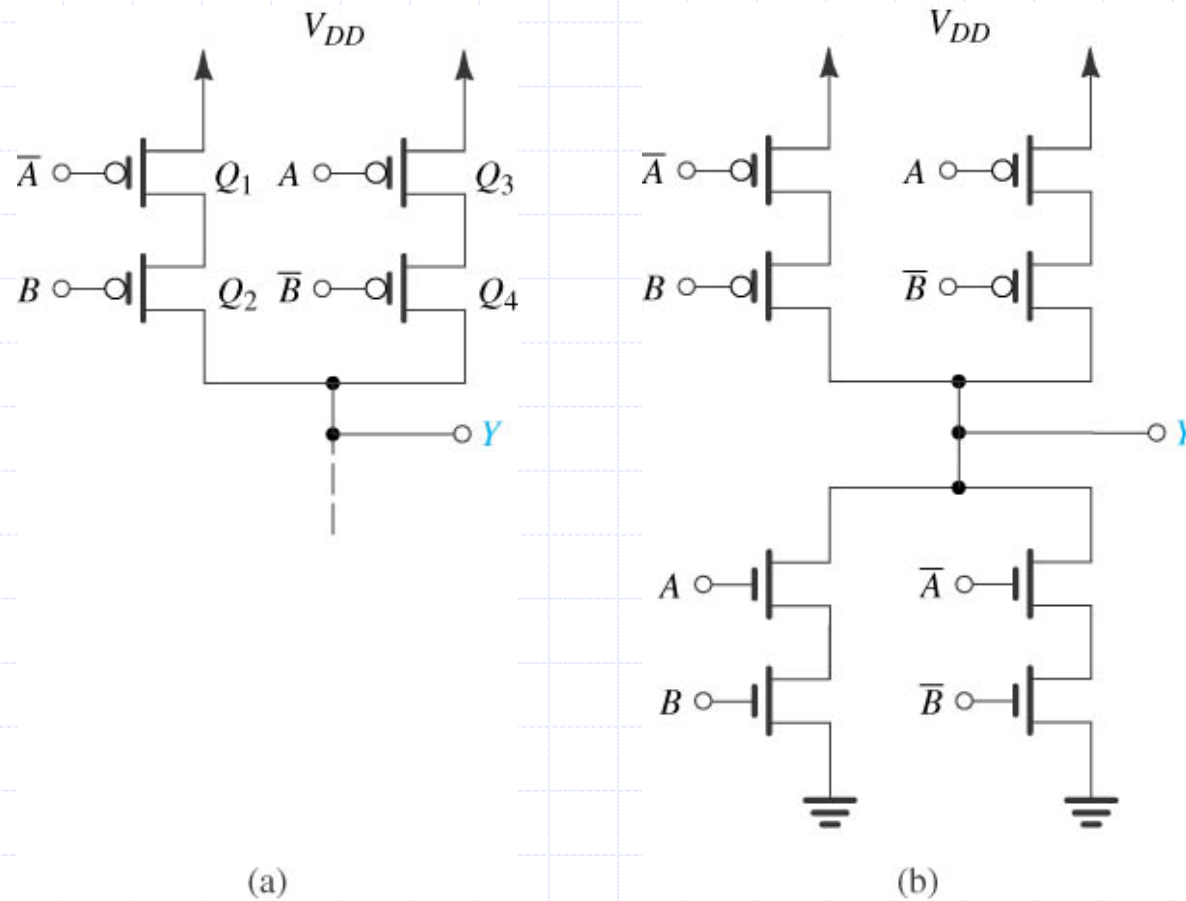


Figure 10.15 Realization of the exclusive-OR (XOR) function

10.3.8 Transistor Sizing

Series

$$\begin{aligned}R_{series} &= r_{DS1} + r_{DS2} + \dots \\&= \frac{\text{constant}}{(W/L)_1} + \frac{\text{constant}}{(W/L)_2} + \dots \\&= \text{constant} \left[\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \dots \right] \\&= \frac{\text{constant}}{(W/L)_{eq}}\end{aligned}$$

$$\therefore (W/L)_{eq} = \frac{1}{\frac{1}{(W/L)_1} + \frac{1}{(W/L)_2} + \dots} \quad (10.27)$$

Parallel

$$\begin{aligned}\frac{1}{R_{parallel}} &= \frac{1}{r_{DS1}} + \frac{1}{r_{DS2}} + \dots \\&= \frac{(W/L)_1}{\text{constant}} + \frac{(W/L)_2}{\text{constant}} + \dots \\&= \frac{1}{\text{constant}} [(W/L)_1 + (W/L)_2 + \dots] \\&= \frac{1}{\text{constant}} (W/L)_{eq}\end{aligned}$$

$$\therefore (W/L)_{eq} = (W/L)_1 + (W/L)_2 + \dots \quad (10.28)$$