7.5 Emerging Technology

- Shorter Wavelengths
- Tri-gate Transistor
- Nanoimprint Lithography
- Dip-Pen Nanolithography

7.5.1 Shorter Wavelengths

- Extreme UV (EUV), electron beam, and x-ray lithography.

TABLE 7.4 Radiation Wavelength and Minimum Resolution

Type of Radiation	Approx. Wavelength (nm)	Min. Resolution (nm)
Ultraviolet (UV)	193	45 [Hand 2006]
Ultraviolet immersion	193	32 [Hand 2006]
Extreme ultraviolet (EUV)	10–14	~22 [Lammers 2008]
Electron beam (e-beam)	2	~20 [Cumming 1996]
X-ray beam	0.8	~16 [Bourdillon and Vladimirsky 2006]

- To overcome the absorption problem, lenses are replaced by mirrors and coating -> high cost

- EUV: In 2011, the line resolution is reduced to 25 nm (Switzerland and Univ. of Wisconsin, Netherlands).

- E-beam: a feature size of ~ 12 nm was written on polymethyl-methacrylate (PMMA) and metalized with a titanium-gold alloy (Univ. New South Wales).
  *A problem with e-beams is they can induce a negative space-charge around the surface of nonconductive materials, which can distort the electron beam and limit its resolution.

7.5.2 Tri-gate Transistor

- In 2011, the design and fabrication of the Tri-gate transistor by Intel: a new 3-D gate FET.

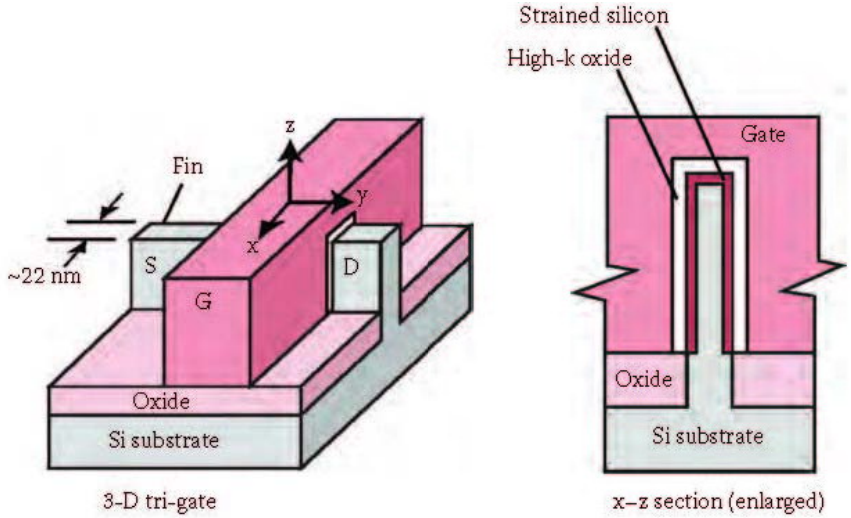

Figure 7.15 Illustration of the 3-D tri-gate transistor and a 2-D section taken in the x–z plane, where S = source, G = gate, and D = drain. The gate wraps around the all three sides of the fin. The x–z section is enlarged but not drawn to scale, and it shows the strained silicon (from Figure 7.11) and high-k oxide insulator (from Figure 7.10).

- 1) The reduction of the transistor size from 32 nm down to 22 nm size, 2) 32% faster and 50% lower power consumption than the 32 nm manufacturing process, 3) low carrier leakage, 4) greater carrier flow in the channel between the source and the drain.

- A ~ 22 nm wide silicon 'fin' rises vertically from the substrate. The fin represents both the source and drain in 3D. The 3-D gate is deposited, and it wraps around all three sides of the fin.
  *3-D gate has three transistors – 1 top-gate transistor and 2 side-gate transistors

7.5.3 Nanoimprint Lithography

- In the mid-1990's, features below 20 nm in size (S. Chou at Princeton Univ.).
  *low cost process – about one-tenth the cost of EUV, e-beam, and x-ray lithography.

- Nanoimprint lithography is a small version of stamping or embossing lithography where a mold is pressed onto a soft material to form a pattern.

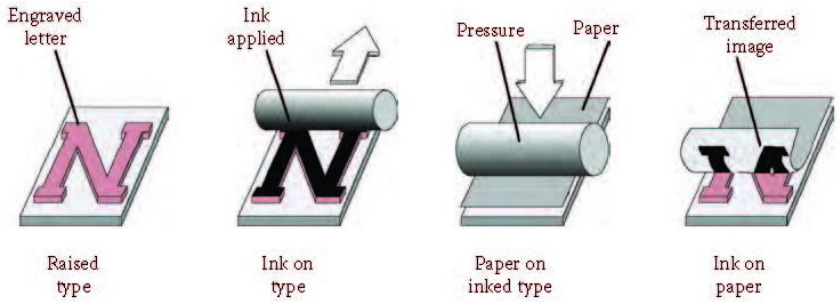

Figure 7.16 Illustration of stamping lithography used by Gutenberg as a method of printing. The process is as follows. Letter "N" (for nano) is engraved and raised on a metal plate. Ink is applied and it sticks to the letter. Paper is laid down and pressed onto the inked letter. The inked letter is transferred onto the paper.

- Two nanoimprinting processes: photo-curable (P) and thermal (T)
  *A template mold (coated with a release agent) with patterns and a substrate with an organic layer -> the replica of the mold.

(1) P-NIT uses an organic monomer layer made of low viscosity monomers (like acrylate or methy methacrylate) that can be polymerized through crosslinking under the exposure of UV light.

(2) T-NIT uses a thermoplastic polymer layer (polyethylene, nylon, or PMMA) heated above its glass transition temperature to develop viscous flow.

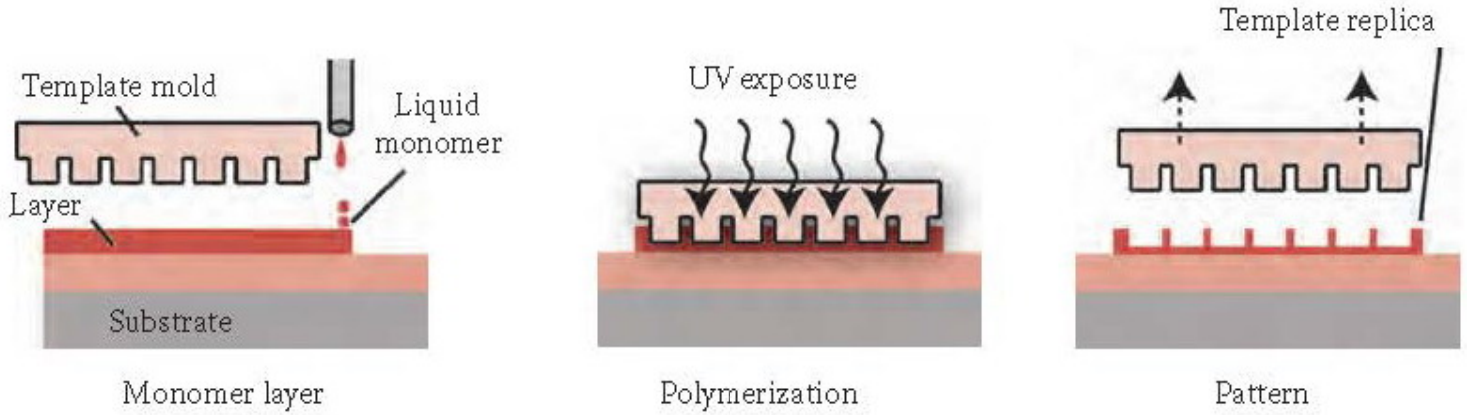

Figure 7.17 Illustration of photo-curable nanoimprint lithography, showing dispensing drops of liquid monomer forming a layer, lowering mold and polymerizing resist by UV exposure, and removing mold from template pattern. [Courtesy

- Feature sizes less than 20 nm can be fabricated.

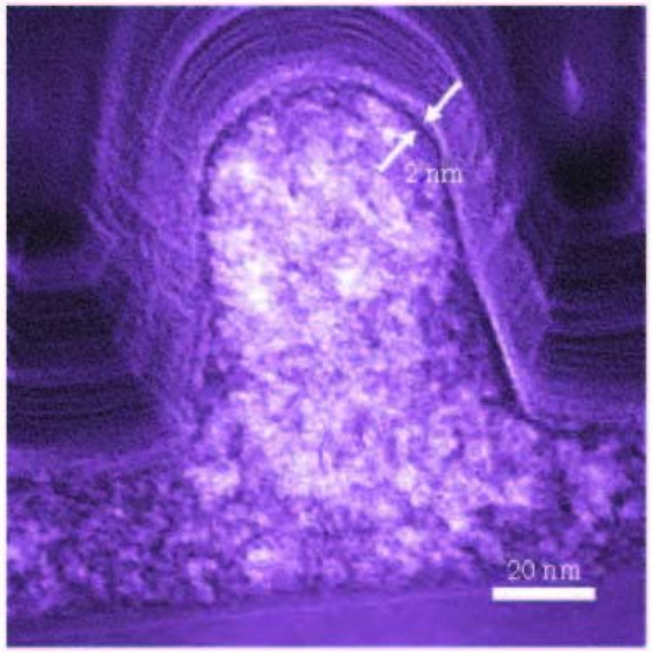

Figure 7.18 Electron micrograph showing the cross section of a spin-on organic glass (SOG), which is an insulator for semiconductor microcircuit. The process forms a dense, stronger skin about 2nm thick on the outside. [Courtesy

7.5.4 Dip-Pen Nanolithography

- Invented in the late-1990's (C. Mirkin, Northwestern Univ.) and being commercialized by Nanoink.

- The dip-pen process uses the tip of a cantilever probe in an AFM to deposit molecular ink onto a substrate. The ink flows from the pen tip onto the substrate by capillary action.

- The pen dispenses the solvent molecules through a meniscus and the molecules are then self-assembled onto the substrate. For the probe tip of a radius of ~5nm, line widths of ~ 20 nm.

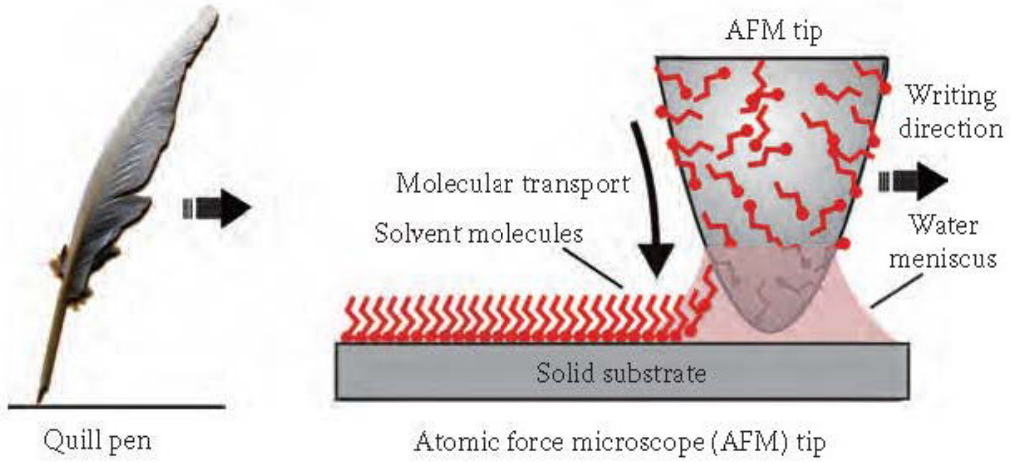

Figure 7.19 Illustration of quill pen to dispense ink and the probe tip of an AFM to dispense molecules that self-assemble onto a substrate. [Courtesy of C. Mirkin, Northwestern University, Evanston, IL.]

- The DPN does not need a mask, can deposit a wide range of inks in many different patterns for ICs.
  *For the probe tip of a radius of ~5nm, line widths of ~ 20 nm.

- In 2006, an electric field-assisted method was developed by IBM Almaden Research Center.
  *It only writes when an electric field is applied and not when the AFM tip contacts the substrate.

- This process is less sensitive to the molecules in the ink and the substrate than DPN.

7.6 Bottom-Up Technology

- Nanotubes
- Crossbar Arrays
- Magnetoresistive Memory
- Phase-Change Memory
- Quantum Bits

7.6.1 Nanotubes

- How does 'top-down' photolithography produce 'bottom-up' nanotube art?

  -> Growth of carbon nanotubes in selective areas (photoresist patterns achieved by photolithography) of the catalyst on the substrate.

- Three configurations: back-gated nanotubes, cantilever nanotubes, and fixed-end nanotubes.

(1) Back-gated nanotubes: a carbon nanotube is placed between the source and the drain.
*The nanotube substitutes for p-channel in the p-type silicon substrate. The nanotube makes contact with the SiO_2 dielectric, and gate is inverted and placed on the bottom of the transistor.

- Due to the short channel of the nanotube (~ 18nm), the source-to-drain conductive channel is shortened over the current 'top-down' transistors -> the switch is faster.

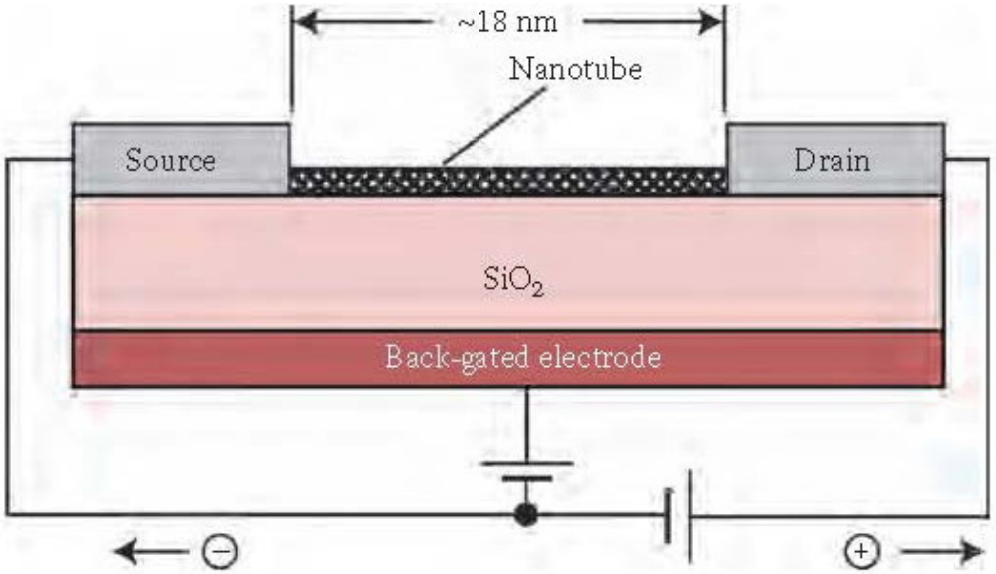

Figure 7.21 Electrical diagram of carbon nanotube semiconductor in back-gated transistor design. Negative charge is an injection of electrons into the nanotube. Positive charge is an injection of holes.

(2) Cantilever nanotubes: fixed at one end and freely suspended at the other end.
*The free end enables to flex up and down, similar to the cantilever probe in an AFM.

- When a positive voltage is applied to the gate, the negatively charged nanotube is attracted to it, and the nanotube is deflected downward toward the drain -> 'conductive' state
*When the nanotube contacts with the drain electrode, there are 'sticky' atomic forces (weak electrostaic and dipole-dipole forces) that hold the nanotubes together.

- In order to 'unstick' the nanotube from the drain ('nonconductive' state), a reverse bias (voltage) must be applied.

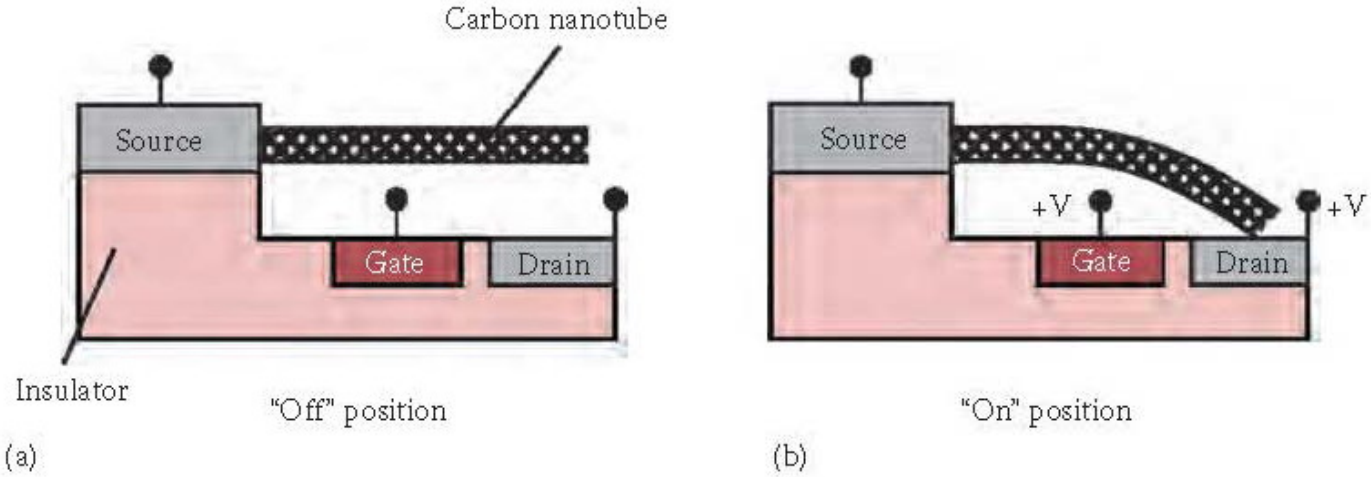

Figure 7.22 Illustration of (a) cantilever-supported nanotube in a nonconductive state, and (b) deflected beam making contact with the drain in a conductive state. [Adapted from Bichoutshaia, E. et al., *Mater. Today*, 11(6), 36, June

(3) Fixed-end nanotubes: supported at both ends between the source and the drain.

- The semiconducting nanotube (in the 'zigzag' or 'chiral' orientation) is flexed downward by a positive voltage.
  *When the nanotube contacts with the gate, the nanotube switches to the conductive state.

- A reverse bias must be applied to the gate in order to release the nanotube and switch it back to a nonconductive state.

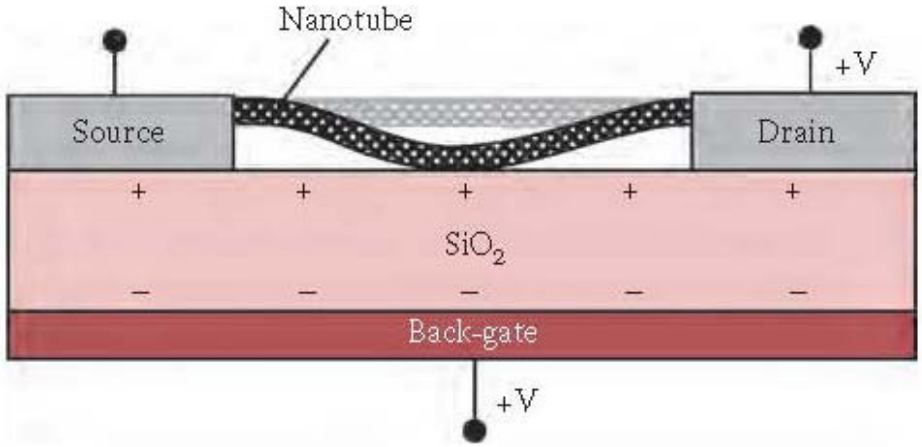

Figure 7.23 Illustration of fixed-end nanotube that is supported at both ends between the source and drain. The nonconductive state is shown in gray (left). The conductive state is shown in black (right), where the nanotube flexes downward and contacts the gate. [Adapted from Bichoutshaia, E. et al., *Mater. Today*, 11(6), 36, June 2008.]

7.6.2 Crossbar Arrays

- A grid of connections between input wires and output wires at various points.
  *The memory cells are stored in the interlayer – providing a high density of memory cells.

- Nanowire crossbar arrays have been fabricated since the late-1990s.
  *They are predicted to store ~ 50 Gbits/cm^2 (about 5x more memory on a chip than the current transistors) and with less energy consumption: commercialization as early as 2013-2017.

- The interlayer is less than 50 nm thick and it insulates the top nanowires from the bottom ones.

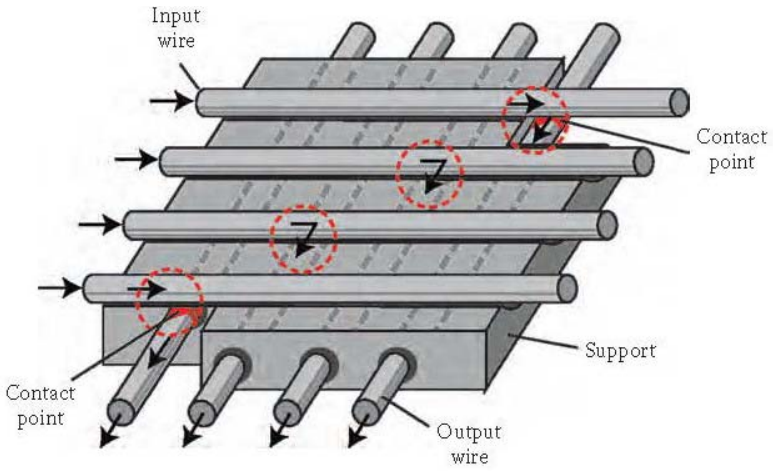

Figure 7.24 Diagram of crossbar switch showing input and output wires with multiple contacts that are shown in red. The contacts make connections between the input and output wires. The interlayer acts as a support and insulator. Arrows indicate the direction of electron flow (e-flow).

- The interlayer can consist of many different materials – oxide semiconductors, ferromagnetic materials, organic molecules.

- The interlayer acts as both a switch and a memory cell – just like the transistor that acts as a switch and a capacitor that acts as the memory cell.

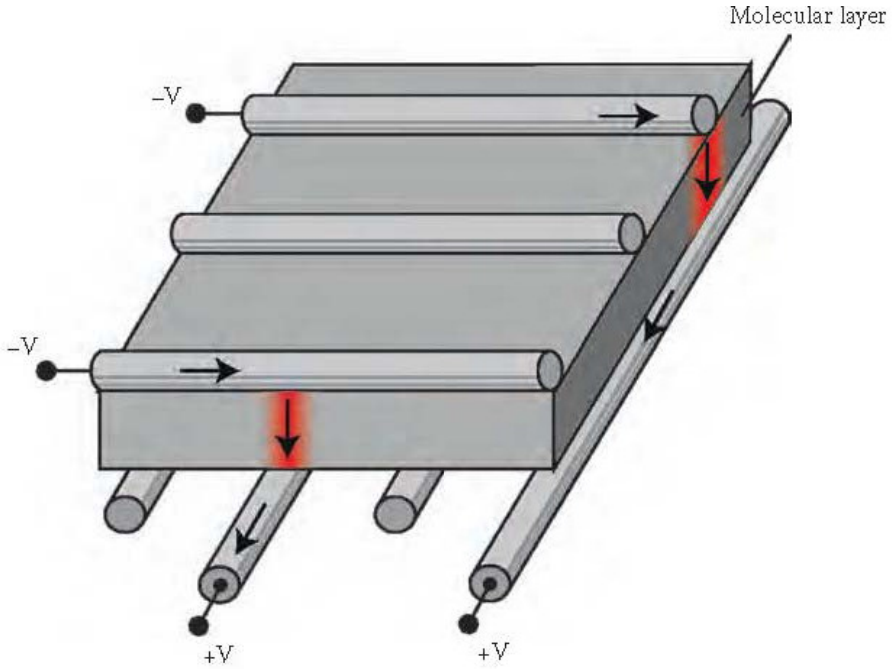

Figure 7.25 Illustration of molecular layer that insulates the nanowire grid. The molecular layer acts as both a memory cell and switch for bit processing. The red areas show the molecular layer is in the conductive state that switches "on," which records a "1" bit. In the nonconductive state the memory cell stores a "0" bit. The arrows indicate the direction of electron flow.

7.6.3 Magnetoresistive Memory (MRAM)

- MRAN on a chip grid of connections is a recent development since the early 2000s.
  * ~30x faster than electrical storage in capacitors and less electrical power.

- Two input lines and two output lines: at the intersection of the lines (wires), there are two ferromagnetic layers that store and replace bits. The ferromagnetic layers are separated by a nonmagnetic spacer.

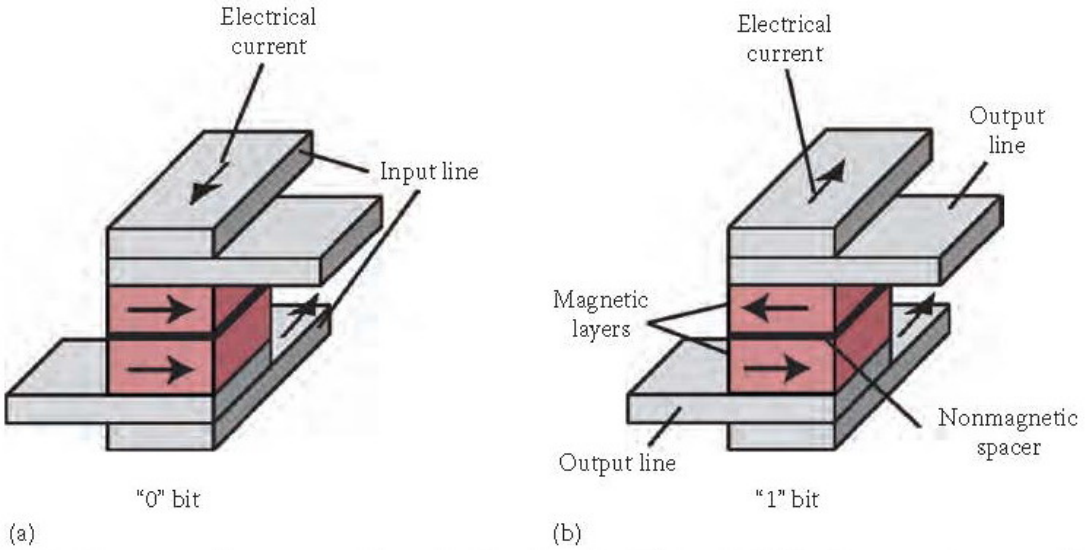

Figure 7.26 Illustration of ferromagnetic layers (red) storing (a) a "0" bit and (b) "1" bit in magnetic memory. Polarity of the magnetic layers is determined by the direction of the electrical current in the input lines. The output lines read the magnetic polarity and convert it into e-current in the output lines. [Adapted from Koch, R., *Sci. Am.*, 293(2), 57, August 2005.]

7.6.4 Phase Change Memory (PRAM)

- Memory is stored using a phase change in the material: flash memory in MP3 players, digital cameras, DVDs
  *Chalcogenide glasses: low T phase change between amorphous (glassy) and crystalline states
  *Group IV-VI elements: $Ge_2Sb_2Te_5$.

- The changes in the material properties can be induced by a pulsed laser: switched 'on' or 'off' by localized heating from a laser with short voltage pulses. The optical property change can be detected and read by a pulsed laser.

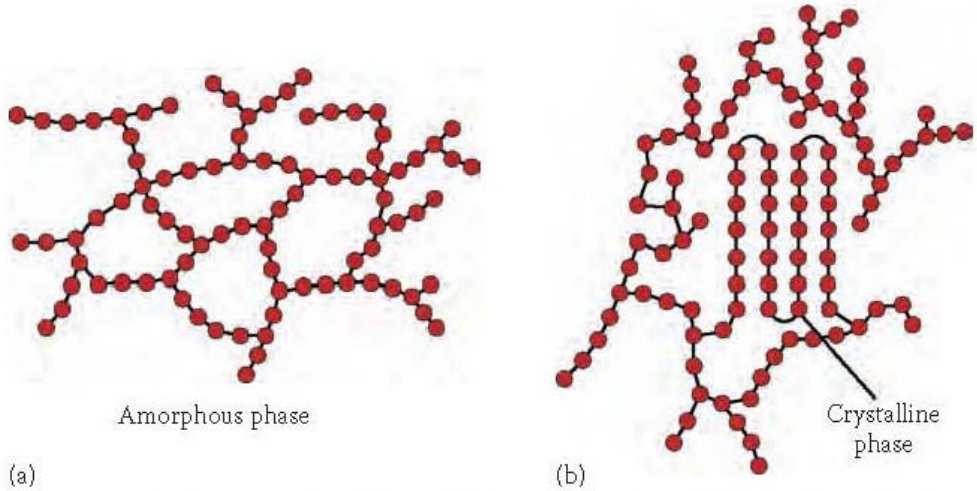

Figure 7.27 Illustration of (a) an amorphous phase and (b) crystalline phase. The amorphous phase has no structural order to its molecules. The crystalline phase has high structural order to its molecules. [Adapted from Kalpakjian, S.,

7.6.5 Quantum Bits (Qubits)

- Quantum bits are units of information that are processed by quantum computers (sometimes called spintronics = electron spin + electronics).
  *In the mid 1990s, Bell Lab demonstrated the feasibility of the quantum computers using qubits.

- The small size of qubits in atoms has potential of storing ~ 150 Tbits/in^2 (~ 23 Tbits/cm^2) of information: may not be commercialized till after 2025.

- Superpostion is a term in quantum mechanics that describes two states that coexist or coincide with each other.
  *Example: an atom that is both in an excited state and the ground state simultaneously – two energy states coexisting at the same time.
  *Electrons can coexist with states 'up' and 'down' ('1' and '0') at the same time.

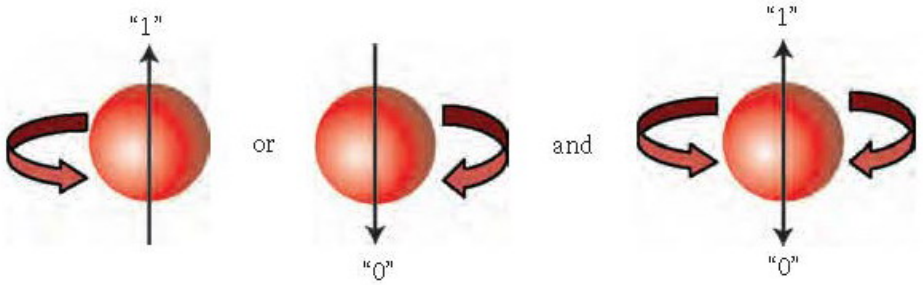

Figure 7.29 Illustration of a magnetic spin states: up ↑ ("1"), down ↓ ("0"), and both up and down ↑ ↓ ("1 and 0"), which is the superposition state.

- A 'qubit' can be represented by the uncertainty of both '1' and '0'.
  *Conversion of binary digits into decimal values:
  Decimal value of '111' in 3 bit sequence = [bit_3.20] + [bit_2.21] + [bit_3.22] = 7

- Each qubit represents both {0} and {1} at the same time (in the superposition state)
  *One bit can hold one decimal value (either 0 or 1); one qubit can hold two decimal values (both {0} and {1}).

TABLE 7.5 Three Bits (bit_1 bit_2 bit_3), Qubits, and Their Decimal Values

Bits	bit_1	bit_2	bit_3	Decimal Value
Bit sequence	0	0	0	0
	1	0	0	1
	0	1	0	2
	1	1	0	3
	0	0	1	4
	1	0	1	5
	0	1	1	6
	1	1	1	7
Qubits	{0}, {1}	{0}, {1}	{0}, {1}	0–7 simultaneously

[Homework/Reading Assignment]

1. Chen, R. et. al., Nanolasers grown on silicon, *Nature Photonics*, 5, 170 (2011).
2. Xiong, F. et. al., Low-power switching of phase-change materials, *Science*, 332, 568 (2011).