Chap. 7 Nanoelectronics

7.1 Introduction

- The electronic components are manufactured in the nanosize range (< 100 nm): Nano-miniaturization of electronics from top-down and bottom-up
- Biological research areas: DNA sequencing, genetic mutations, and diagnosing various genes and their potential diseases.

7.2 Computer Applications

- Random Access Memory (RAM)
- Volatile RAM
- Nonvolatile RAM
- Smaller, Faster, and Better

7.2.1 RAM

- During logic, computational, and decision-making functions, the bits (memory cells) are constantly being replaced by new bits, consisting of 1s (stored bits) and 0s (non-stored bits).

- The “R” in RAM means that any of the stored bits can be randomly accessed in any order regardless of their location in the memory cells.

7.2.2 Volatile RAM

- The current technology for storing and replacing bits in computer memory happens in two ways: either through volatile (dynamic RAM; DRAM) or non-volatile (static RAM; SRAM) storage.
- A typical DRAM contains a transistor and a capacitor: over 3 billion FETs in a computer.

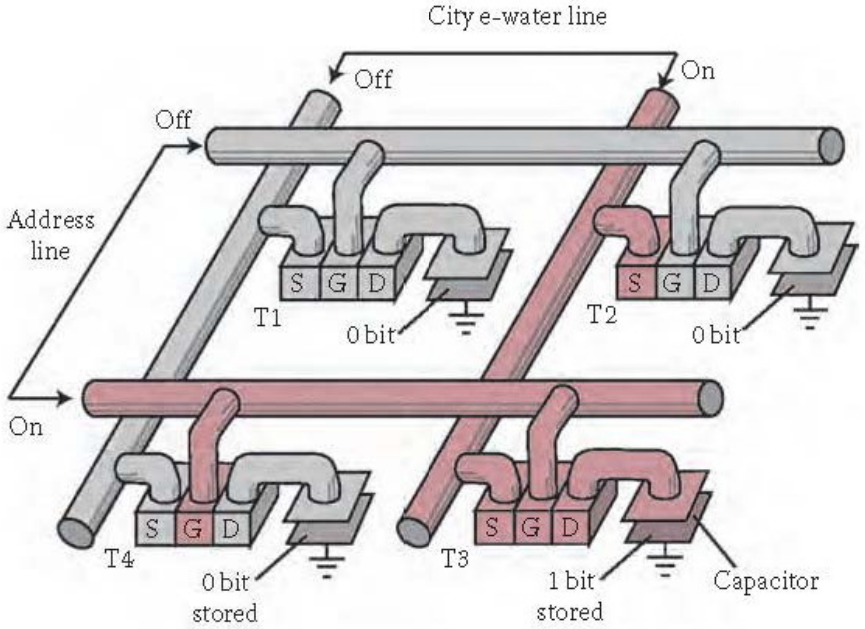


Figure 7.1 Illustration of four memory cells that includes transistors (T1, T2, T3, T4) and their capacitors that store electrical charge in the form of bits. Circular wires (lines) are connected to the source and gate of the transistors. Transistors T1, T2, and T4 are turned "off," which store 0 bits in the gray capacitors. Transistor T3 is turned "on," which stores 1 bit in the red colored capacitor. [Adapted from Macaulay, D., *The New Way Things Work*, Houghton Mifflin

- SRAM is slightly different from DRAM because it has extra backup circuits that periodically refresh the electric charge to retain the stored data.
  *Its most common use is in "cached" data travelling between a computer's CPU and RAM.

- The advantage of SRAM over DRAM: Its capacitors have to be refreshed less frequently, and its storage and replacement speed is much faster than DRAM.

- The disadvantage of SRAM: Its circuits are larger in size and thus have a lower density of memory cells.

TABLE 7.1 Performance Characteristics of Conventional Memory vs. Future Flash Memory

	Conventional Memory			Future Flash Memory		
Performance	**DRAM**	**SRAM**	**Flash**	**MRAM[a]**	**PRAM[b]**	**NRAM[c]**
Read/write speed	Medium	Fastest	Fast	Fast	Fast	Fast
Nonvolatile	No	Limited	Yes	Yes	Yes	Yes
Cell density	High	Low	Medium	Med-high	High	High
Miniaturization	Limited	Good	Limited	Good	Excellent	Excellent

[a] Magnetoresistive RAM.
[b] Phase-change RAM.
[c] Nanotube RAM.

7.2.3 Nonvolatile RAM

- It is also call flash memory or FRAM: memory cards, PDAs, laptops.

- Magnetoresistive RAM (MRAM), phase-change RAM (PRAM), nanotube RAM (NRAM).

7.2.4 Smaller, Faster, and Better

- Power of processing bits in chip technology: high speed, increased bit storage capacity
  1) Transistor size is directly proportional to the gate length (size): reduction of the gate size.
  2) Speed: increase of the bandwidth.

7.3 Lithographic Tools

- Design: The Plan
- Clean Rooms
- Photolithography: Patterning Technology
- Feature Resolution
- Photonics

7.3.1 Design

- International Technology Roadmap of Semiconductors (ITRS): forecast of the number of transistors on a chip and transistor size.

TABLE 7.2 Transistors on a Chip and Transistor Size vs. Time Roadmap[a]

Year	1995	1999	2001	2003	2005	2008	2011	2014	2016
Transistors per chip	12.0 M	23.8 M	47.6 M	95.2 M	190 M	539 M	1.5 G	4.3 G	—
Feature size (nm)	350	180	130	100	80	70	50	34	22

[a] 2001 International Technology Roadmap for Semiconductors (Ref. ITRS) as determined by the Semiconductor Industry Association (Ref. SIA).
M = Mega = 10^6; G = Giga = 10^9.

- Using the "top-down" photolithographic technology, the transistor size will reach a limit of ~ 16 nm [currently, ~8 nm].

7.3.2 Clean Rooms

- The air quality index: a particular matter (PM) of sizes < 2.5 um ($PM_{2.5}$) to be 134 ug/m^3 - particle mass per cubic meter of air.

*For a spherical particle of 2.5 um and density of 1.5 g/cm^3,
the mass concentration of 134 ug/m^3 in air --> a particle concentration of ~1.09x10^7 particles/m^3.

- The class of a clean room: class #1 (most clean) to class #1000 (least clean).

*Class #1: < 1 particle per cubic feet of air (< 36 particles/m^3 of air) for particles > 0.35 um.
*Class #1000: < 1000 particles/ft^3 of air (< 36,000 particles/m^3 of air).

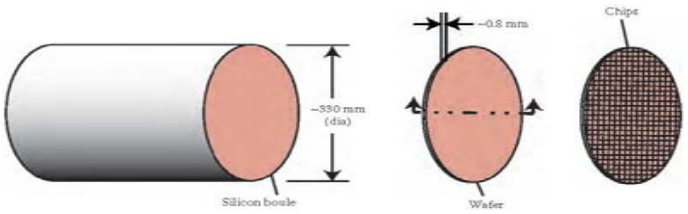
- In fabricating micro- and nana-devices, class #1 and #10 clean rooms are commonly used.

7.3.4 Photolithography

- Light is used to transfer a geometrical pattern through a mask onto a photosensitive emulsion that is called photoresist (or simply resist).

- Two types of photoresists : positive and negative
  (1) Positive photoresists are photosensitive polymers that break down when exposed to light, and the exposed patterns are dissolved in a solvent. The unexposed patterns remain insoluble to the solvent.
  (2) Negative resists are monomers that polymerize into hard coatings under exposure to light, and they are insoluble to chemical solvents.

- Wafers: thin layers that are sliced from a cylinder of a high purity single crystal (p-type Si), ~ 330-450 mm (or ~13-17.7 inch) in diameter



- Over 250 processing steps are needed to fabricate ICs on a single wafer.

- The photographic process is repeated hundreds of times with three types of processing : imaging, etching, and deposition.

*6 main fabrication steps (SORLED = semiconductor/oxide/resist/lithography/etching/deposition)

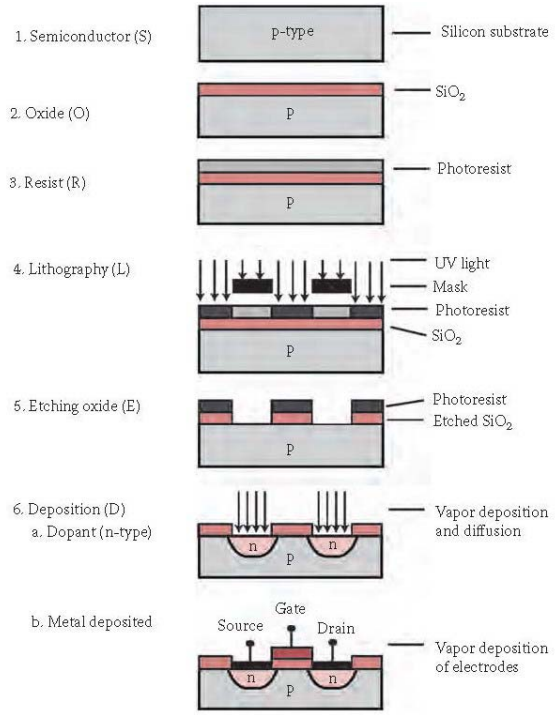


Figure 7.6 Six-step SORLED lithographic process for fabricating an FET, where S = semiconductor, O = oxide, R = resist (photoresist), L = lithography, E = etching, and D = deposition.

7.3.5 Feature Resolution

- Resolution is defined as the minimum separation between two features (distinguishable).

  light diffraction, wavelength of radiation, numerical aperture of medium, and radiation interaction with the photoresist.

  (1) Light diffraction: the spreading out or separation of light waves as they pass through a slit or grating <- constructive and destructive interference patterns between two travelling waves.

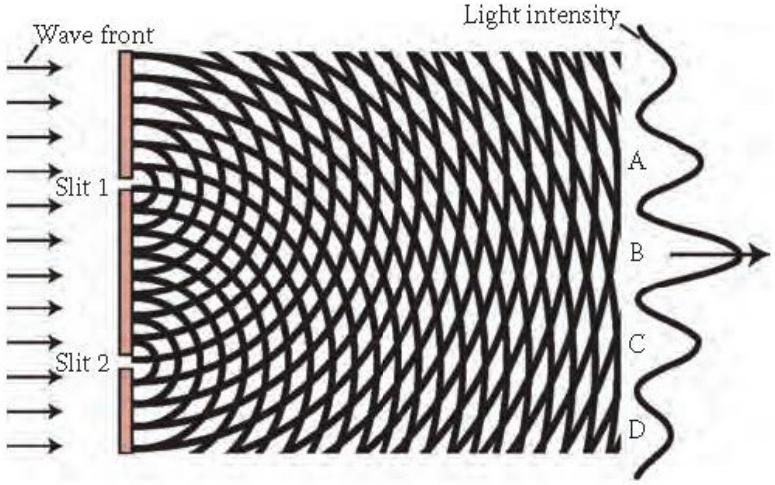


Figure 7.7 Diagram showing light wave front that interacts with itself as it passes through two slits to produce constructive interference at positions A, B, C, D (as shown by high light intensity). Destructive interference occurs where the light intensity is low. [Courtesy of Young Diffraction.]

Diffraction determines the resolution limit of a microscopic, photolithographic image, and pattern features on a chip -> the wavelength must be reduced below the desired resolution.

(2) Wavelength: shorter wavelength radiation is necessary to produce smaller features on a chip. Currently, in the UV range at about 193 nm, the feature size of ~45 nm on a chip.

(3) Numerical aperture: the feature resolution is inversely proportional to NA of a medium. For smaller size features, a lens with a larger NA is needed.

(4) Radiation interaction with photoresist: the generation of secondary photons and electrons limits the resolution of the photoresist.

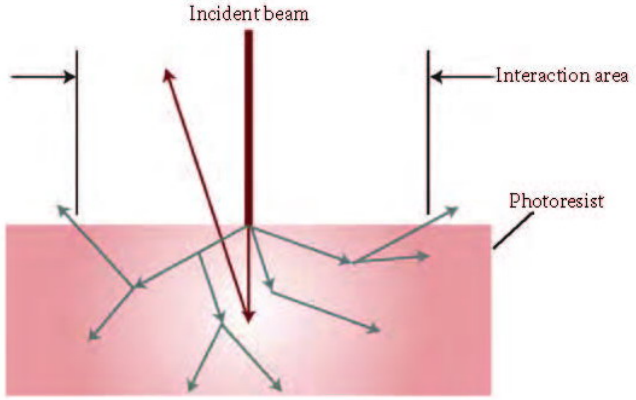


Figure 7.8 Illustration of incident beam colliding with the surface of photoresist. The incident beam creates a back-scattered beam (red arrow) that is reflected from the material and secondary electron scattering (gray arrows), where electrons exit the material and produce an interaction area.

7.3.5 Photonics

- Photonics is the application of light generation, emission, and transmission (from UV to IR).

(1) Pumped lasers
LASER (light amplification by stimulated emission of radiation): monochromatic (coherent).

(2) Laser diodes (injection laser diodes): image scanner, optical readers, telecommunications
Recombination of electrons and holes in the active region
Roughened end: confinement of photons
Polished (cleaved) end: escape of amplified radiation

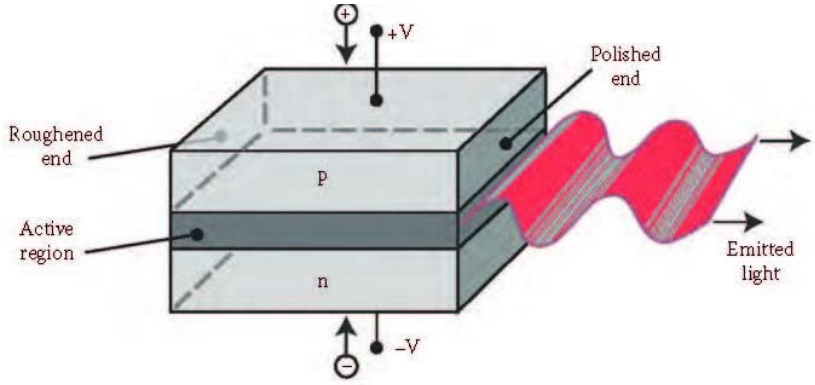


Figure 7.9 Illustration of a semiconductor laser diode that has a forward bias (+V and –V) across the p-type and n-type materials. Active region generates photons that are reflected back and forth across the polished and roughened surfaces. Finally, light is emitted through the polished end.

7.4 Recent Chip Development

- Hafnium-Based Insulator
- Strained Silicon
- Immersion Lithography
- Laser-on-a-Chip

7.4.1 Hafnium-Based Insulator

- For over 50 years, SiO_2 has been used as the insulator on a chip.
- In 2007, Intel announced to replace SiO_2 by a hafnium-based insulator to reduce the size of the transistor from 65 to 45 nm.

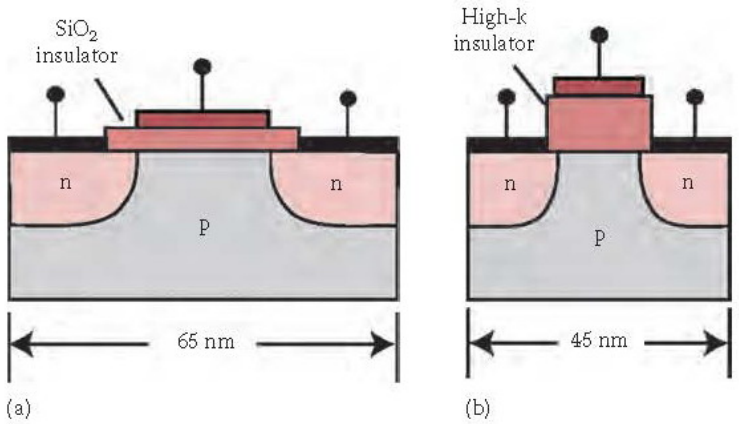


Figure 7.10 Illustration of 65 nm transistor with SiO_2 insulator (a) and 45 nm transistor with Hf-based high-k insulator (b).

- An insulator works as a “capacitor”: its capacitance is proportional to the dielectric constant but inversely proportional to the layer thickness.
  *A high-*k* insulator has high capacity to hold charges but has a slow switching speed.

TABLE 7.3 Estimated Dielectric Constant (k), Thickness of SiO_2, HfO_2, and $HfSiO_{4-x}N_x$, and Transistor Size

Insulator	Dielectric Constant (k)	Est. Insulator Thickness (nm)	Transistor Size (nm)
SiO_2	3.7[a]	~1.2	65
HfO_2	~25 (est.[b])	~3	45
$HfSiO_{4-x}N_x$[c]	~18 (est.[b])	~3	45

[a] Dielectric constants of materials, http://clippercontrols.com/info/dielectric_constants.html
[b] Estimated values.
[c] Nitrided hafnium silicate (where N substitutes for O in hafnium silicate).

- Typical SiO_2 layers are ~1 nm (less than 5 molecules thick), so that they do not hold charges very well -> electrons can tunnel through the layer, which causes a power loss and resistive heating of the transistor due to the current leakage.

- Two high-*k* materials: hafnium oxide and nitrided-hafnium silicate

7.4.2 Strained Silicon

- Improvement of the speed of transmitting bits by either the reduction of the size of the transistor or the increase of the electron mobility.

- What is strained silicon? the distortions of the lattice arrangement of atoms

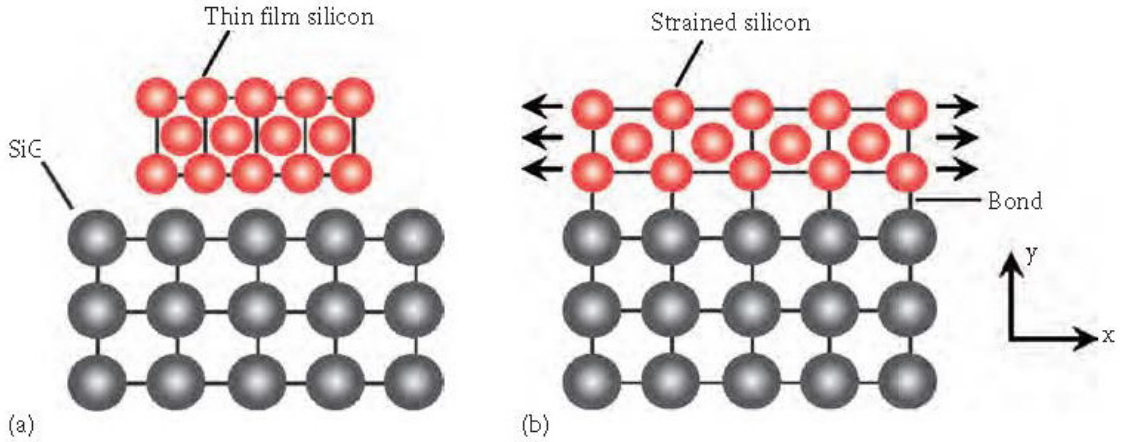


Figure 7.11 Cross-section illustration of (a) the individual atom arrangements of silicon (Si) unstrained and SiGe alloy. (b) Now the silicon thin film is vapor deposited as an n-channel on top of the SiGe alloy. The Si thin film is chemically bonded to SiGe, and the SiGe atoms stretch the Si atoms. As the Si atoms align with the SiGe atoms, the Si atoms become strained. Arrows indicate the Si thin film being stretched in tension.

- Application of the stress to the lattice: tensile (stretching) or compressive.

- On SiGe substrate (base material), Si lattice is forced to be stretched along the *x*-axis.

- When SiC (less lattice spacing than Si) is deposited at the source and drain, Si n-channel will be strained under a tensile stress.
- If Si_3N_4 (greater lattice spacing than Si) is deposited at the gate above as an insulator, n-channel will be strained under a tensile stress.

- When Si is strained or stretched, an electron can move faster through the strained Si lattice owing to fewer collisions with Si atoms.

7.4.3 Immersion Lithography

- Immersion lithography developed by IBM Almaden Research Center in 2006: ~ 32 nm size.
  *Performed in a 'wet' medium (water or oil) with a refractive index greater than air, placed between the lens and the wafer with a photoresist top layer.

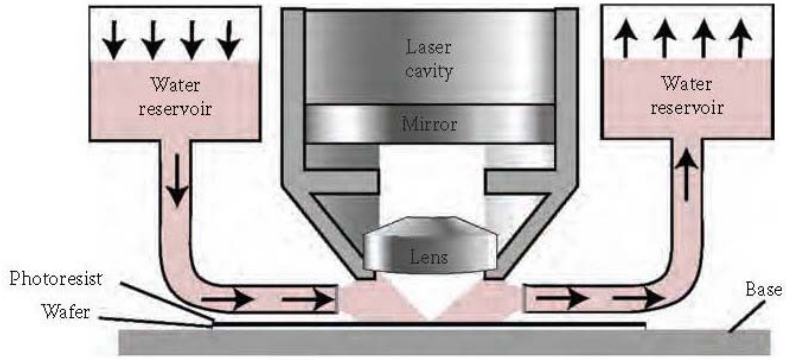


Figure 7.12 Water immersion lithography using argon-fluoride laser and lens to focus the radiation. Water is supplied by the left reservoir and recovered by the right reservoir. Water increases the refractive index of the medium over air, and the resolution is improved. [Adapted from Stix, G., *Sci. Am.*, 293(1), 64, July 2005.]

- Water is an ideal immersion fluid due to its high transparency, high purity, and low cost. It has a higher refractive index (1.44) for 193 nm UV light than that for aor (1.00).

- The line width was reduced from 90 to ~ 30 nm by using liquid immersion lithography. The feature size can be further reduced when higher refractive index oils are substituted for water as the medium.

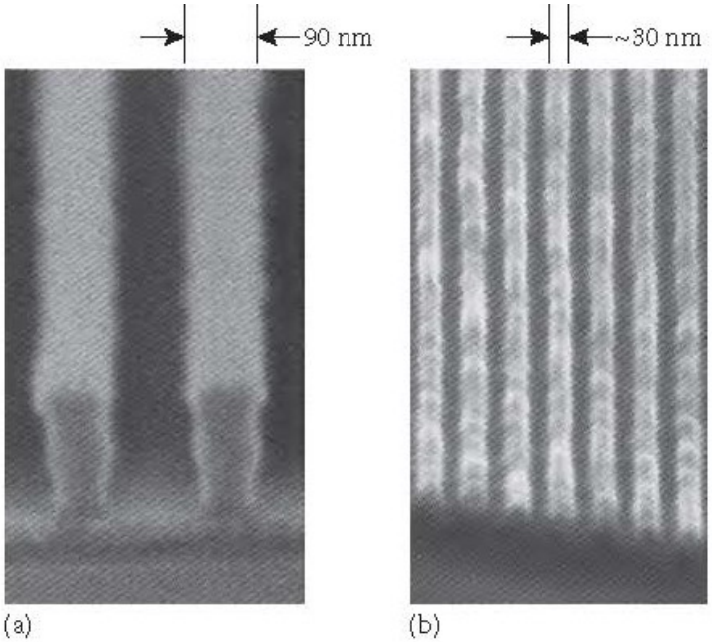


Figure 7.13 Micrographs of different feature sizes showing (a) line width of 90 nm using dry immersion (air) and (b) ~30 nm wide lines using liquid immersion. [Courtesy of IBM Research, San Jose, CA.]

7.4.4 Laser-on-a Chip

- Increase of the bandwidth by transmitting bits on a chip at the speed of light rather than by the electron conduction: high-definition digital video disc (DVD) players, computers, laser printers.

- Three components required: a laser diode, optical mirrors, and a waveguide.
  (a p-n laser diode, a silicon optical cavity, and a silicon waveguide (channel))
  *The band gap at the p-n junction is designed to emit infrared (IR) light (~ 1200 nm wavelength) that can be transmitted through silicon with little absorption (or energy loss).

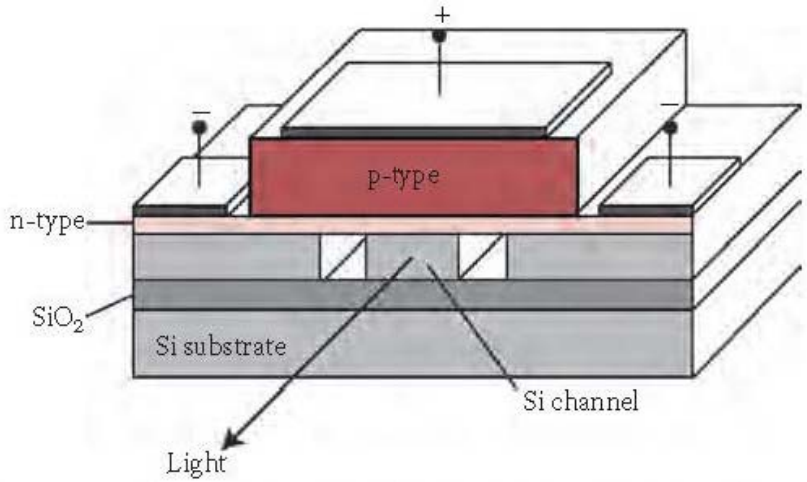


Figure 7.14 Cross section of hybrid laser diode with InGaAs (p-type) and InP (n-type) laser diode and silicon waveguide. A forward bias causes electrons and holes to recombine and emit infrared light into the silicon optical cavity. Then the light is transmitted through the silicon waveguide, as shown by the arrow.