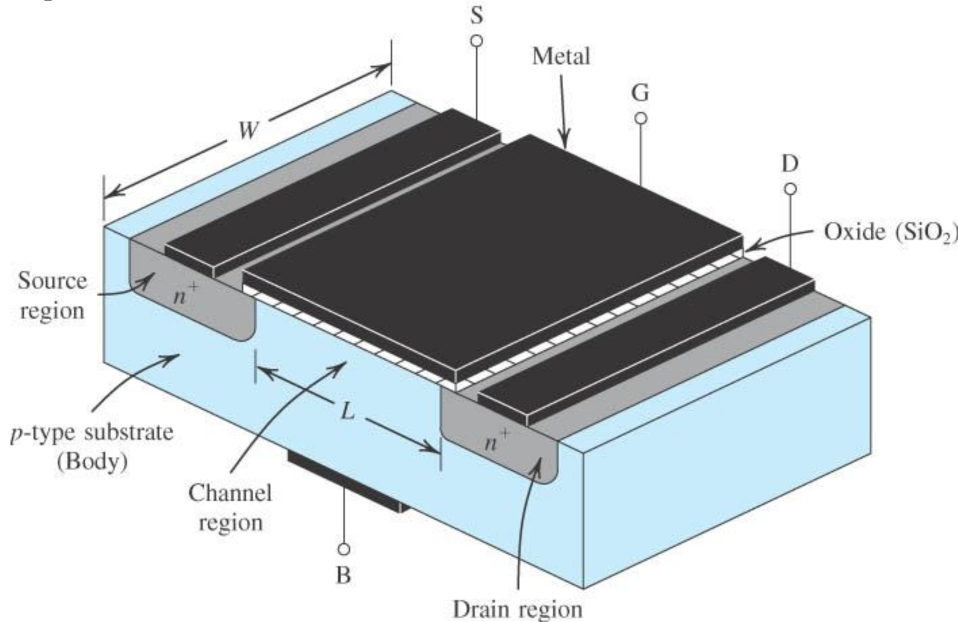
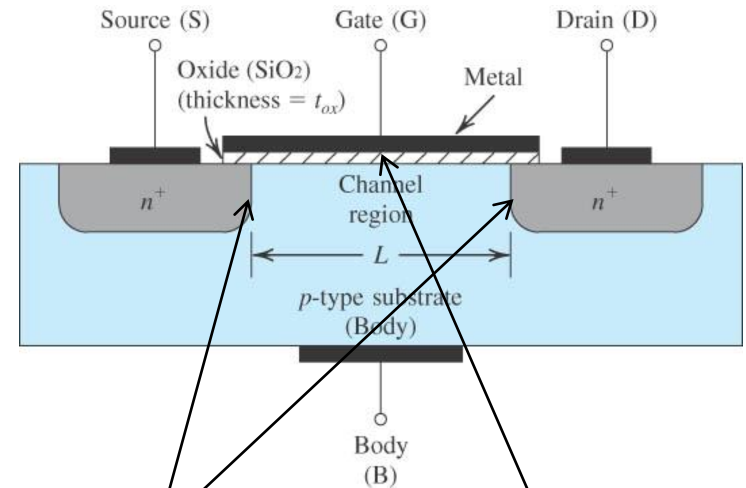
Field Effect Transistors

- **Two PN junctions** and **MOS capacitor** form a **MOSFET** (metal-oxide-semiconductor field effect transistor).





Two PN diodes

Capacitor

Transistors make DRAM, Flash Memory, Nonvolatile Memory, CMOS Microprocessor (AP), Other Digital Circuits

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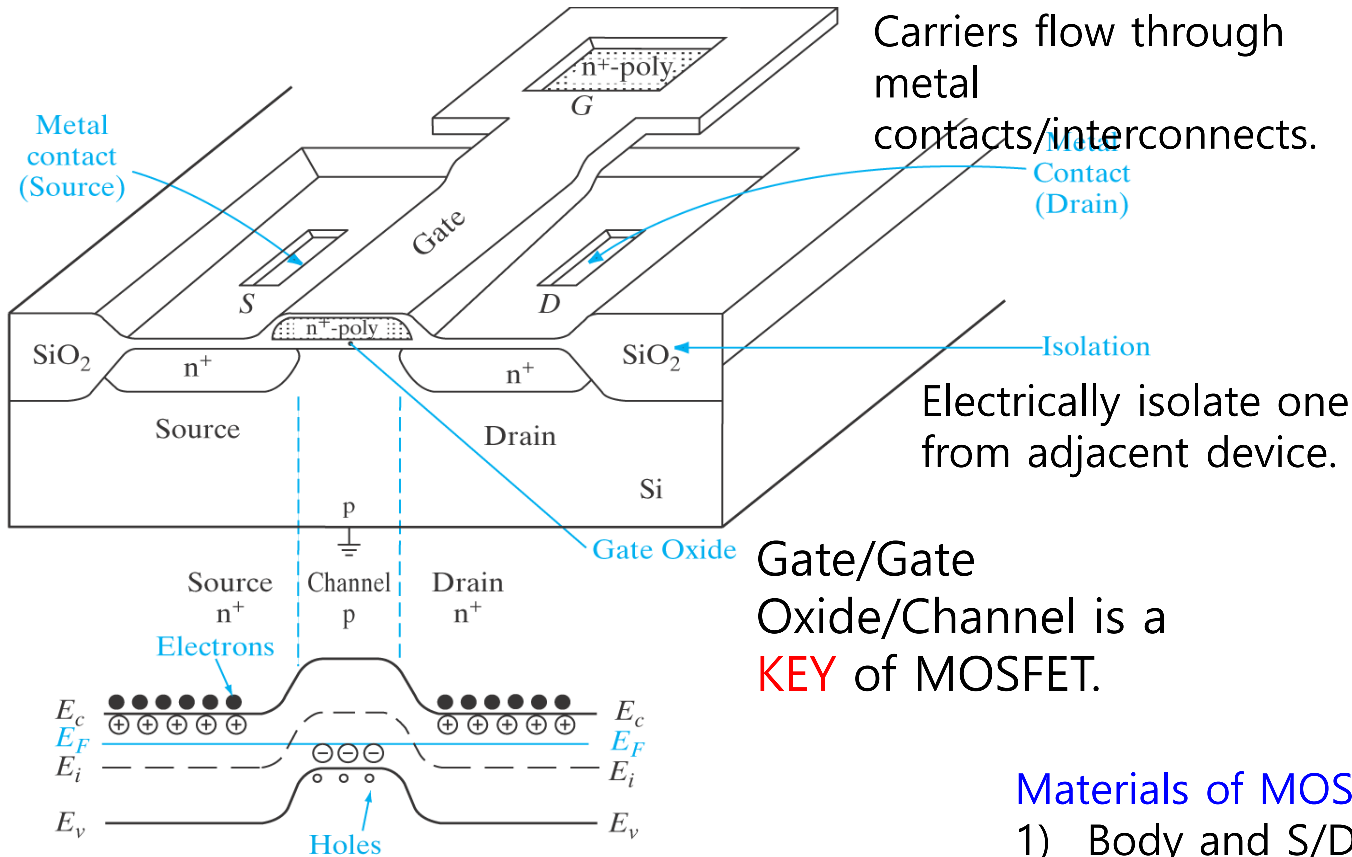
MOSFET Structure



Carriers flow through metal contacts/interconnects.

Electrically isolate one from adjacent device.

Gate/Gate Oxide/Channel is a KEY of MOSFET.

Materials of MOSFET (DRAM)

1) Body and S/D – silicon
2) Insulator, ILD/IMD – SiO_2, low k
3) Gate – Poly Si, metal
4) Gate dielectric – SiO_2, high k
5) Interconnection – Al/Cu
6) Via – W
7) Barrier – Silicide, others
8) Capacitor – Poly Si, high k

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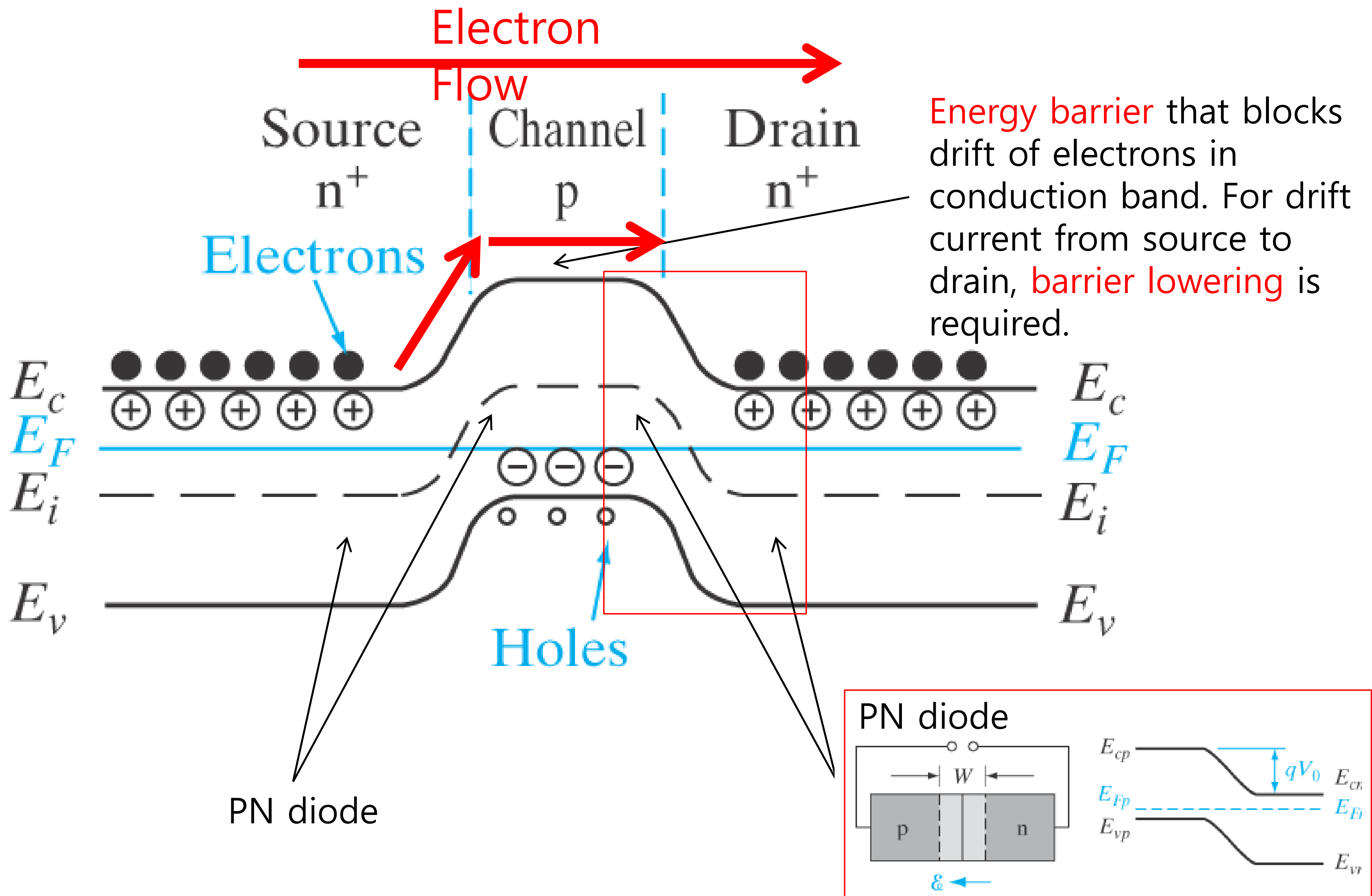
MOSFET Energy Band



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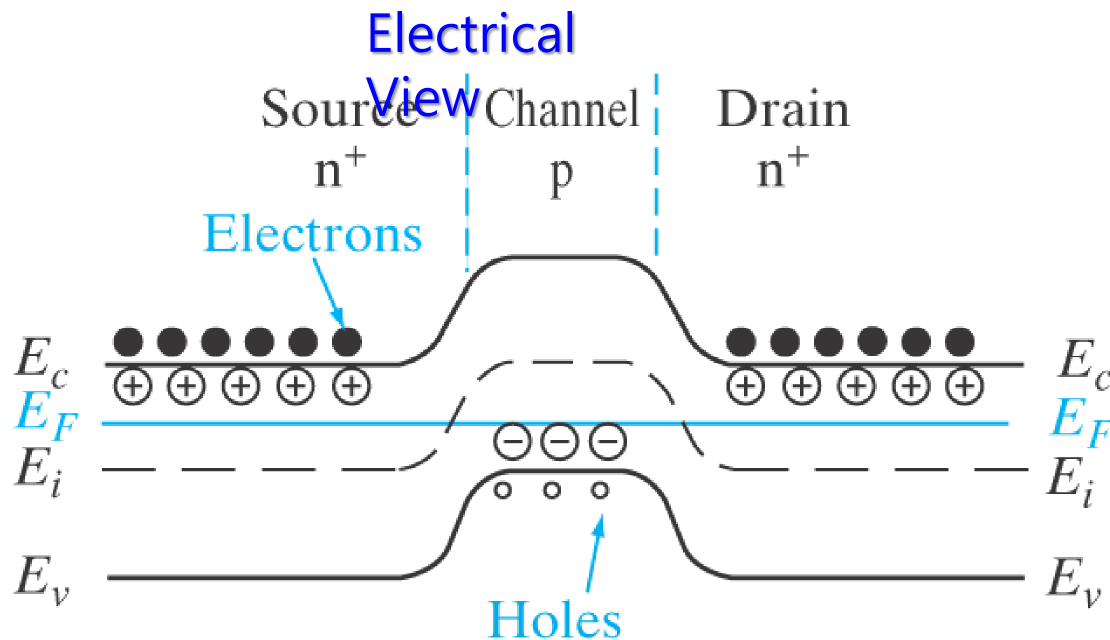
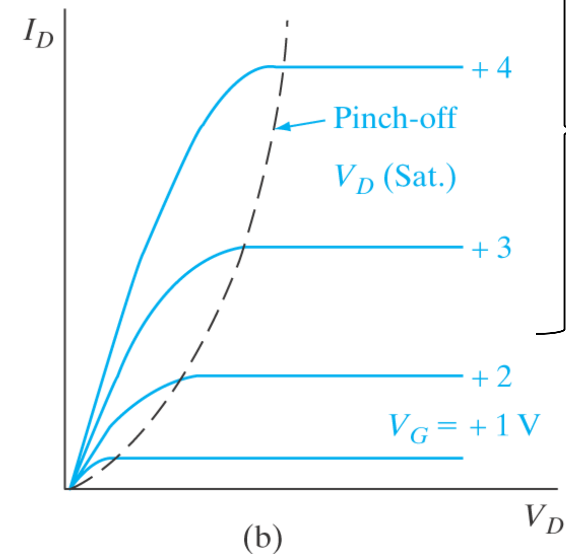
Channel

- Energy barrier lowering by applying the positive gate bias, which cause the accumulation of electrons near the semiconductor-insulator interface.
- With larger gate bias, more electron accumulation and more barrier lowering (lower resistance).
- By applying a small drain bias, current flows from the source to drain, when the gate bias is larger than the threshold voltage (V_T, minimum gate voltage required to induce the channel).





By inducing electrons near the interface , a conducting channel forms, which is a kind of gate-controlled resistor.

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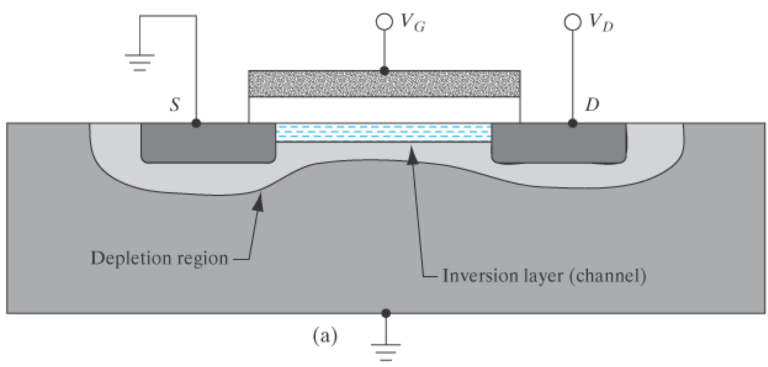
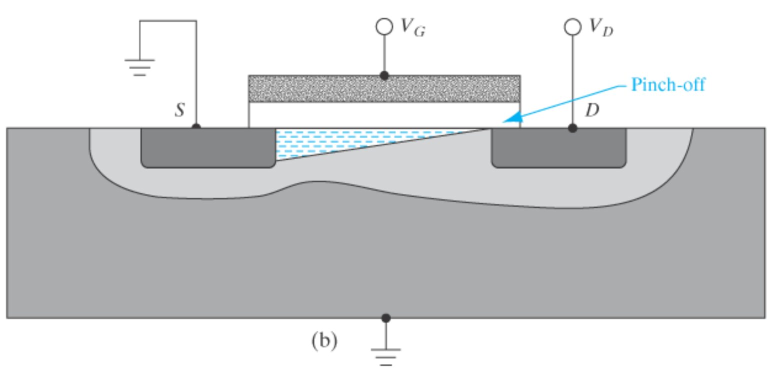
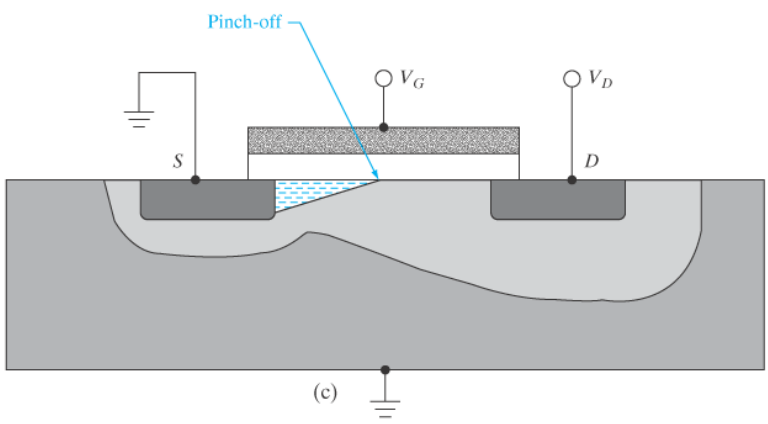
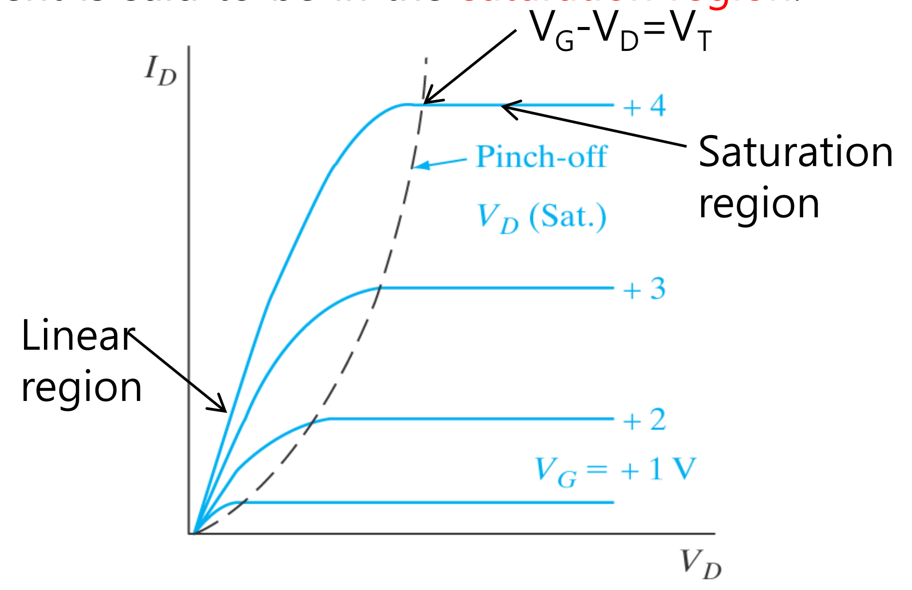
Pinch-Off







- While the conducting channel is formed by the positive gate bias (in the case of nmos, p type substrate), the drain current increases linearly with the drain bias (in linear regime, before pinch off).
- As more drain current flows in the channel by increasing V_D, there is more Ohmic voltage drop along the channel, starting from the source, V_G, to the drain, V_G-V_D. And when V_G-V_D=V_T, the channel (inversion layer) disappears and returns to depletion region (with electric field).
- From this point, the channel is pinched off and travels at the saturation drift velocity. The drain current is said to be in the saturation region.



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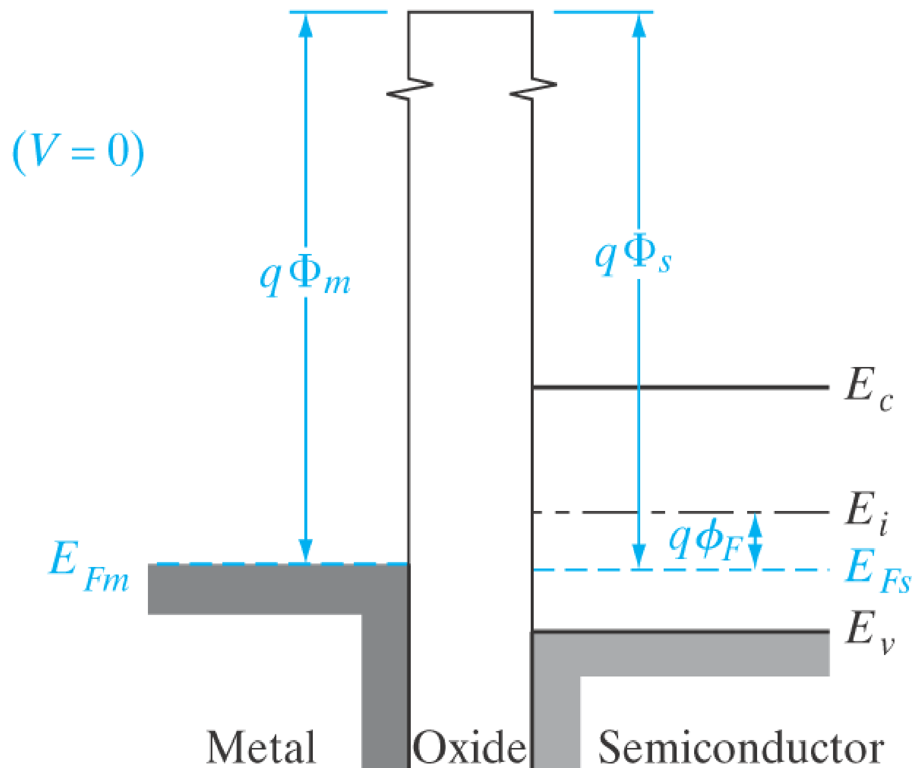
Band Structure of MOSCAP



1. Flat Band

Requirement of Gate dielectric (SiO_2)
i) Good interface
ii) Wide E_g insulator

- The work function is defined in terms of energy required to remove an electron from the Fermi level to outside of metal. But in MOS, a modified work function $q\Phi_m$ is used, which is the energy from the metal Fermi level to the conduction band of oxide. Similarly $q\Phi_s$ is the energy between the semiconductor Fermi level to the conduction band of oxide.
- In ideal (simplest) case, we assume that $\Phi_m=\Phi_s$.
- Another important quantity is $q\Phi_F$, which measures the position of Fermi level below the intrinsic level E_i of semiconductor. This quantity shows how strongly p-type the semiconductor is.
- The MOS(metal-oxide-semiconductor) structure on the left diagram is basically a capacitor. Therefore, if we apply a bias to metal side, the opposite charge is induced on the other side, semiconductor side.

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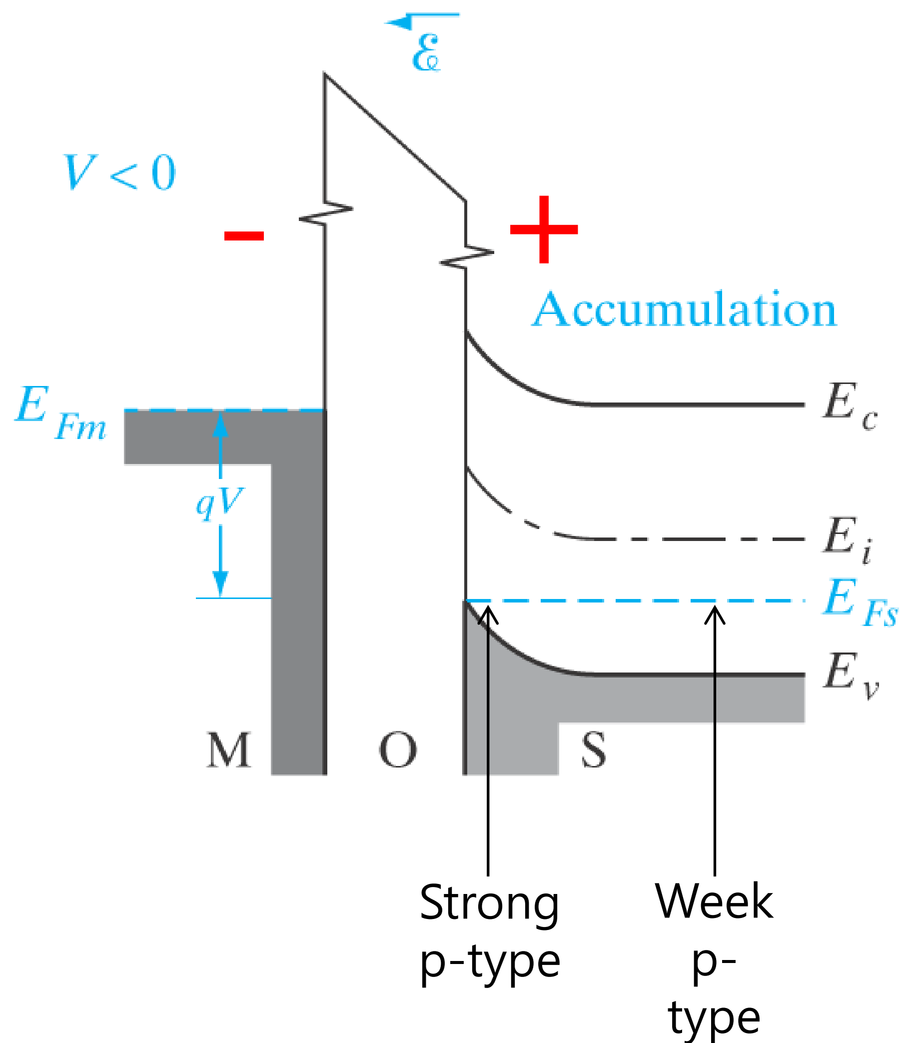

2. Accumulation

- If we apply the negative bias to the metal and the positive bias to the semiconductor, the electric field directs from semiconductor to metal. Electrons are deposited to the metal-insulator surface and equal amount of positive charges are accumulated to the insulator-semiconductor interface (hole accumulation).
- Since electrons are deposited to the metal surface, the electron energies are raised in the metal relative to the semiconductor, which increases E_{Fm} over E_{Fs} by qV (V is applied voltage).
- Since the modified work functions do not change, the band structure should be bent as shown in the left diagram. Also E_{Fs} does not change since no current flows from metal to semiconductor. Therefore, semiconductor near the insulator interface becomes more p-type due to accumulation.
- This makes energy barrier (in npn n type MOS structure) even higher (strong off).

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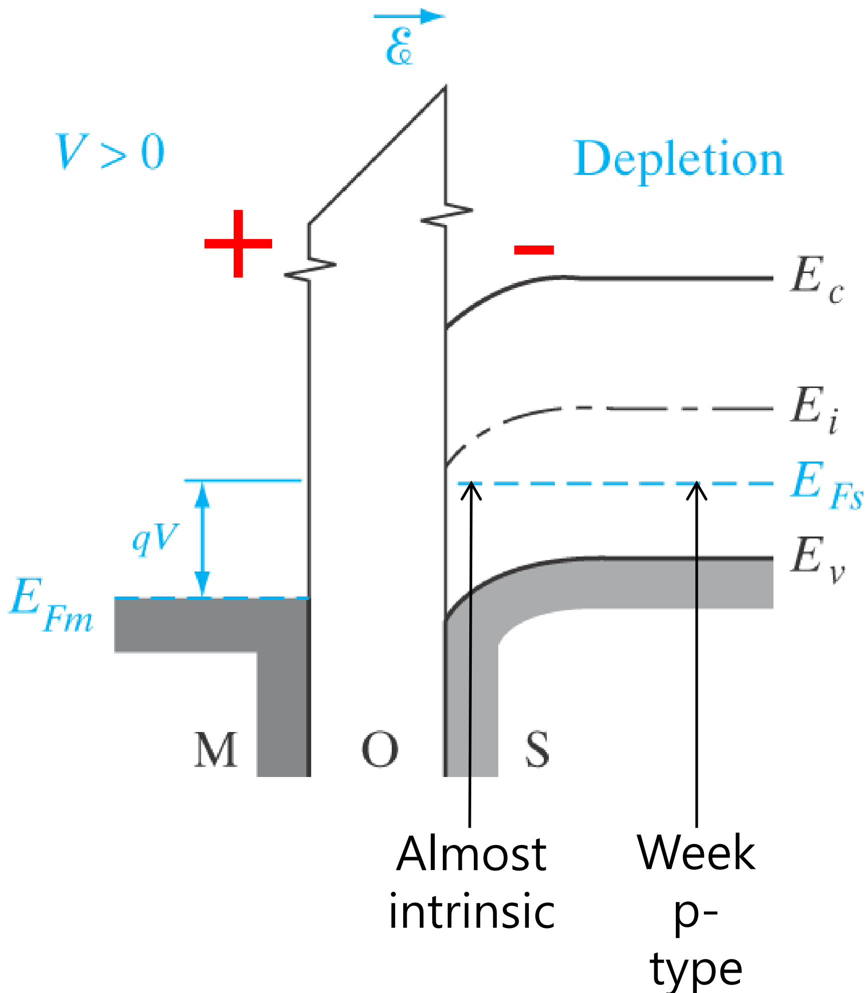

3. Depletion

- If we apply the positive bias to the metal and the negative bias to the semiconductor, the electric field directs from metal to semiconductor. Electrons are pulled out of the metal-insulator surface and equal amount of negative charges are accumulated to the insulator-semiconductor interface.
- Since electrons are removed from the metal surface, the electron energies are decreased in the metal relative to the semiconductor, which decreases E_{Fm} over E_{Fs} by qV (V is applied voltage).
- Since the modified work functions do not change, the band structure should be bent as shown in the left diagram. Also E_{Fs} does not change, since no current flows from metal to semiconductor. Therefore, semiconductor near the insulator interface becomes more intrinsic due to depletion.
- This makes energy barrier (in npn n type MOS structure) lower but channel is still not conducting (no carrier due to depletion, weak off).

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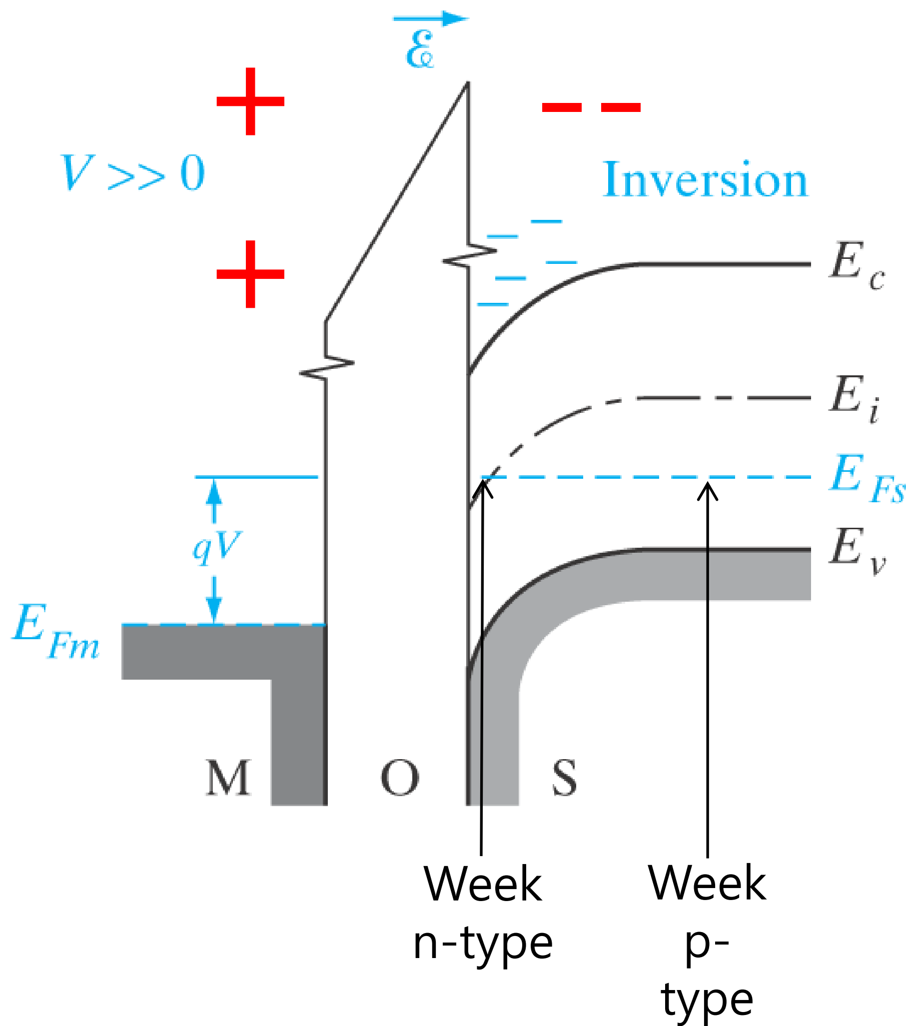

4. Inversion

- If we apply the more positive bias to the metal and the negative bias to the semiconductor, the stronger electric field directs from metal to semiconductor. More electrons are pulled out of the metal-insulator surface and equal amount of negative charges are accumulated to the insulator-semiconductor.
- Since electrons are removed from the metal surface, the electron energies are decreased in the metal relative to the semiconductor, which decreases E_{Fm} over E_{Fs} by qV (V is applied voltage). And if E_{Fs} is sufficiently larger than E_i, enough electrons exist near interface between semiconductor and insulator. This n-type surface is formed not by doping but by inversion.
- This inversion is a key factor of control of MOSFET operation (on and off).
- This inversion makes energy barrier (in npn band structure of n type MOS) low (on).
- Where do electrons come from? S/D

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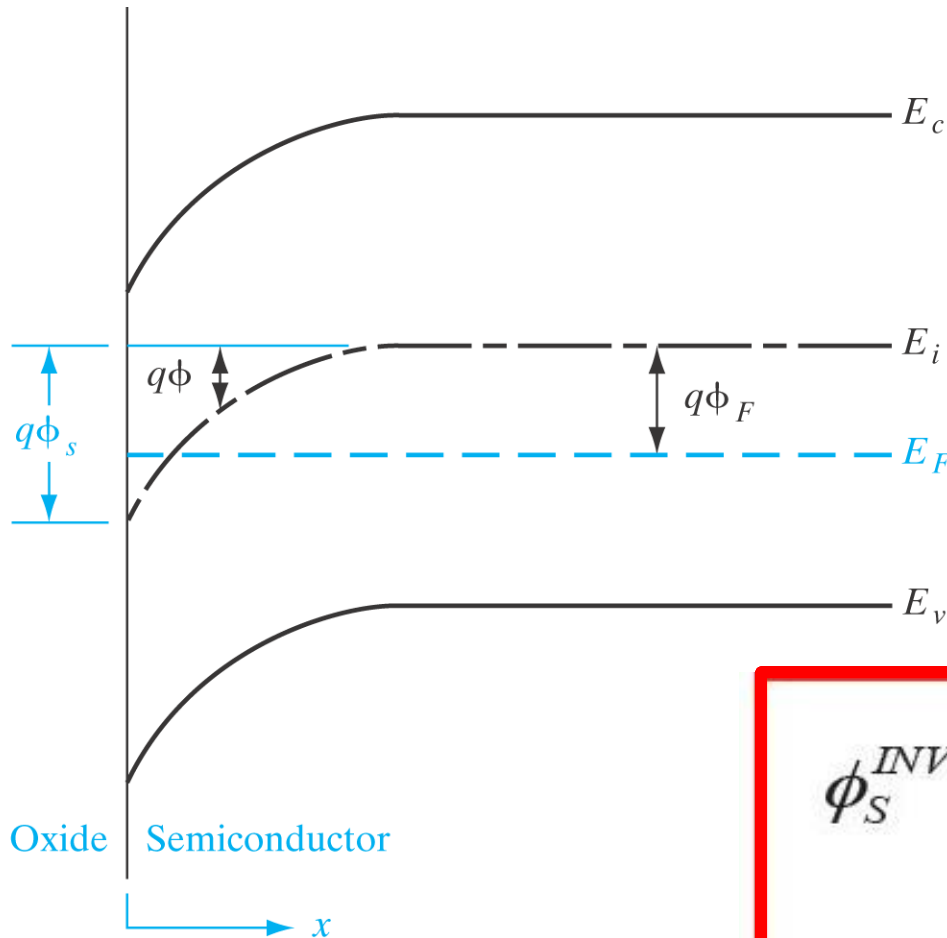
Required Bias for Turn-on



- The surface is inverted if ϕ_s is larger than ϕ_F.
- But the criterion for true n-type conducting channel (strong inversion) is $\phi_s = 2\phi_F$.

Relationship between N_A, N_D and n_i

$$\phi_S^{INV} = 2\phi_F = 2\frac{k_b T}{q}\ln\left(\frac{N_A}{n_i}\right)$$

$$\phi_S^{INV} = 2\phi_F = 2\frac{k_b T}{q}\ln\left(\frac{N_D}{n_i}\right)$$

As the higher channel doping is applied, the higher field is needed for the strong inversion.

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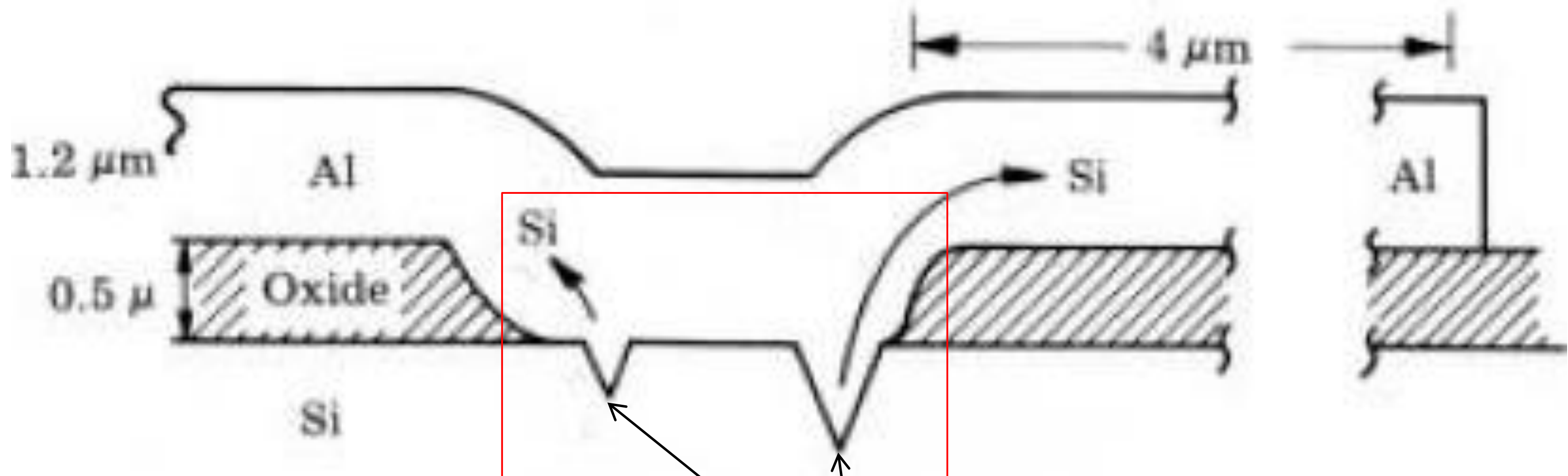
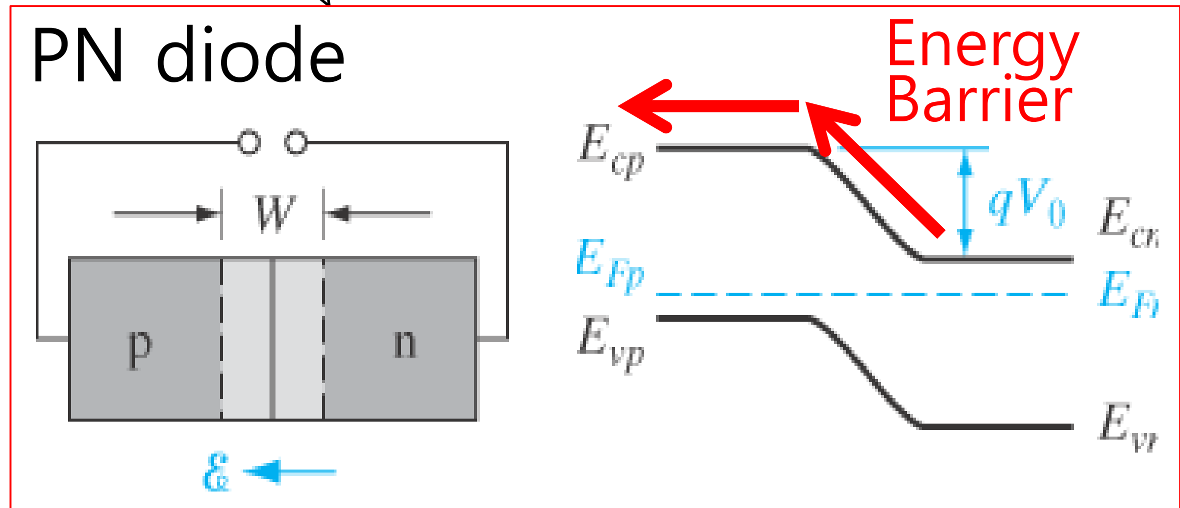
High Contact R Diode





Solution

(1) Al-Si Alloy
(2) Silicide (Barrier)

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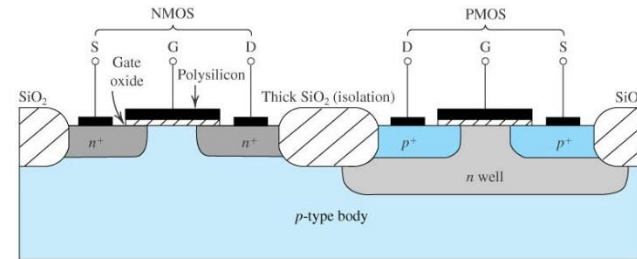
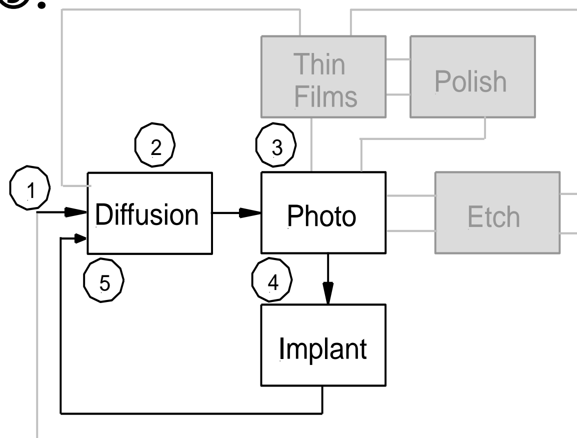
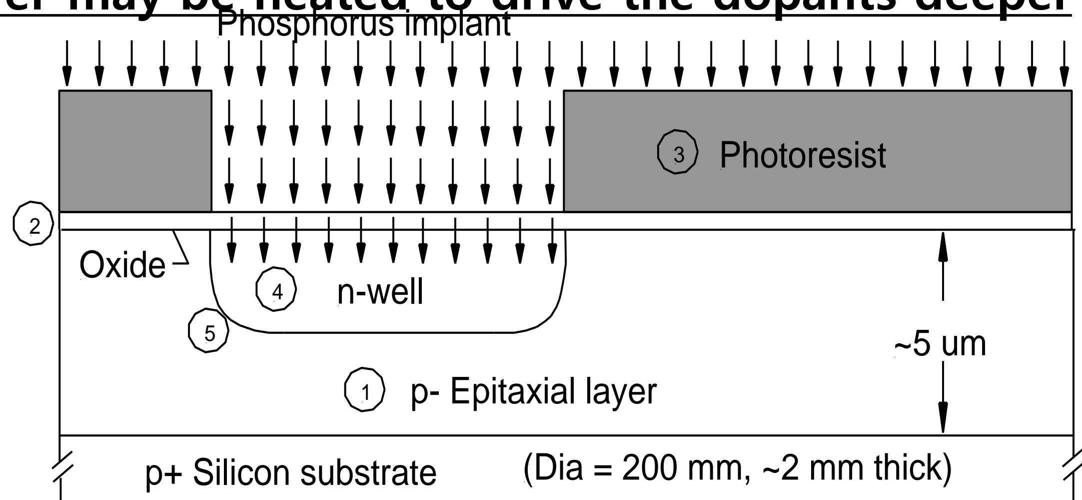
n-well Formation



- To make nmos and pmos in one substrate, we need electrically defined lightly doped regions, n well for pmos and p well for nmos.

- Photoresist ③ is used as a "mask" for the ion implantation ④. The ions do not have enough energy to penetrate through the photoresist and except for the holes in the photoresist, these implanted ions lodge in the photoresist. When this layer is removed (either by dissolving in acetone or using a plasma etcher) the implanted ions in the photoresist are removed also. After removal, the wafer may be heated to drive the dopants deeper ⑤.

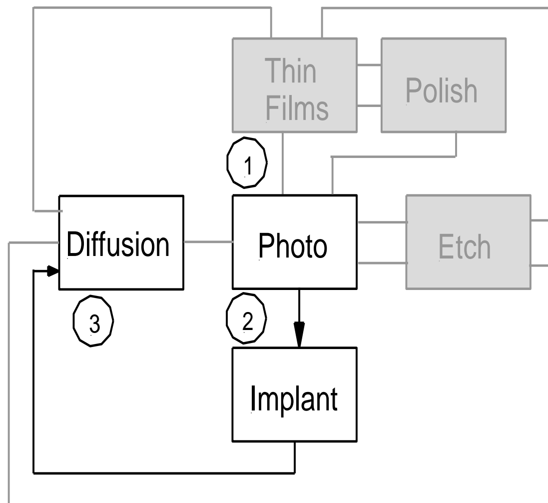


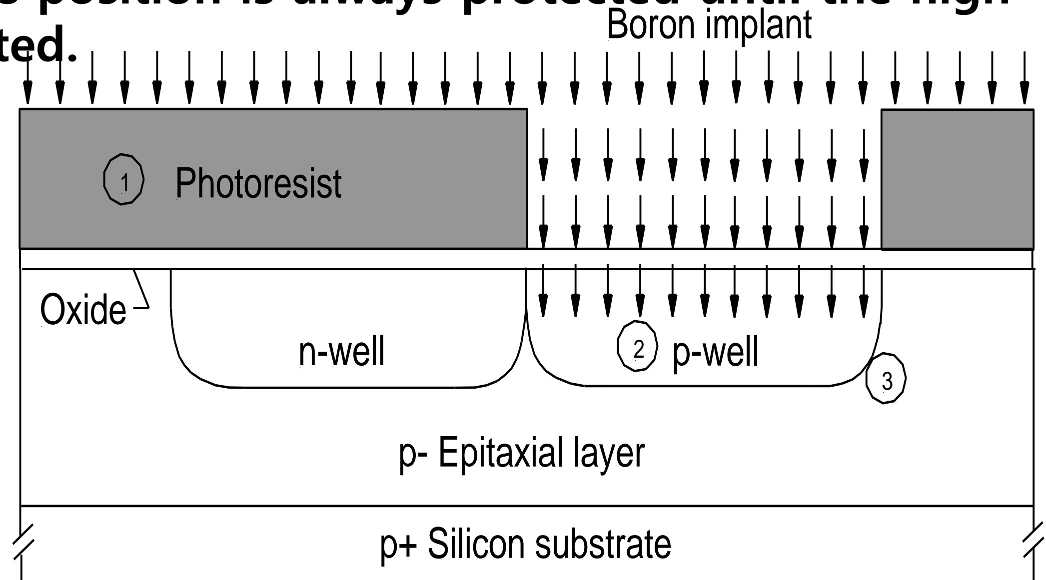


p-well Formation

- A new photoresist pattern ① is used for the p-well ion implantation mask.

- A thin layer of oxide is left over in the p-well during implantation. This is a <u>"sacrificial oxide", usually only 150A thick, which will be removed later to prevent contamination of the region which will hold the Gate Oxide</u>. The Gate Oxide must be totally defect-free to operate smoothly in an integrated circuit, so its position is always protected until the high quality Gate Oxide is deposited.





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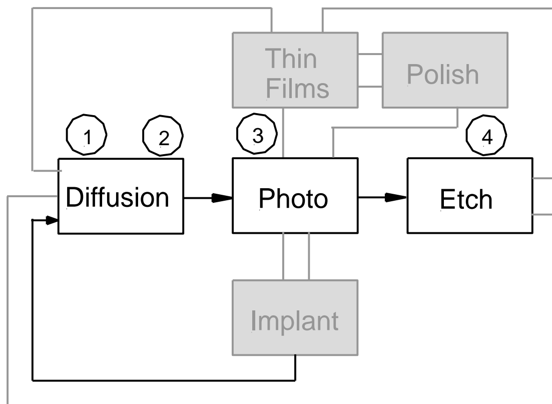
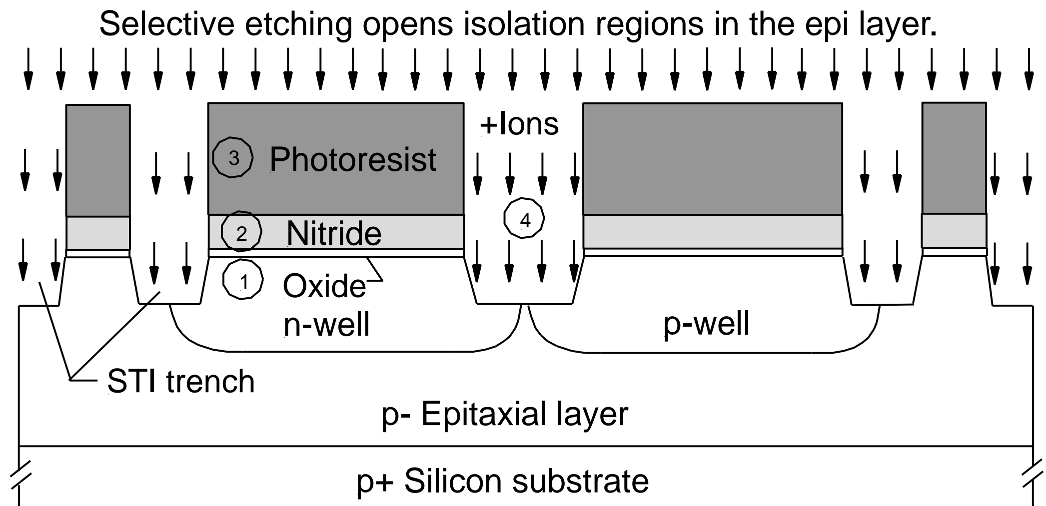
Trench Etch for STI (STI = Shallow Trench Isolation)

- First a thin layer of SiO2 ①, 150A, is laid down to protect the gate region, then a layer of Si_3N_4 ② (1500A) is deposited, possibly by LPCVD (low pressure CVD). Si_3N_4 is a high quality masking material in case the photoresist fails. The trench etching step (below) is energetic, and this Si_3N_4 layer protects the areas where the devices will be formed (active area).

- Photoresist is deposited and patterned ③ . Then plasma etching uses high intensity RF to ionize either fluorine or chlorine based gases. The F or Cl ions then react with the exposed Si_3N_4 and silicon, forming gaseous products which are removed using vacuum pumps (dry etching using RIE).





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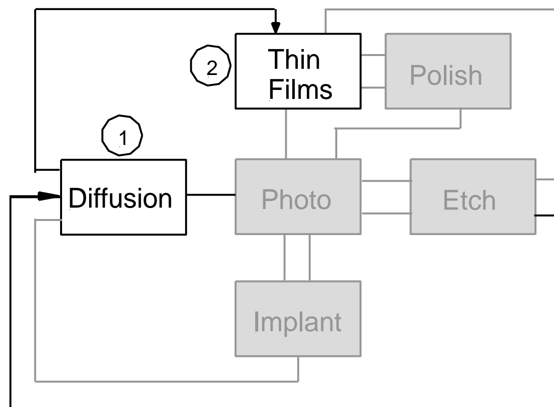
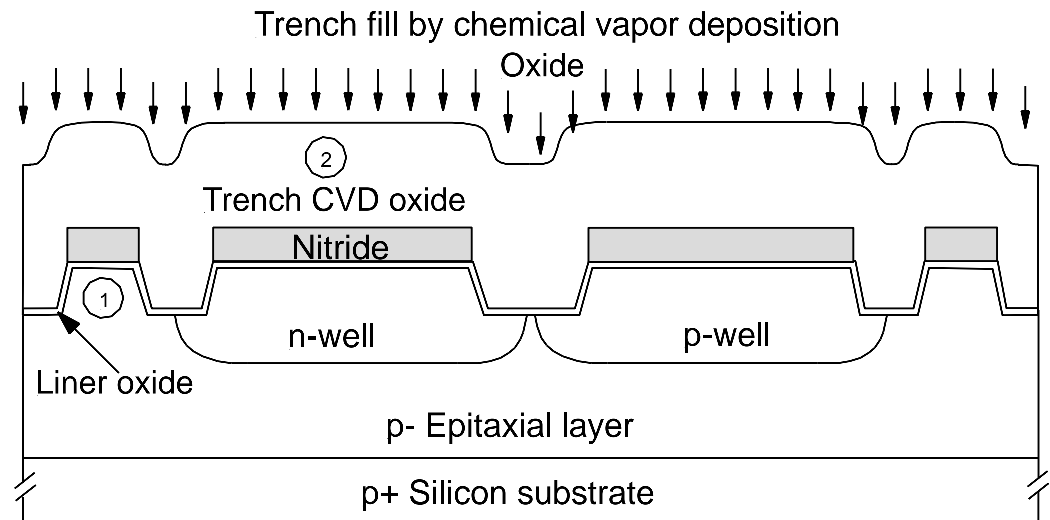
Oxide Fill for STI

- The isolation trench is exposed to oxygen at medium temperature (750°C) to grow a thin protective oxide, SiO_2, of about 150A thickness ① .

- Next a thick layer of CVD oxide, SiO_2, is deposited ② . This layer will act primarily as a fill to the isolation trenches (Field Oxide) to electrically isolate each devices.





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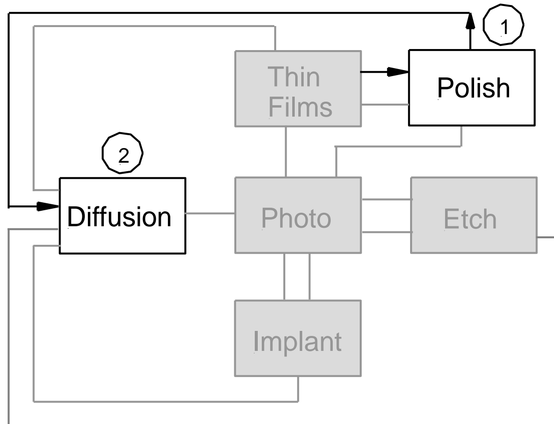
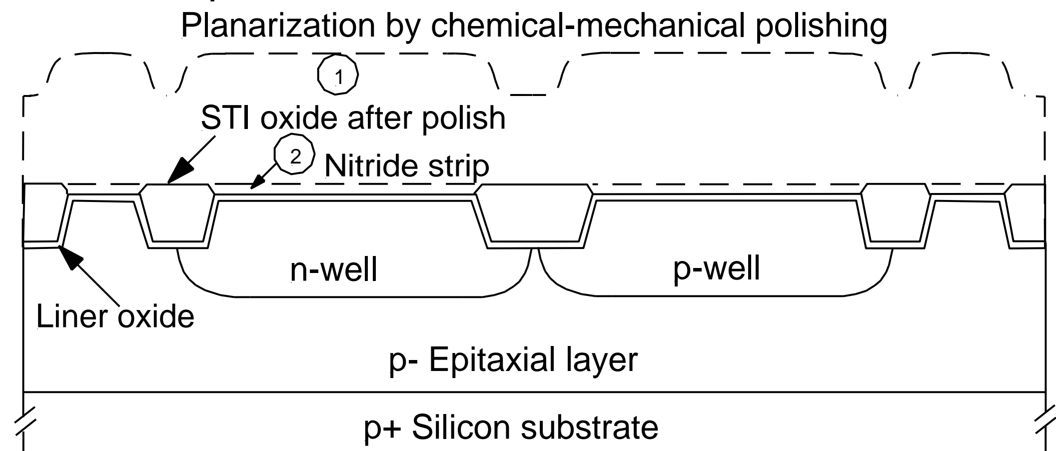
STI Formation

- The isolation is completed by polishing the coarse CVD oxide back to the wafer surface.

- This polishing is called CMP, Chemical Mechanical Planarization.

- A polishing pad rotates in contact with the wafer surface, with lubrication provided by a slurry containing nano-size polishing particulates and chemicals. The reactants are specially chosen to react preferentially with porous SiO_2. Hence the Si_3N_4 layer protects the region where the active devices will be formed and CMP stops when the CMP pad reaches the nitride film.





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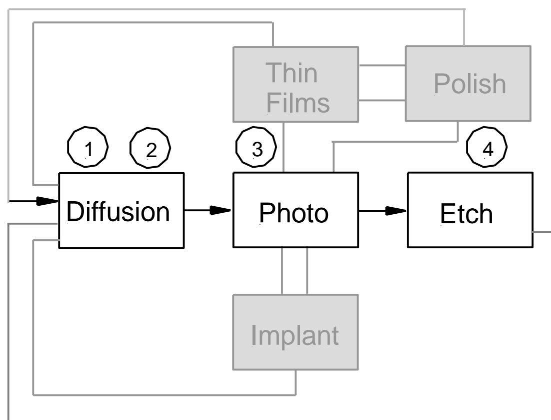
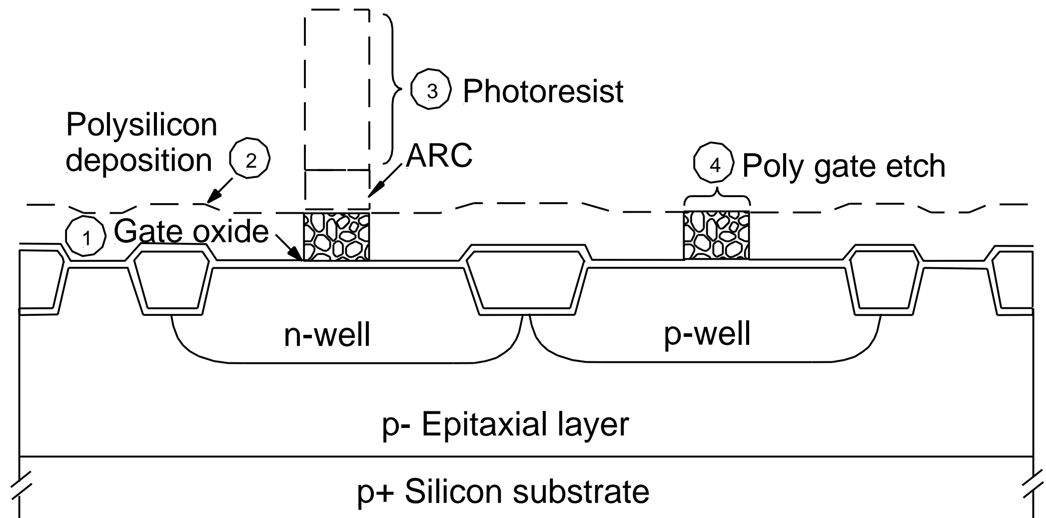
Poly Si Gate Structure Process

- Photoresist is applied, patterned and the Si_3N_4 is removed for the Gate Oxide processing. The wafer is then put into the oxide furnace and high temperature (1000°C) O_2 gas is introduced to grow about ~25A thick highest quality $SiO_2$①.

- Silicon is then deposited on the wafer using RF-CVD with silane (SiH_3). A plasma dissociates the silane, and the silicon atoms deposit on the surface. Since the temperature is modest (<500°C) the silicon forms in poly-crystalline grains.

- Finally, photoresist is again applied and the most critical patterning is done ③ . The Gate Width is the finest (thinnest) dimension which will be required. The polysilicon is then etched ④.





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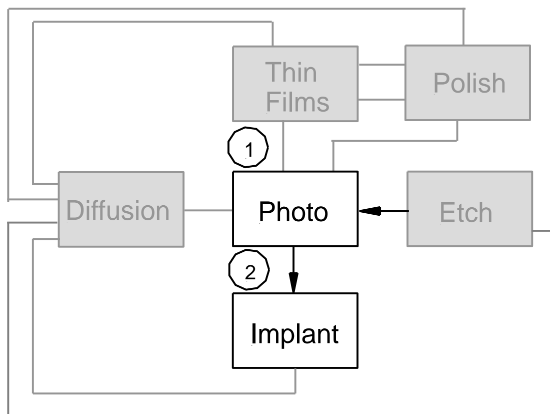
n⁻ LDD Implant (LDD = Lightly Doped Drain)

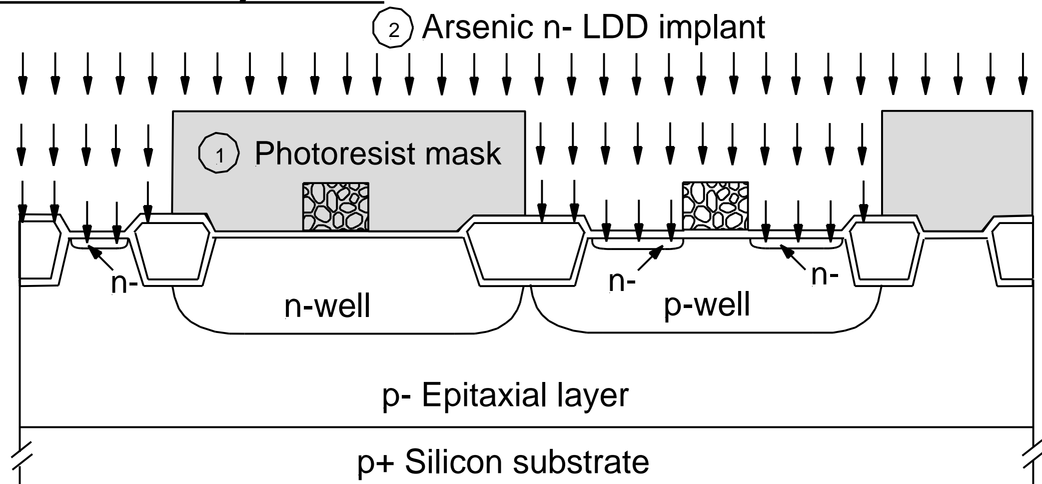
- The concept of Lightly Doped Drain is to prevent "punch-through".

- Since the gate is so narrow, the electric fields of the S/G and G/D junctions are so close that energetic electrons with high kinetic energy (hot carriers) might jump into the gate oxide and are trapped. By reducing the doping of the drain, the electric field decreases and hot carrier can be prevented.

- The disadvantage of LDD is the higher series resistance and lower drive current. In these days, LDD doping concentration is increased up to 10^{19} cm^{-3} by using low power supply voltage (VDD).

- Uses Self-Aligned Gate to form Source/Drain.





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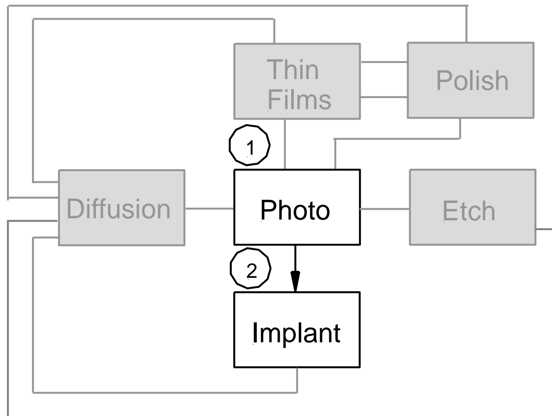
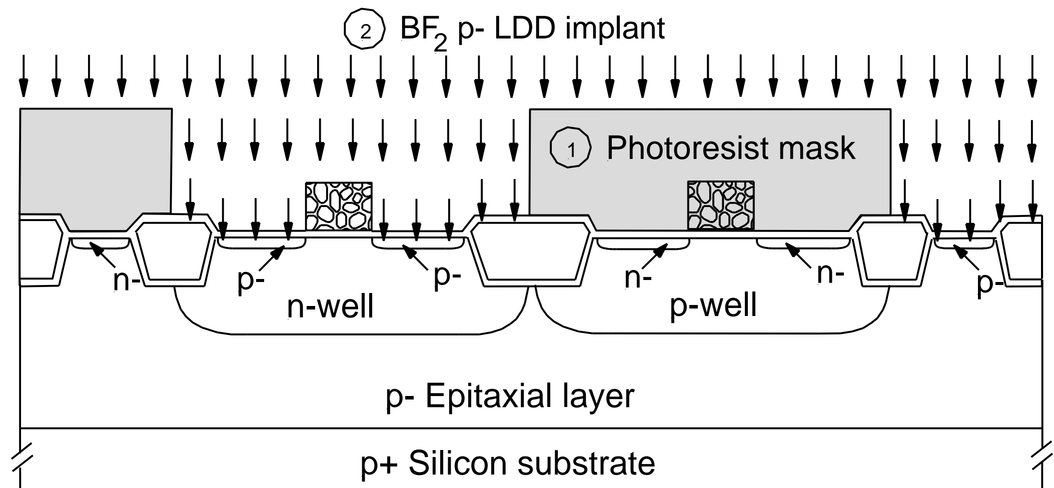
p^- LDD Implant (LDD = Lightly Doped Drain)

- Similarly to the previous step, photoresist is deposited and patterned, and then Molecular BF_2 is implanted for the lightly doped Source and Drain of the pMOS cell ②.

- Uses Self-Aligned Gate to form Source/Drain.





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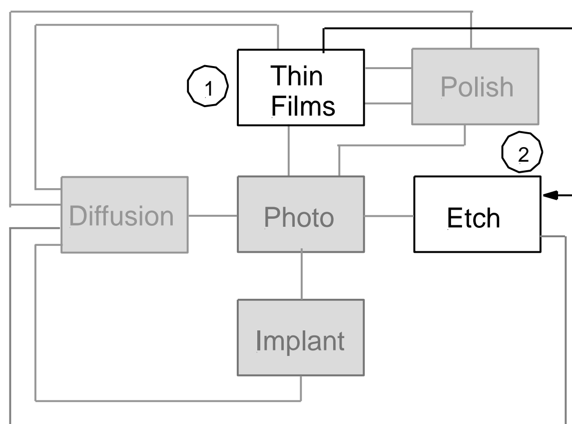
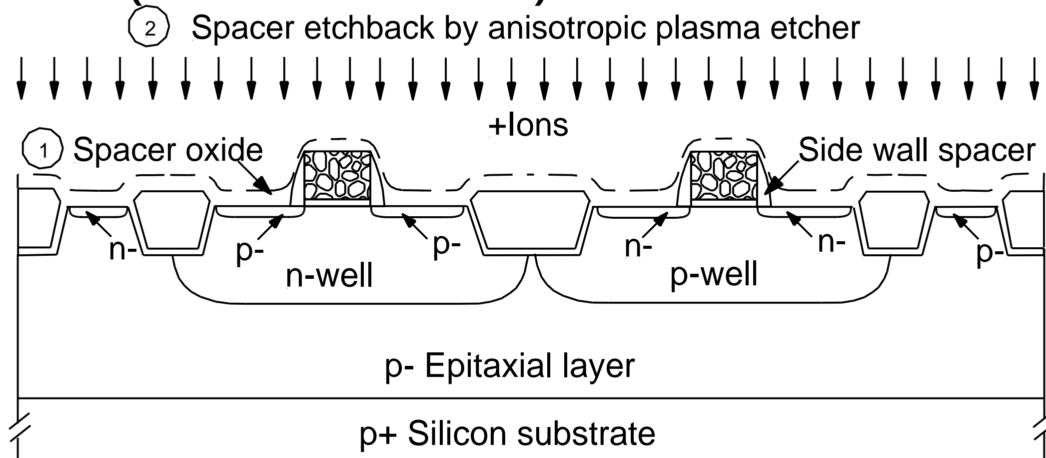
Side Wall Spacer Formation

- Polysilicon will be the electrical contact for the Gate. It must be electrically protected from the metallic contacts to the Source and Drain. So a thin "side-wall spacer oxide" is deposited on the side of the Gate to obtain electrical isolation. This Spacer will also keep the next implantation (S/D) away from the edge of the Gate.

- A thin SiO_2 layer ① (1000A) is deposited using CVD. Since the CVD is non-directional, the oxide will coat both horizontal and vertical surfaces equally.

- Without using photoresist, this oxide is immediately removed using a directional anisotropic etch ②. The etch will remove the flat (horizontal) oxide and leave the vertical SiO_2 on the sides of the Gate (No mask is needed).





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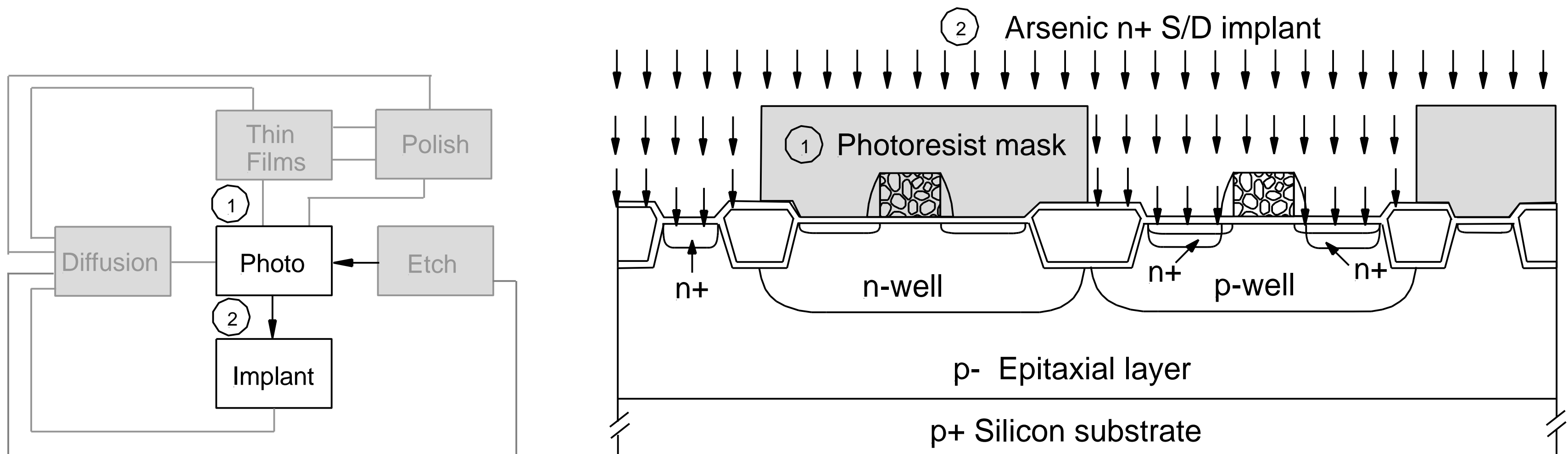
n^+ Source/Drain Implant

- A second implant ② is made into the Source and Drain.

- The S/D implant is slightly narrower than the previous S/D implant because the Gate now includes the "Gate Side-wall spacer" which was deposited in the previous step. Hence the Source and Drain will be lightly doped next to the Gate, reducing punch-through, and more heavily doped where the metallic contacts will connect.



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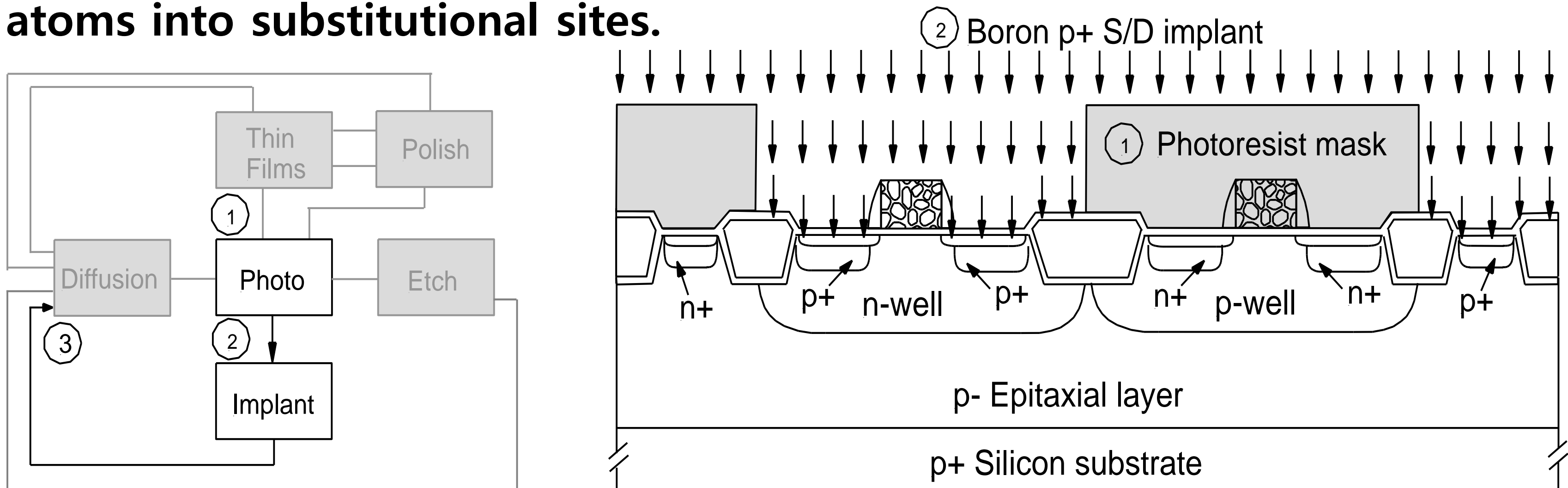
p^+ Source/Drain Implant

- Similar to the previous step, the pMOS device is patterned and implanted.

- After this step, the damage to the wafer from the series of implantation must be annealed.

- These anneals are necessary to eliminate the intermediate defect clusters that form as the silicon recrystallizes and absorbs the dopant atoms into substitutional sites.



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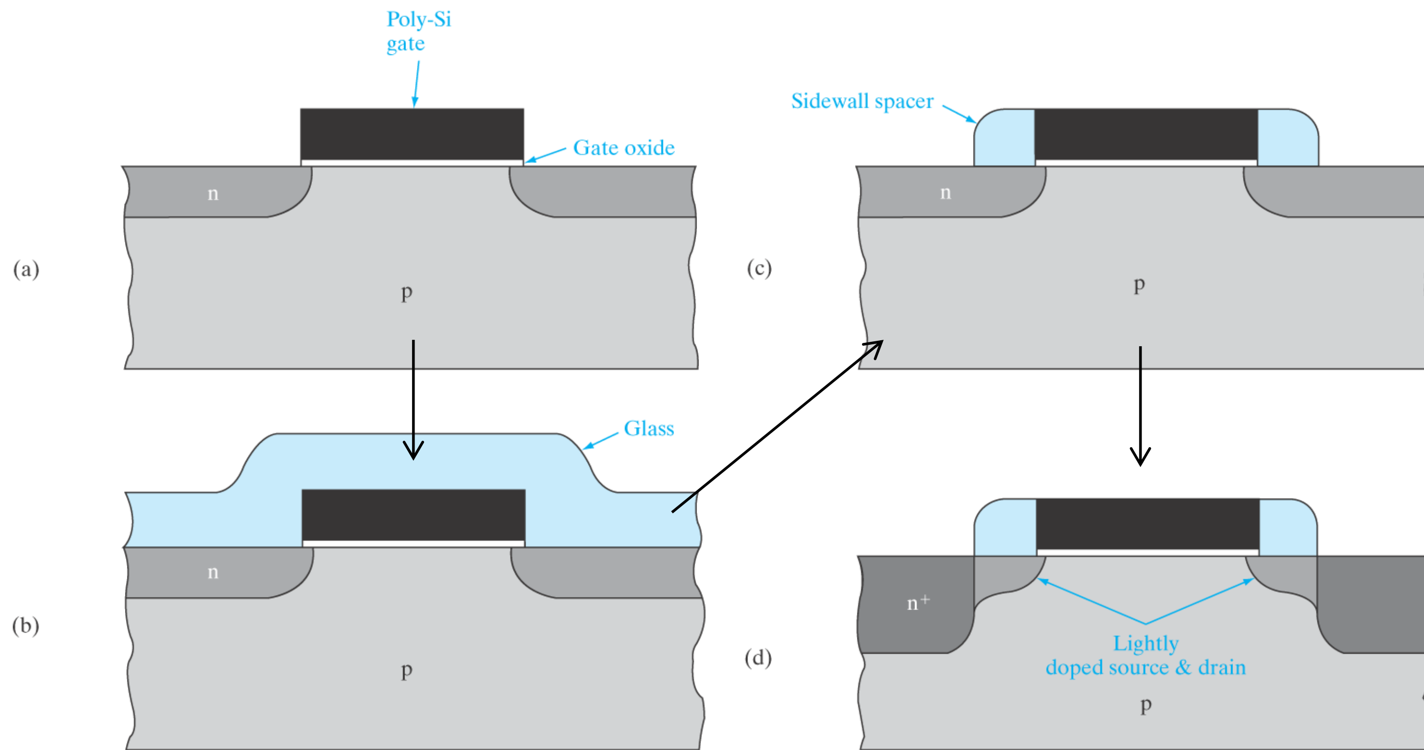


Figure 9.7

Fabrication of the lightly doped drain structure, using sidewall spacers. The polysilicon gate covers the thin gate oxide and masks the first low-dose implant (a). A thick layer is deposited by CVD (b) and is anisotropically etched away to leave only the sidewall spacers (c). These spacers serve as a mask for the second, high-dose implant. After a drive-in diffusion, the LDD structure results (d).

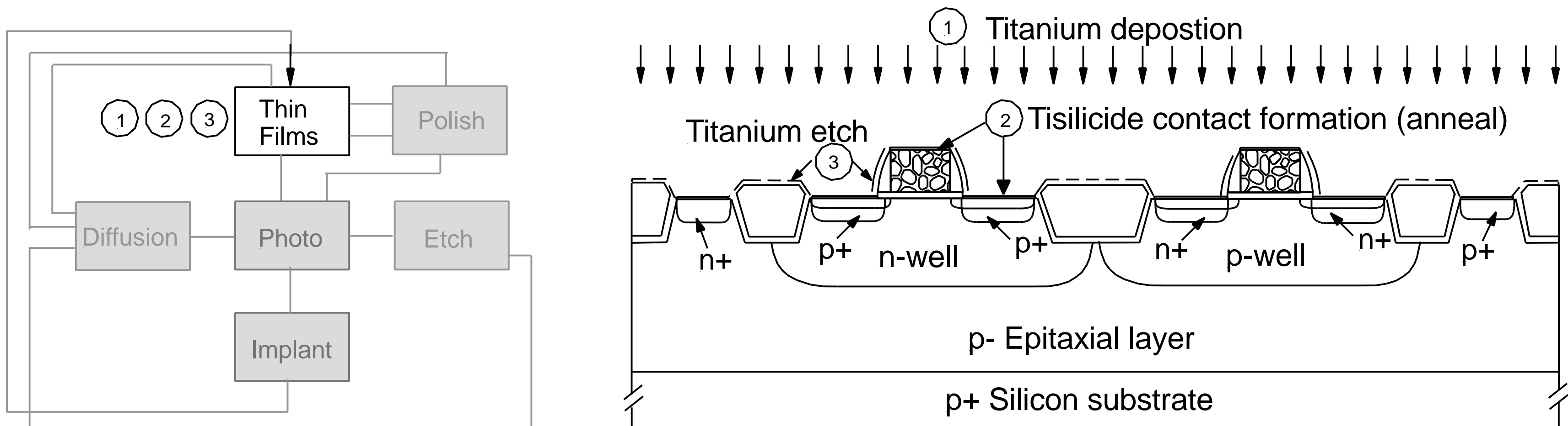
Contact Formation (SALICIDE)

- Metal contacts are formed by using the fact that many metals will not bond to SiO_2, however they will easily form silicides with bare silicon. Examples are Ti, Co or Pt.

- The metal is deposited ① , and then with a modest heat treatment, the Ti/Si interface undergoes solid-phase reactions forming titanium silicide, $TiSi_2$. This contact is a perfect ohmic contact with the silicon substrate.

- The Ti which is in contact with the SiO2, which is everywhere except for the device contact areas, does not form silicide. So a slight metal etch will remove this Ti.

- Since the Ti in the contact areas has already reacted an formed $TiSi_2$, this new compound is impervious to the Ti etchant. This step OMITS a lithography step!



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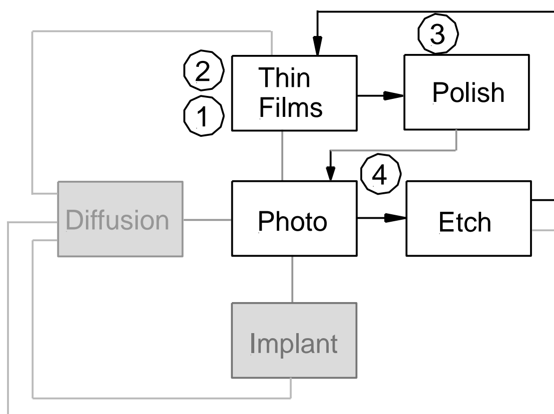
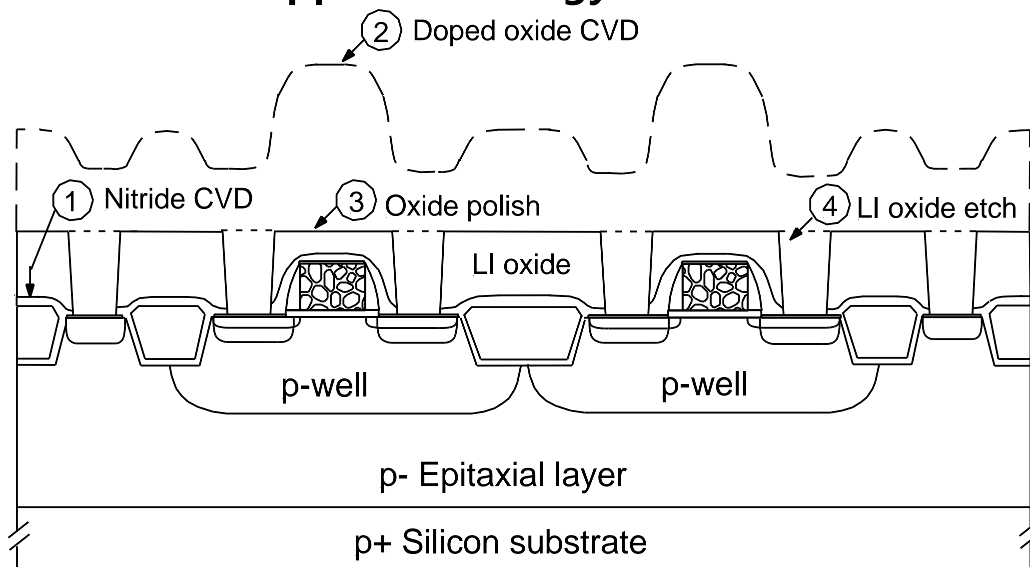
Oxide Dielectric Formation (ILD)

1. **Thin layer of Si_3N_4 is deposited (CVD, 100 nm), to protect all active components from contamination. See layer ① in diagram.**
2. **Thick SiO_2 is deposited (CVD, 1000 nm, ②). This oxide is usually doped with boron or phosphorus to obtain better dielectric qualities which matches signal propogation.**
3. **CMP planarizes the SiO_2 layer, ②, until it is a smooth layer about 800 nm above silicon, ③.**
4. **"Trenches", ④, are patterned on the SiO_2 layer, ②, using lithography and then these deep narrow bands are etched using directional plasma etching. These trenches will form "plugs" to connect to upper metallurgy lines.**





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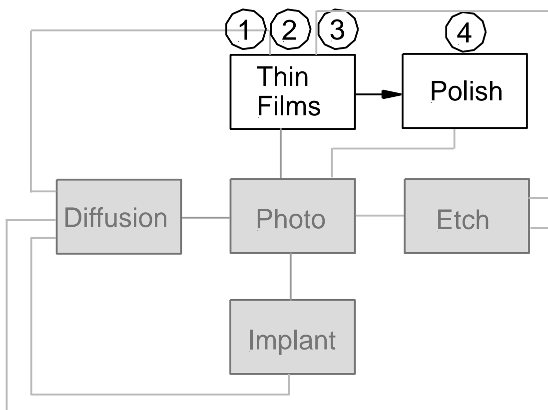
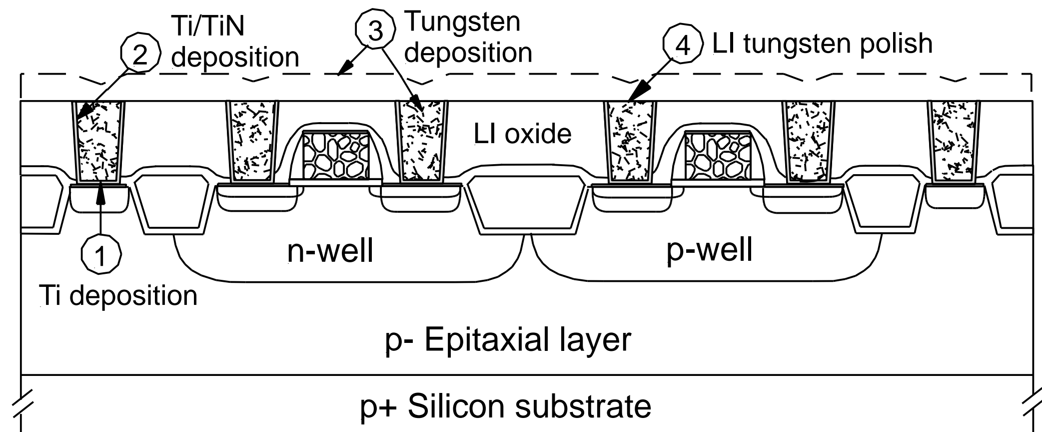
Local Interconnect (LI) Metal Formation

1. A thin layer of "glue", ①, is applied to the trenches. Most metals will not stick to oxides, but metals such as Cr and Ti adhere well and can act as glue to make the metallic connectors stick to the SiO_2. We will assume that Ti is used for this adhesion layer.
2. A thin layer of titanium nitride, TiN, is immediately applied (CVD, 20 nm, ②). This is a diffusion barrier to prevent the next metal from chemically interacting with the active components. The layer is thin enough that it adds little electrical resistance.
3. Tungsten is deposited to fill all trenches, ③ (could also use Al or Cu). Cu is preferred, but requires an electroless deposition.
4. A CMP polish is finally applied to smooth down the metal and oxide to form a glass-like surface, ④.





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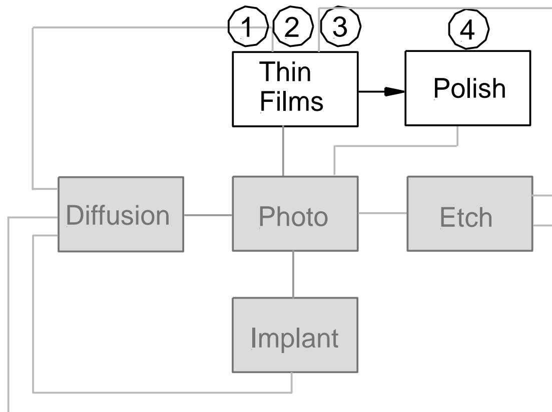
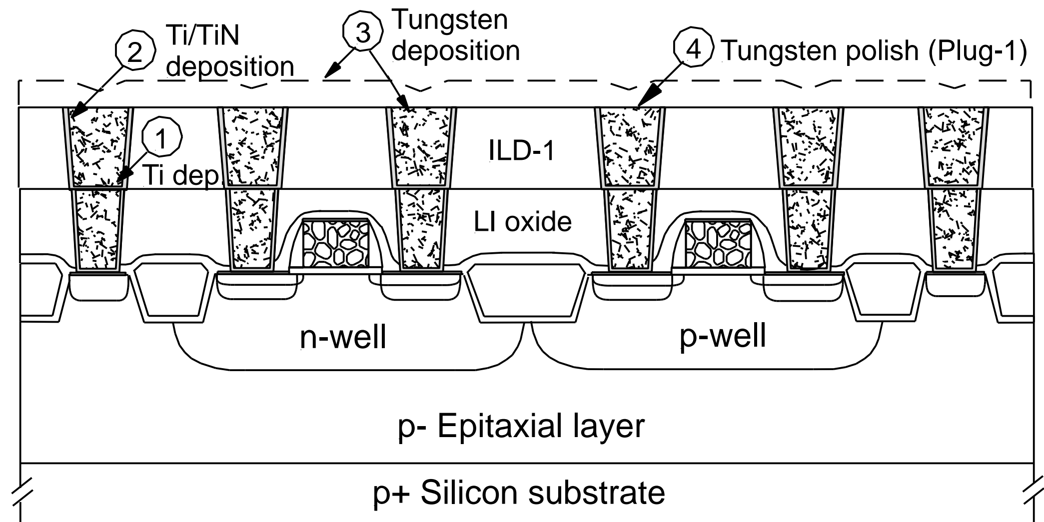
Plug-1 Formation (Plug = Metal in Via)

1. Deposit thin layer to Ti (5nm, ①) to act as glue on the bottom and sides or the trenches.
2. Deposit very thin layer of TiN (CVD, 20um, ②) for a diffusion barrier.
3. Deposit tungsten (CVD, 800 nm, ③) to fill all the via openings.
4. Use tungsten CMP process ④ to polish the tungsten down to a smooth layer with the SiO_2 .





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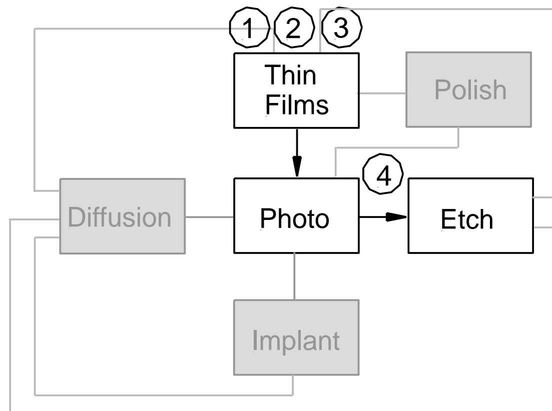
Interconnect Construction

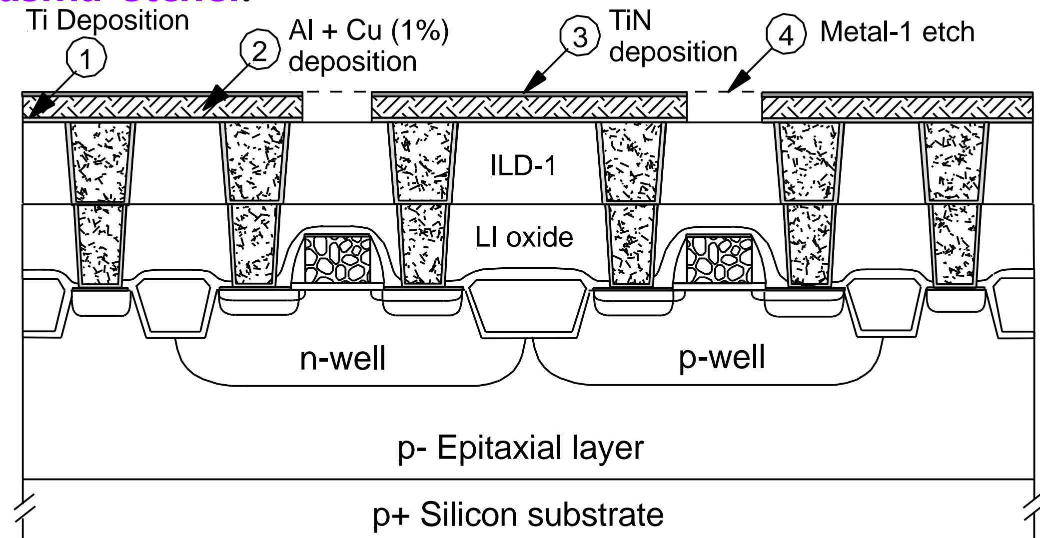
1. As before, a thin layer of titanium ① is sputtered onto the wafer (which contains Vias and plugs) as a glue between the tungsten plugs and the metal connection wires.

2. The metallization will be Al (②, 1-3% Cu, 200 nm), deposited using sputtering. The Cu is added (Al+Cu) to prevent "electro-migration", the undesireable motion of atoms under currents of >5MA/cm^2. (Recently Cu Damascene process is being used after electroplating of Cu.)

3. A thin TiN (③, 50 nm, sputtered) is deposited to act as an anti-reflective coating over the metal. Without this, the next photoresist exposure would be non-uniform with the resist over the metal getting a double exposure of light (since metal reflects light back).

4. Photoresist ④ is applied and patterned, then the 3-layer metal stack (Ti/Al(Cu)/TiN) etched using a plasma etcher.





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