Fundamentals of Microelectronics

- CH1 Why Microelectronics?
- CH2 Basic Physics of Semiconductors
- CH3 Diode Circuits
- CH4 Physics of Bipolar Transistors
- CH5 Bipolar Amplifiers
- CH6 Physics of MOS Transistors
- CH7 CMOS Amplifiers
- CH8 Operational Amplifier As A Black Box
- CH16 Digital CMOS Circuits

Chapter 7 CMOS Amplifiers

- 7.1 General Considerations
- 7.2 Common-Source Stage
- 7.3 Common-Gate Stage
- 7.4 Source Follower
- 7.5 Summary and Additional Examples

Chapter Outline

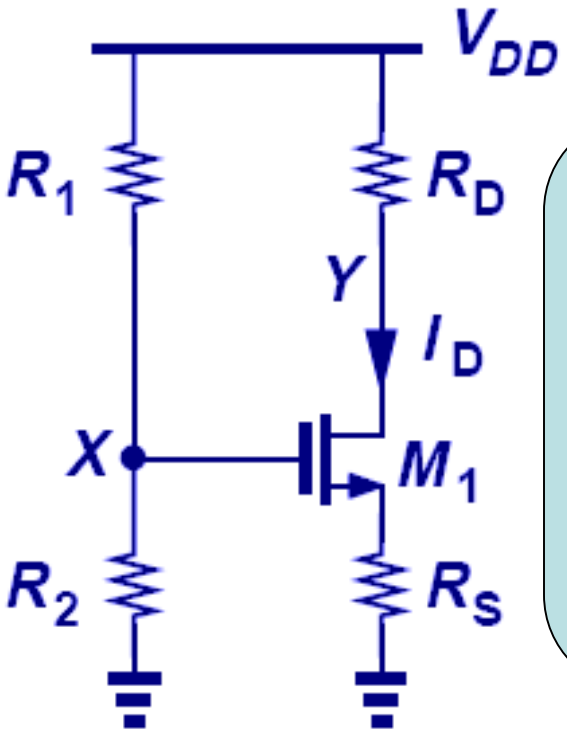
General Concepts

- Biasing of MOS Stages
- Realization of Current Sources

MOS Amplifiers

- Common-Source Stage
- Common-Gate Stage
- Source Follower

MOS Biasing



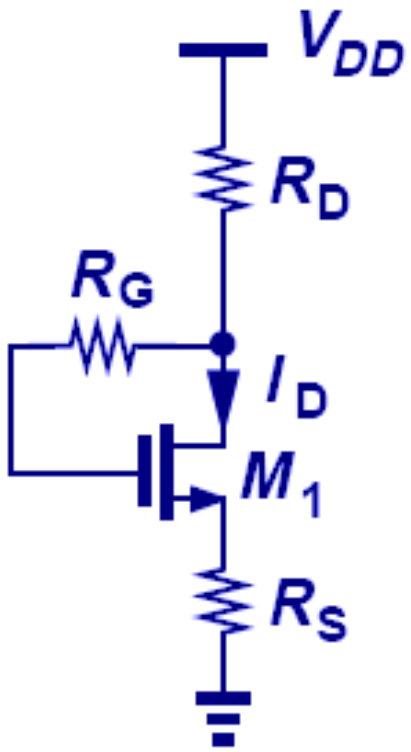
$$\frac{R_2 V_{DD}}{R_1 + R_2} = V_{GS} + I_D R_S \;\;\&\&\;\; I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2$$

$$V_{GS} = -\left(V_1 - V_{TH}\right) + \sqrt{V_1^2 + 2V_1\left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH}\right)}$$

$$V_1 = \frac{1}{\mu_n C_{ox}\dfrac{W}{L}R_S}$$

- **Voltage at X is determined by V_{DD}, R_1, and R_2.**
- **V_{GS} can be found using the equation above, and I_D can be found by using the NMOS current equation.**

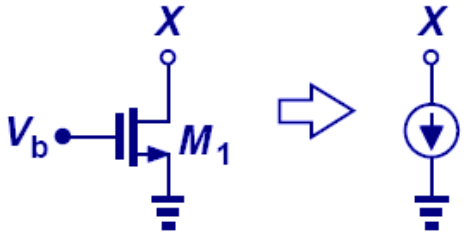
Self-Biased MOS Stage



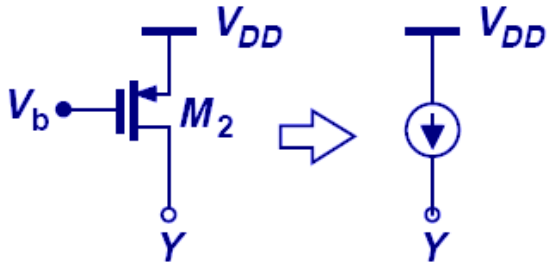
$$I_D R_D + V_{GS} + R_S I_D = V_{DD}$$

- **The circuit above is analyzed by noting M1 is in saturation and no potential drop appears across R_G.**

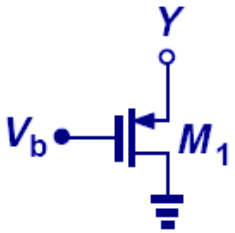
Current Sources



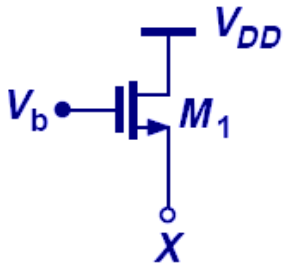
(a)



(b)



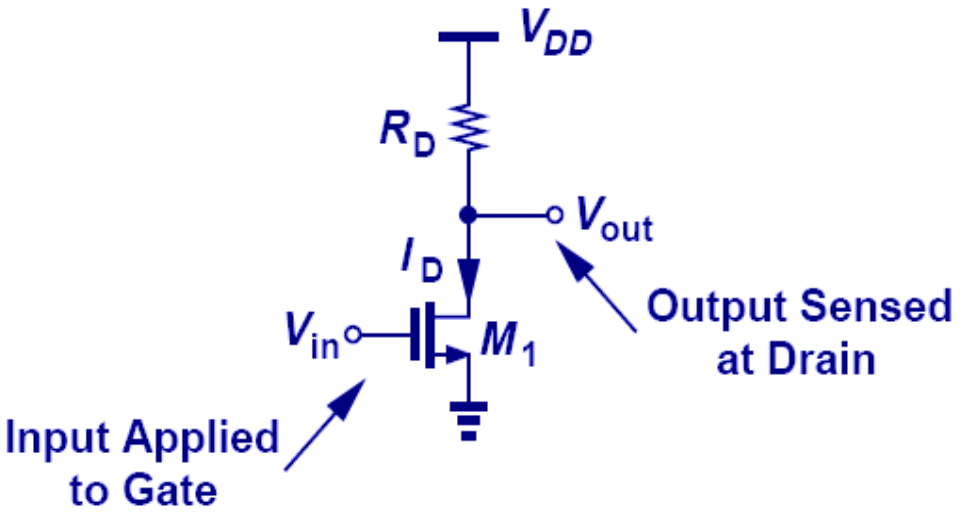
(c)

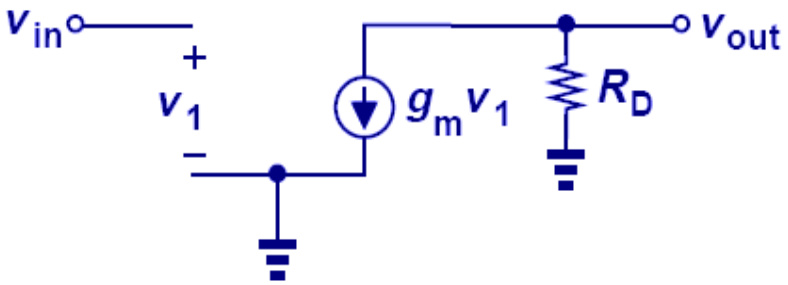


(d)

- **When in saturation region, a MOSFET behaves as a current source.**
- **NMOS draws current from a point to ground (sinks current), whereas PMOS draws current from V_{DD} to a point (sources current).**

Common-Source Stage



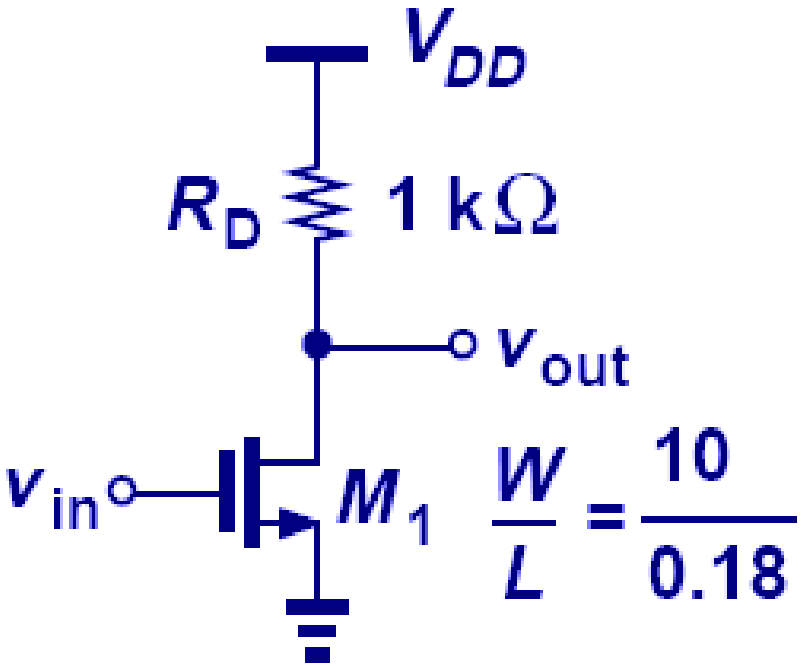


$$\lambda = 0$$

$$A_v = -g_m R_D$$

$$A_v = -\sqrt{2\mu_n C_{ox} \frac{W}{L} I_D R_D}$$

Operation in Saturation



$$V_{in} - V_{out} < V_{TH}$$
$$V_{GS} - (V_{DD} - R_D I_D) < V_{TH}$$
$$R_D I_D < V_{DD} - (V_{GS} - V_{TH})$$

- In order to maintain operation in saturation, V_{out} cannot fall below V_{in} by more than one threshold voltage.
- The condition above ensures operation in saturation.

Example 7.4

Example 7.4

Calculate the small-signal voltage gain of the CS stage shown in Fig. 7.6 if $I_D = 1\,\text{mA}$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $\lambda = 0$. Verify that M_1 operates in saturation.

Solution We have

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L} I_D}$$

$$= \frac{1}{300\,\Omega}.$$

Thus,

$$A_v = -g_m R_D$$

$$= 3.33.$$

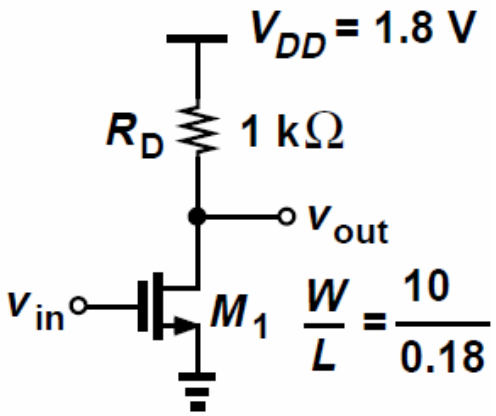


Figure 7.6 Example of CS stage.

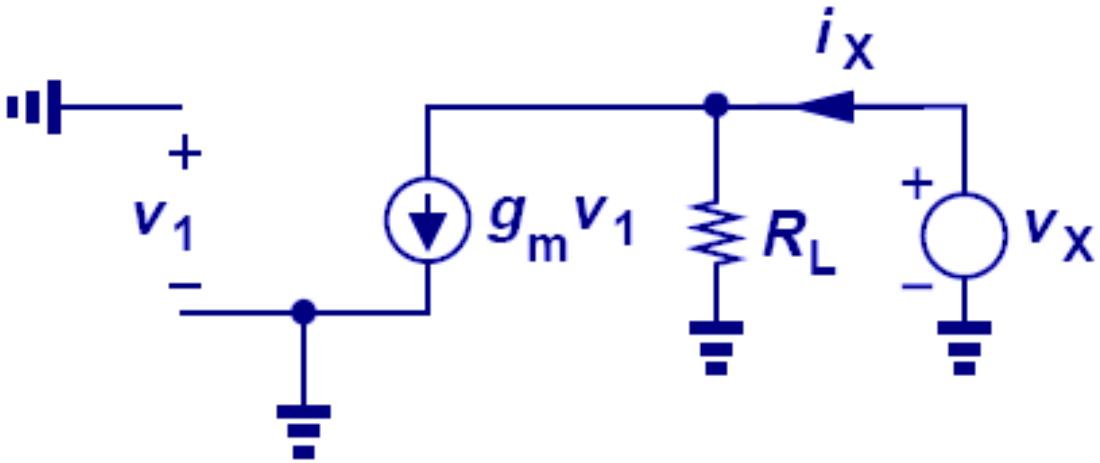
To check the operation region, we first determine the gate-source voltage:

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_D}{\mu_n C_{ox}\frac{W}{L}}} \tag{7.42}$$

$$= 1.1\,\text{V}. \tag{7.43}$$

The drain voltage is equal to $V_{DD} - R_D I_D = 0.8\,\text{V}$. Since $V_{GS} - V_{TH} = 0.6\,\text{V}$, the device indeed operates in saturation and has a margin of 0.2 V with respect to the triode region. For example, if R_D is doubled with the intention of doubling A_v, then M_1 enters the triode region and its transconductance drops.

CS Stage with λ=0

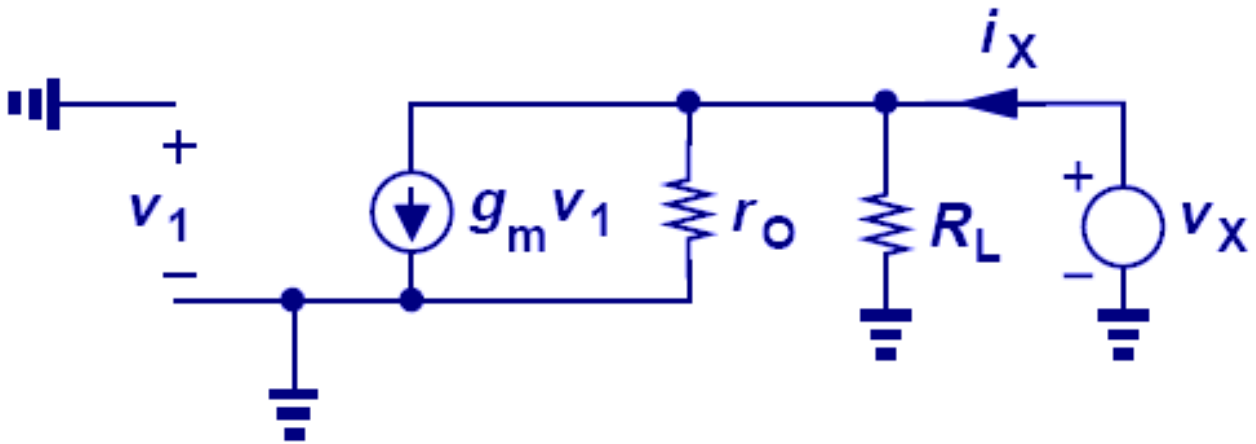


$$A_v = -g_m R_L$$

$$R_{in} = \infty$$

$$R_{out} = R_L$$

CS Stage with $\lambda \neq 0$



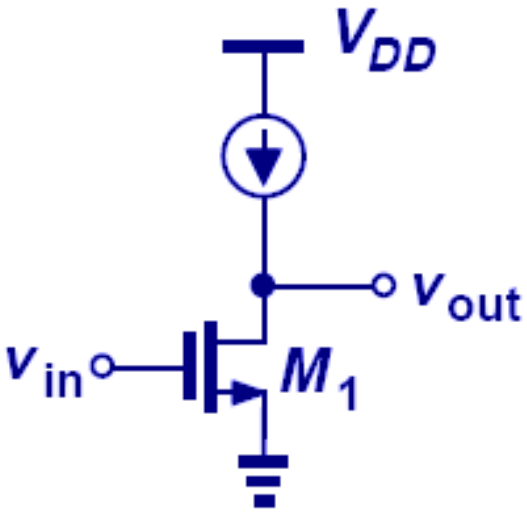
$$A_v = -g_m\left(R_L \parallel r_O\right)$$

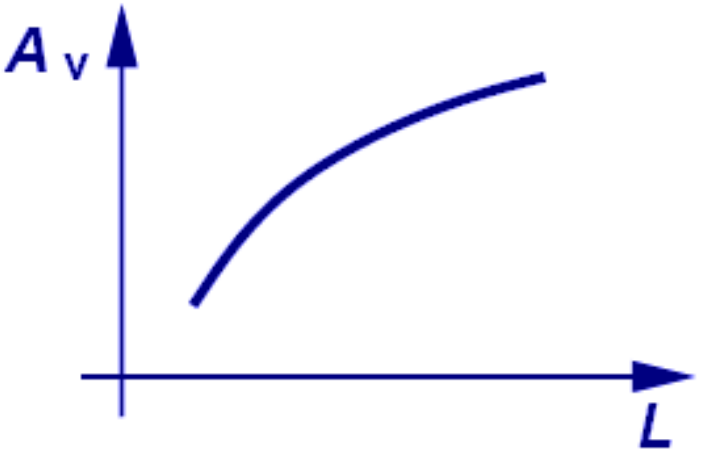
$$R_{in} = \infty$$

$$R_{out} = R_L \parallel r_O$$

- **However, Early effect and channel length modulation affect CE and CS stages in a similar manner.**

CS Gain Variation with Channel Length

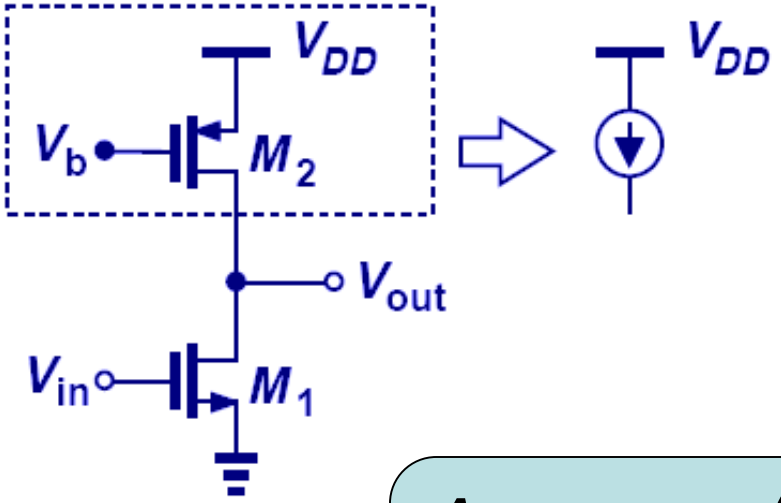


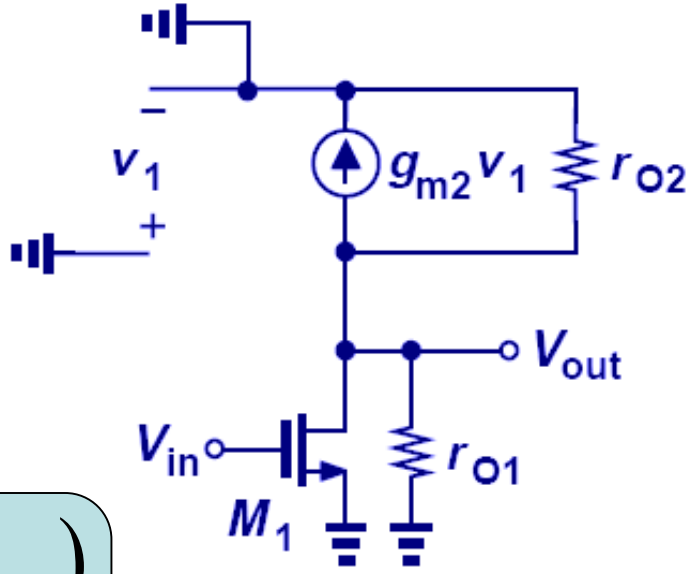


$$|A_v| = \frac{\sqrt{2\mu_n C_{ox}\frac{W}{L}}}{\lambda\sqrt{I_D}} \propto \sqrt{\frac{2\mu_n C_{ox} WL}{I_D}}$$

- **Since λ is inversely proportional to L, the voltage gain actually becomes proportional to the square root of L.**

CS Stage with Current-Source Load



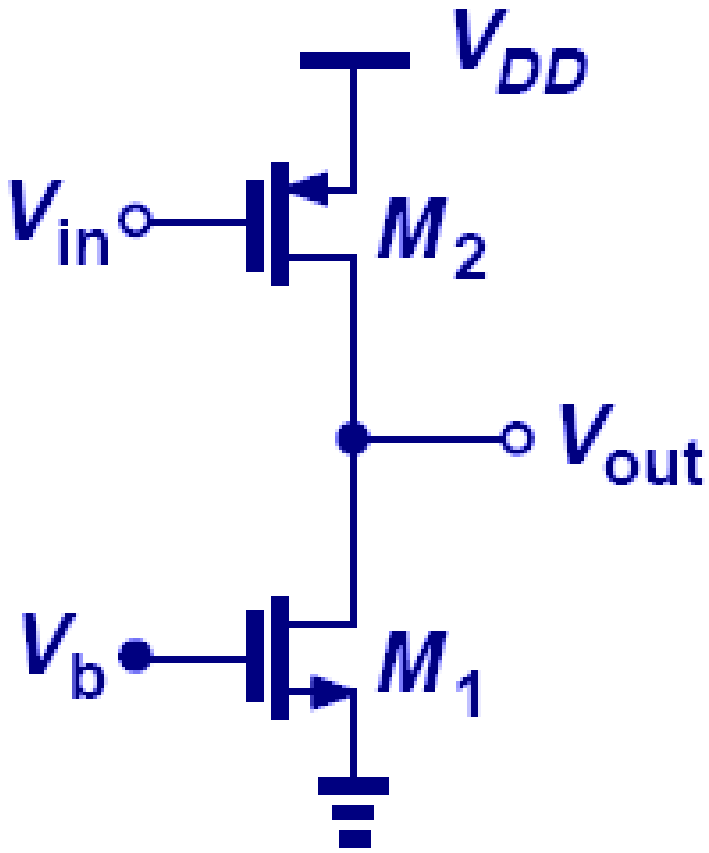


$$A_v = -g_{m1}(r_{O1} \parallel r_{O2})$$

$$R_{out} = r_{O1} \parallel r_{O2}$$

- To alleviate the headroom problem, an active current-source load is used.
- This is advantageous because a current-source has a high output resistance and can tolerate a small voltage drop across it.

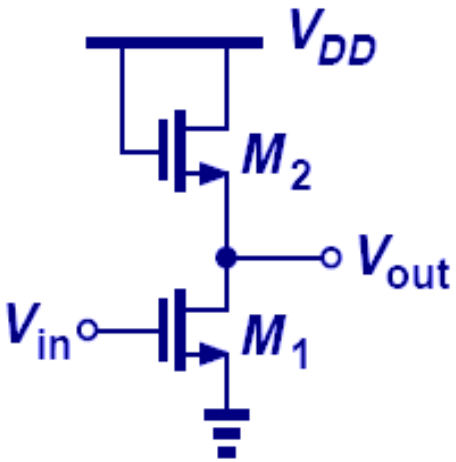
PMOS CS Stage with NMOS as Load

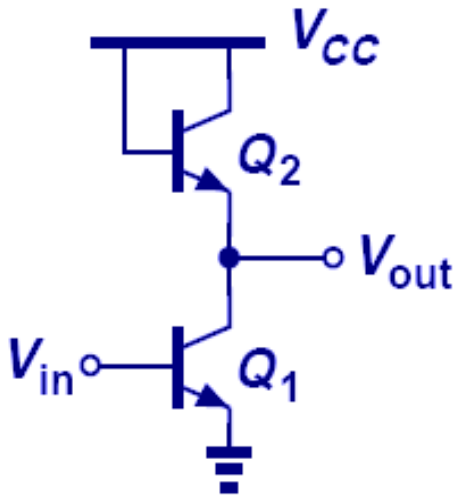


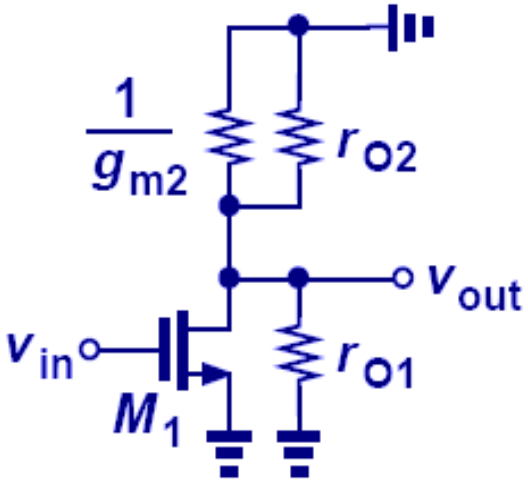
$$A_v = -g_{m2}(r_{O1} \| r_{O2})$$

- **Similarly, with PMOS as input stage and NMOS as the load, the voltage gain is the same as before.**

CS Stage with Diode-Connected Load





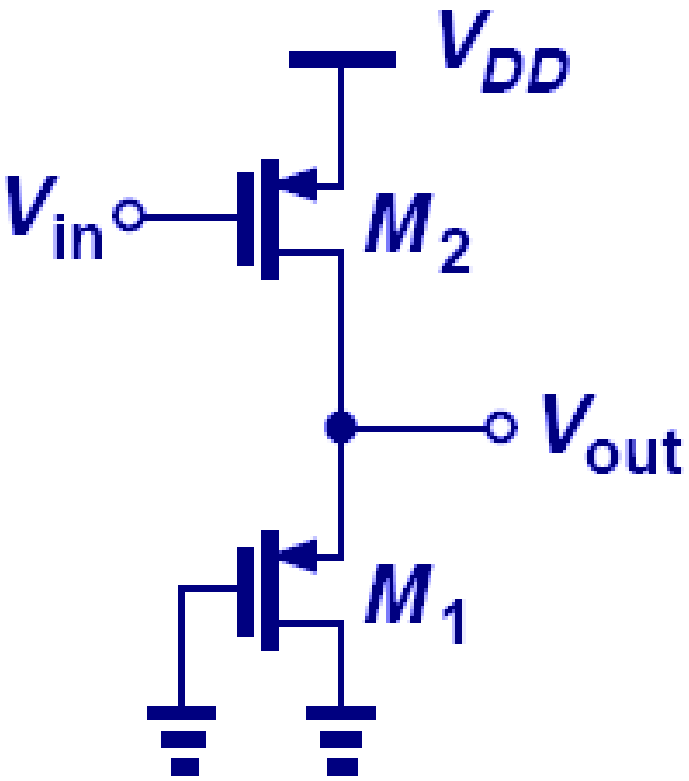


$$A_v = -g_{m1} \cdot \frac{1}{g_{m2}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}$$

$$A_v = -g_{m1}\left(\frac{1}{g_{m2}} \parallel r_{O2} \parallel r_{O1}\right)$$

- **Lower gain, but less dependent on process parameters.**

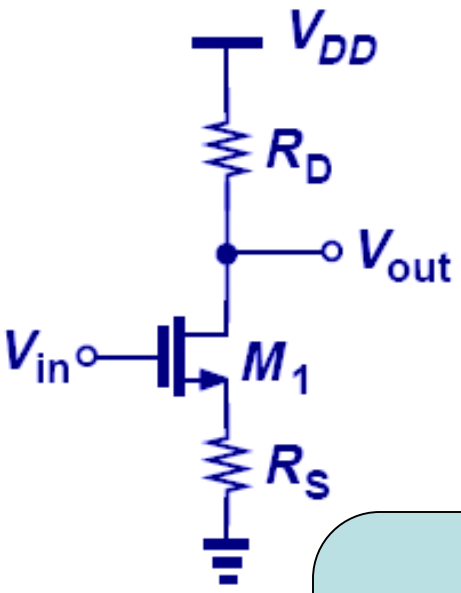
CS Stage with Diode-Connected PMOS Device

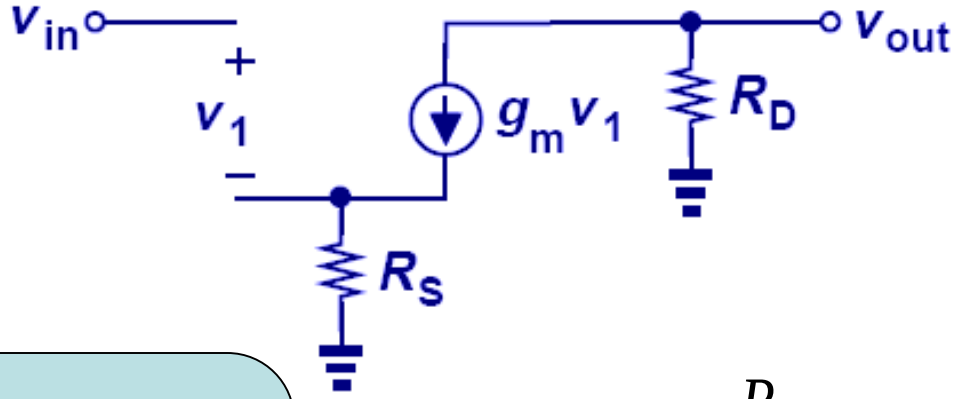


$$A_v = -g_{m2}\left(\frac{1}{g_{m1}} \| r_{o1} \| r_{o2}\right)$$

- **Note that PMOS circuit symbol is usually drawn with the source on top of the drain.**

CS Stage with Degeneration





$$A_v = -\frac{R_D}{R_S + \frac{1}{g_m}\left(1 + \frac{R_S + R_D}{r_0}\right)}$$

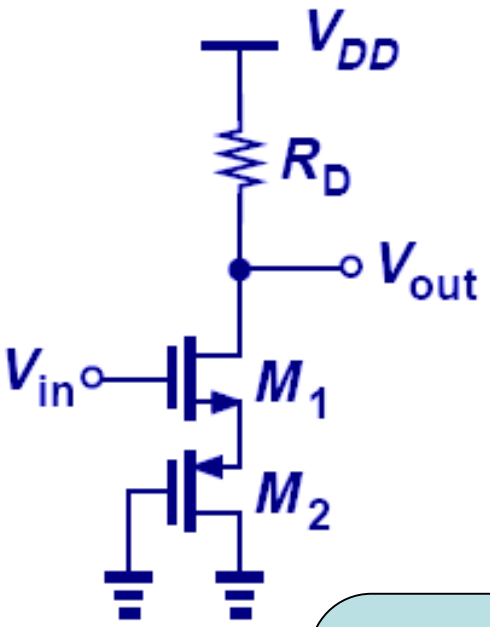
$\lambda \neq 0$

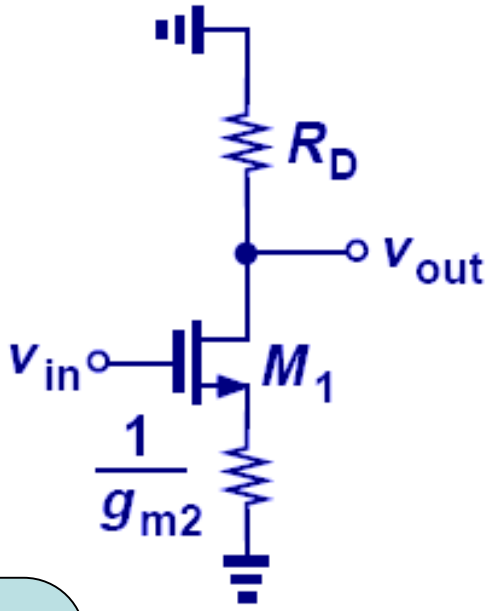
$$A_v = -\frac{R_D}{\frac{1}{g_m} + R_S}$$

$\lambda = 0$

- **Similar to bipolar counterpart, when a CS stage is degenerated, its gain, I/O impedances, and linearity change.**

Example of CS Stage with Degeneration

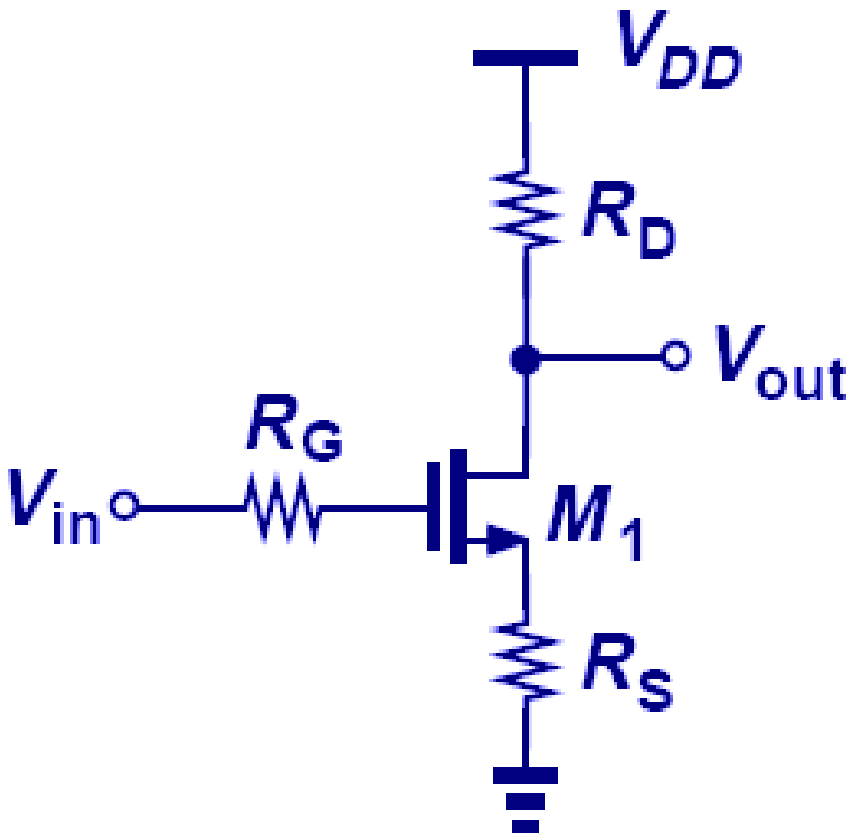




$$A_v = -\frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- **A diode-connected device degenerates a CS stage.**

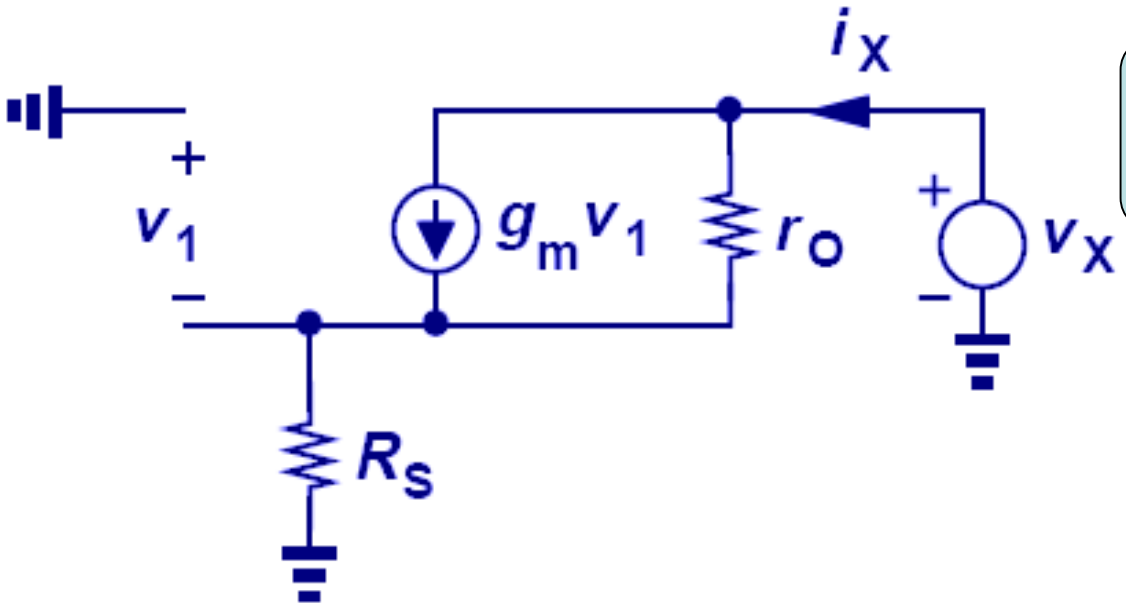
CS Stage with Gate Resistance



$$V_{R_G} = 0$$

- **Since at low frequencies, the gate conducts no current, gate resistance does not affect the gain or I/O impedances.**

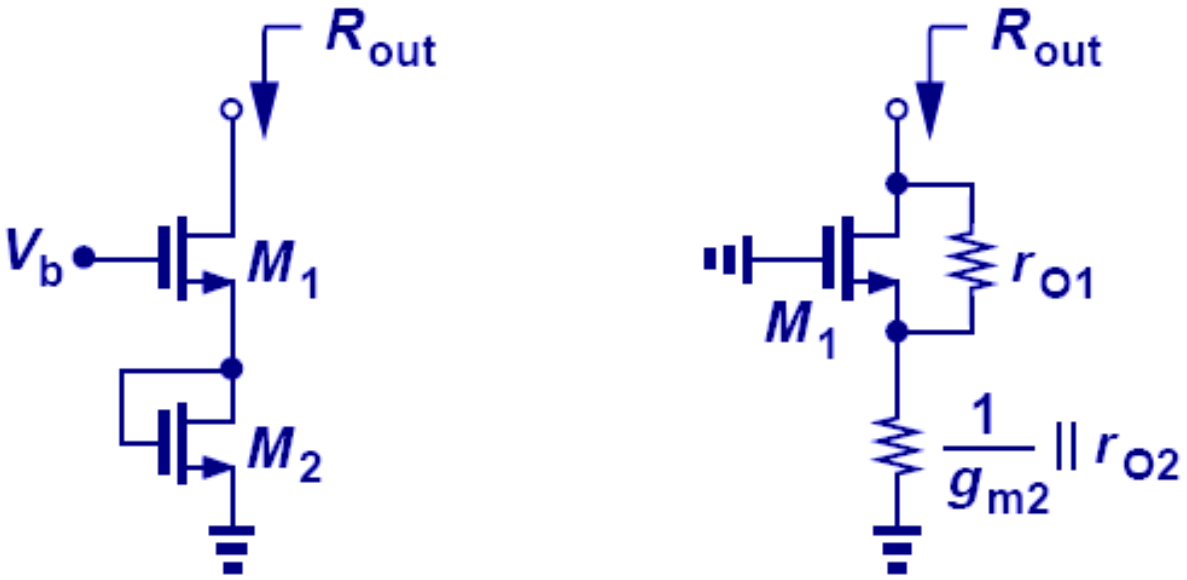
Output Impedance of CS Stage with Degeneration



$$r_{out} \approx g_m r_O R_S + r_O$$

- **Similar to the bipolar counterpart, degeneration boosts output impedance.**

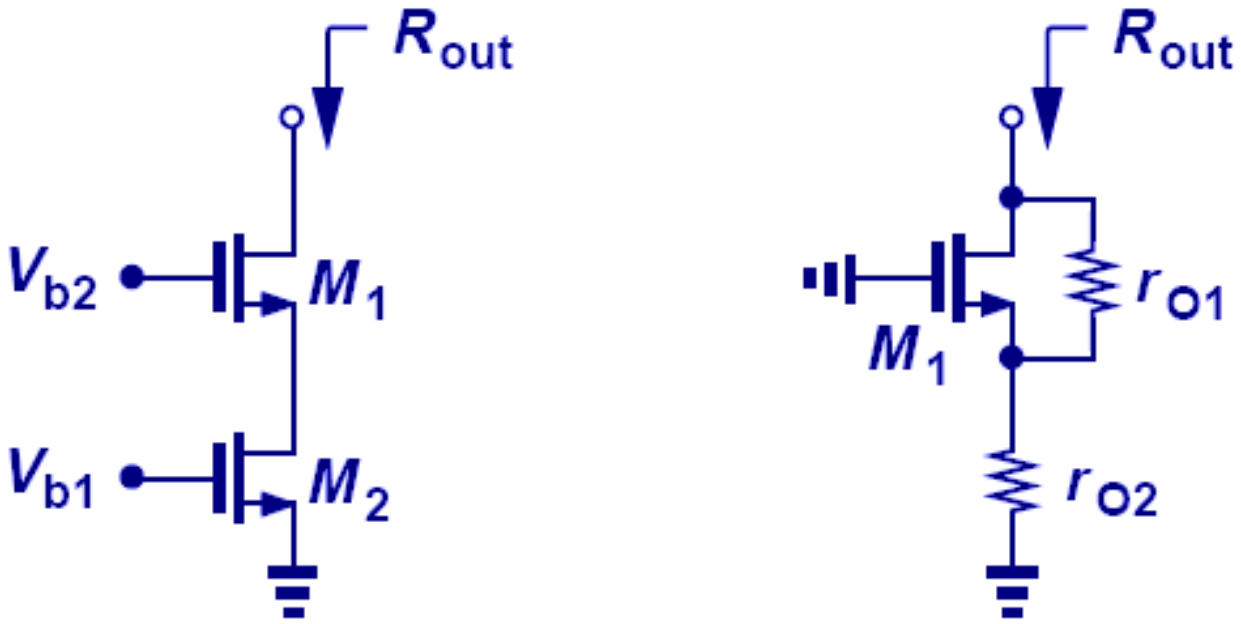
Output Impedance Example (I)



$$R_{out} = r_{O1}\left(1 + g_{m1}\frac{1}{g_{m2}}\right) + \frac{1}{g_{m2}}$$

- When $1/g_m$ is parallel with r_{O2}, we often just consider $1/g_m$.

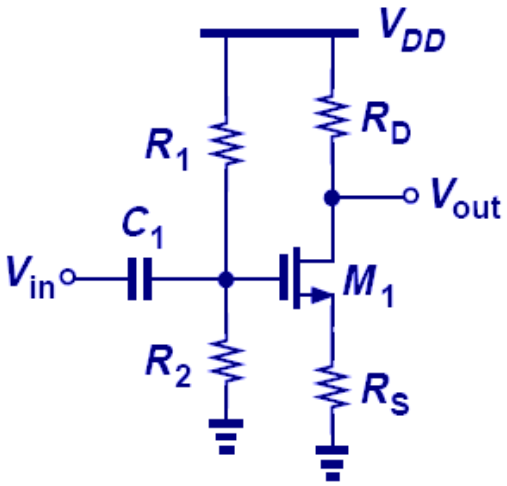
Output Impedance Example (II)

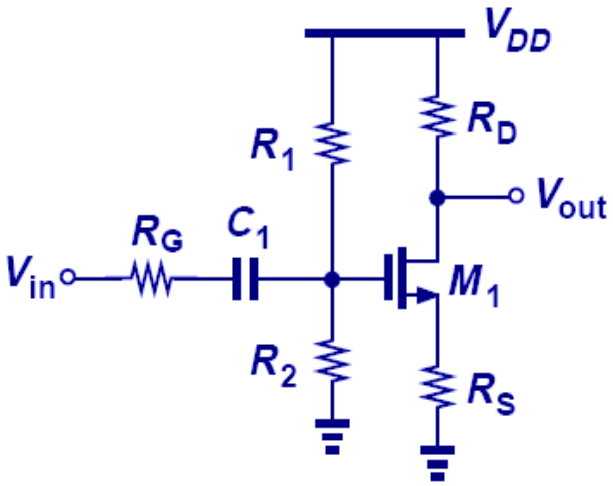


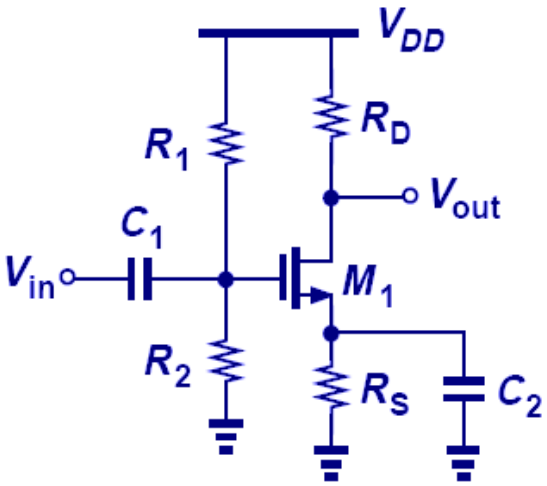
$$R_{out} \approx g_{m1} r_{O1} r_{O2} + r_{O1}$$

- **In this example, the impedance that degenerates the CS stage is r_O, instead of $1/g_m$ in the previous example.**

CS Core with Biasing



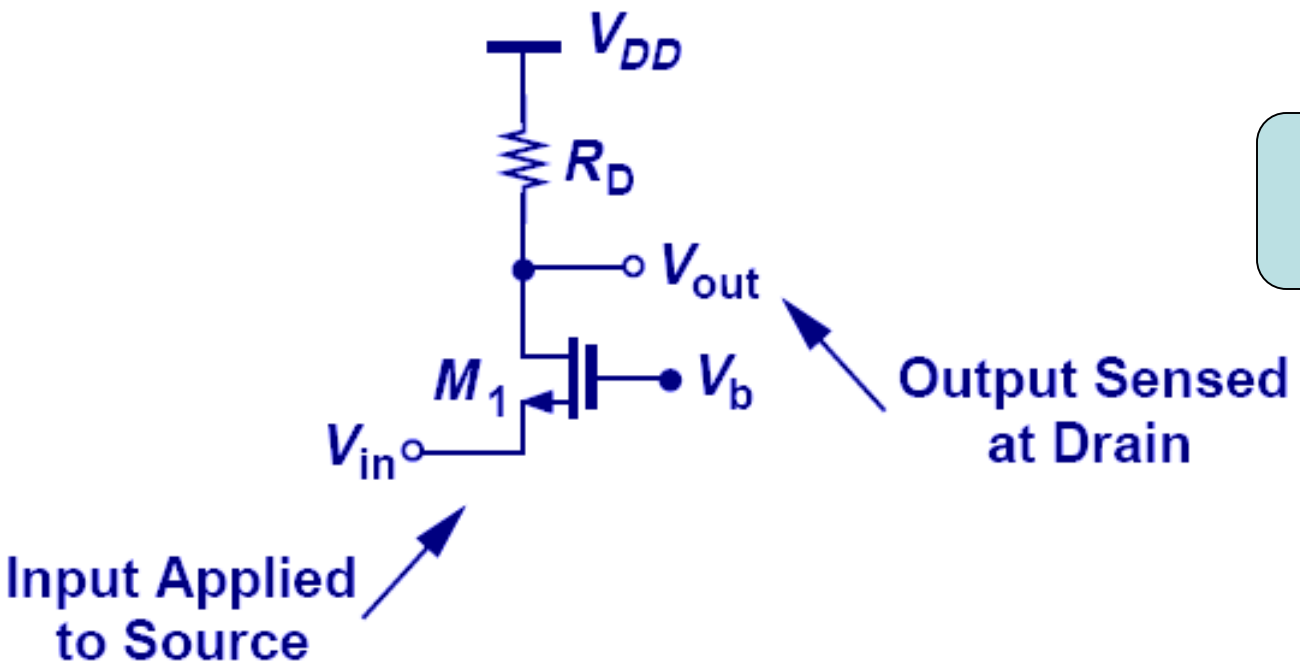




$$A_v = \frac{R_1 \| R_2}{R_G + R_1 \| R_2} \cdot \frac{-R_D}{\frac{1}{g_m} + R_S}, A_v = -\frac{R_1 \| R_2}{R_G + R_1 \| R_2} g_m R_D$$

- **Degeneration is used to stabilize bias point, and a bypass capacitor can be used to obtain a larger small-signal voltage gain at the frequency of interest.**

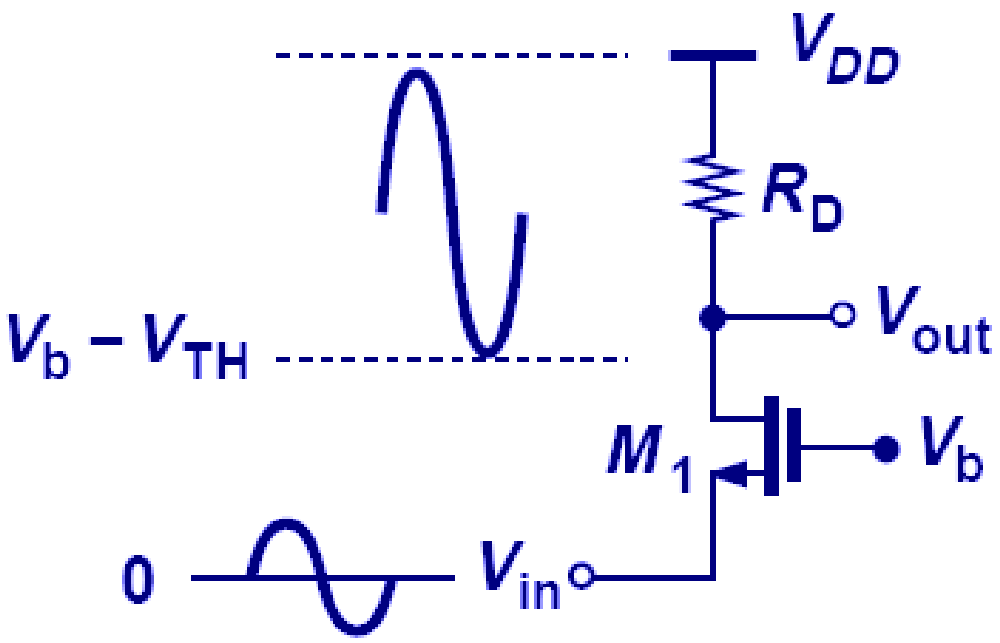
Common-Gate Stage



$$A_v = g_m R_D$$

- **Common-gate stage is similar to common-base stage: a rise in input causes a rise in output. So the gain is positive.**

Signal Levels in CG Stage



- **In order to maintain M_1 in saturation, the signal swing at V_{out} cannot fall below V_b-V_{TH}.**

Example 7.12

Example 7.12

A microphone having a dc level of zero drives a CG stage biased at $I_D = 0.5\,\text{mA}$. If $W/L = 50$, $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, and $V_{DD} = 1.8\,\text{V}$, determine the maximum allowable value of R_D and hence the maximum voltage gain. Neglect channel-length modulation.

Solution

With W/L known, the gate-source voltage can be determined from

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2$$

as

$$V_{GS} = 0.947\,\text{V}.$$

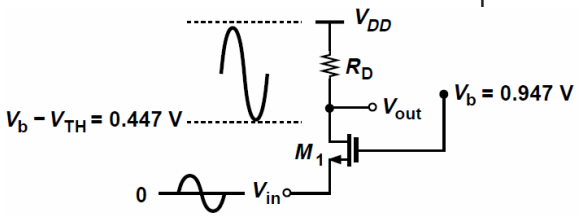


Figure 7.22 Signal levels in CG stage.

For M_1 to remain in saturation,

$$V_{DD} - I_D R_D > V_b - V_{TH} \tag{7.98}$$

and hence

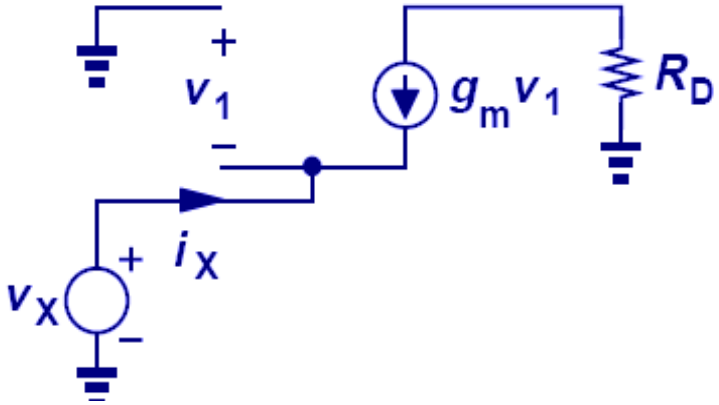
$$R_D < 2.71\,\text{k}\Omega. \tag{7.99}$$

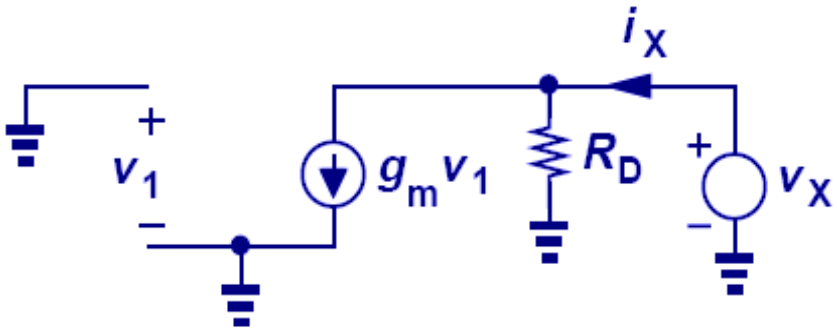
Also, the above value of W/L and I_D yield $g_m = (447\,\Omega)^{-1}$ and

$$A_v \leq 6.06. \tag{7.100}$$

Figure 7.22 summarizes the allowable signal levels in this design. The gate voltage can be generated using a resistive divider similar to that in Fig. 7.20(a).

I/O Impedances of CG Stage





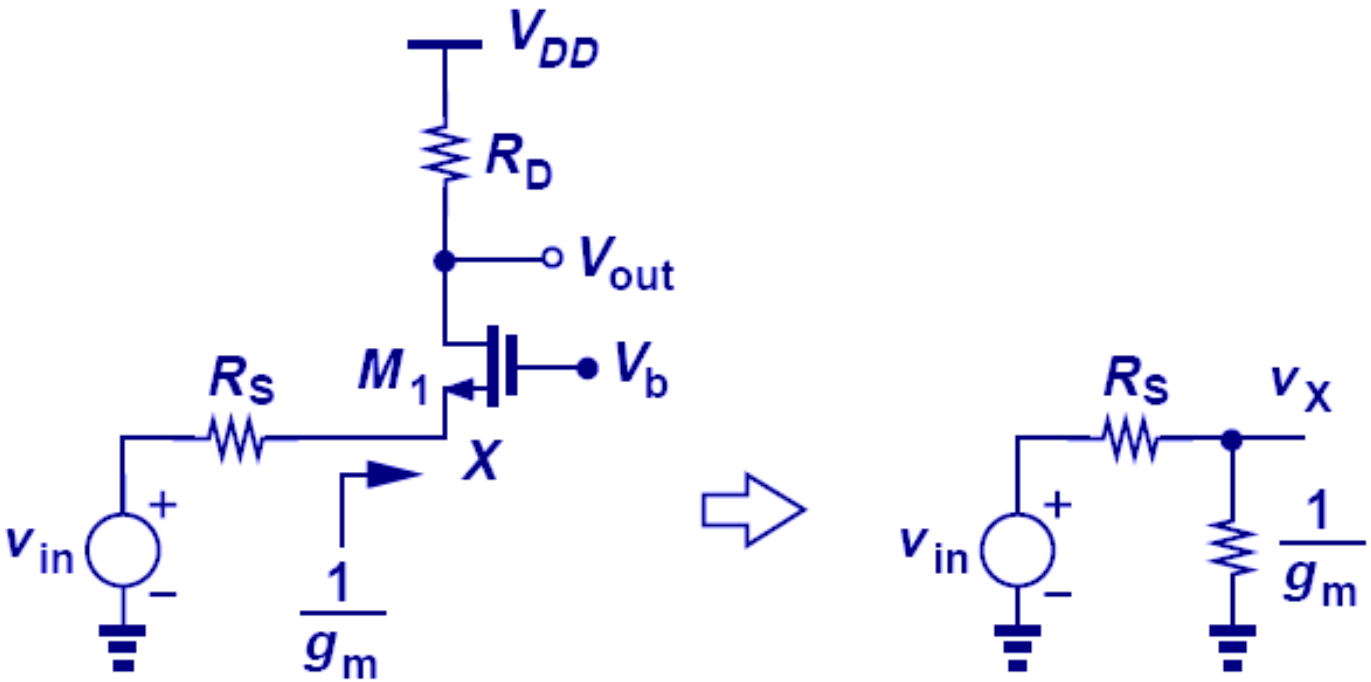
$$R_{in} = \frac{1}{g_m}$$

$$\lambda = 0$$

$$R_{out} = R_D$$

- **The input and output impedances of CG stage are similar to those of CB stage.**

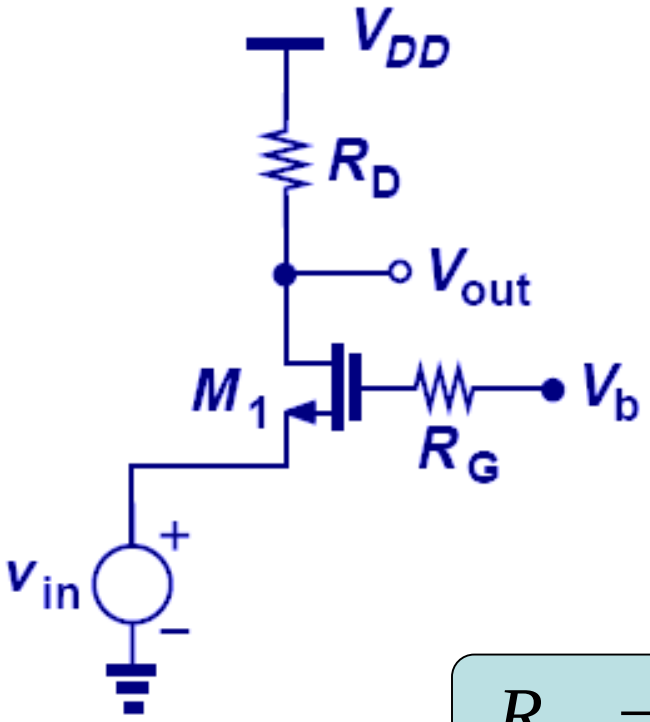
CG Stage with Source Resistance

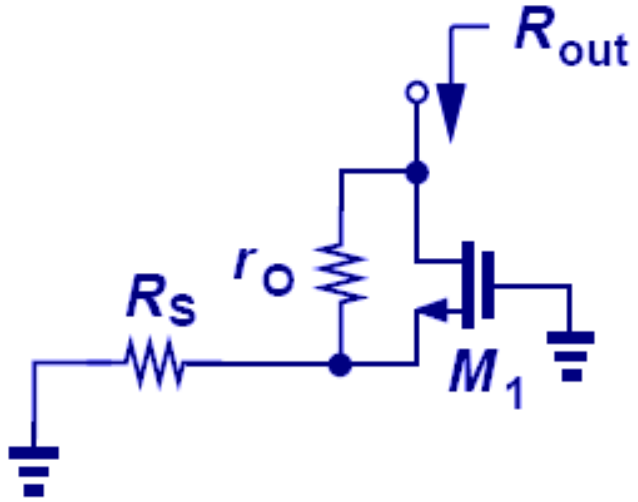


$$A_v = \frac{R_D}{\frac{1}{g_m} + R_S}$$

- **When a source resistance is present, the voltage gain is equal to that of a CS stage with degeneration, only positive.**

Generalized CG Behavior

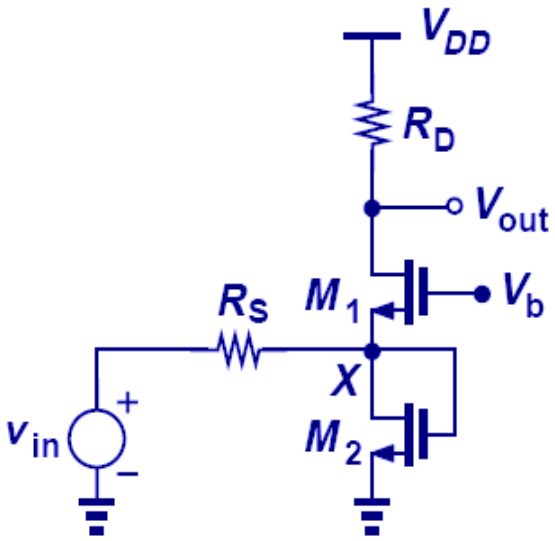


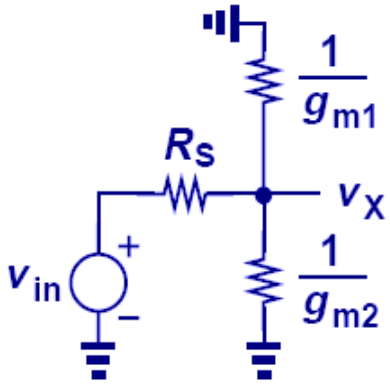


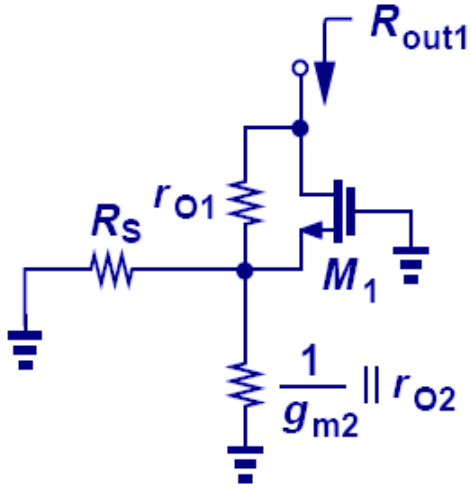
$$R_{out} = (1 + g_m r_O) R_S + r_O$$

- When a gate resistance is present it does not affect the gain and I/O impedances since there is no potential drop across it (at low frequencies).
- The output impedance of a CG stage with source resistance is identical to that of CS stage with degeneration.

Example of CG Stage



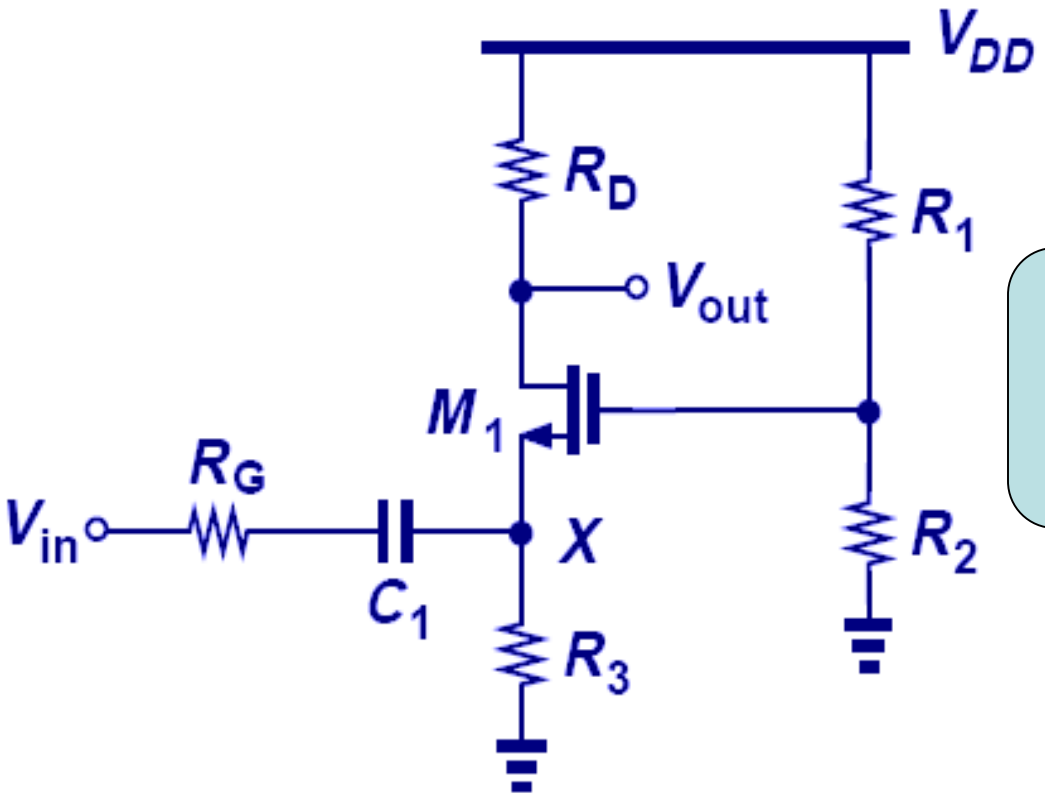




$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}R_D}{1+(g_{m1}+g_{m2})R_S} \qquad R_{out} \approx \left[g_{m1}r_{O1}\left(\frac{1}{g_{m2}} \| R_S\right) + r_{O1} \right] \| R_D$$

- **Diode-connected M_2 acts as a resistor to provide the bias current.**

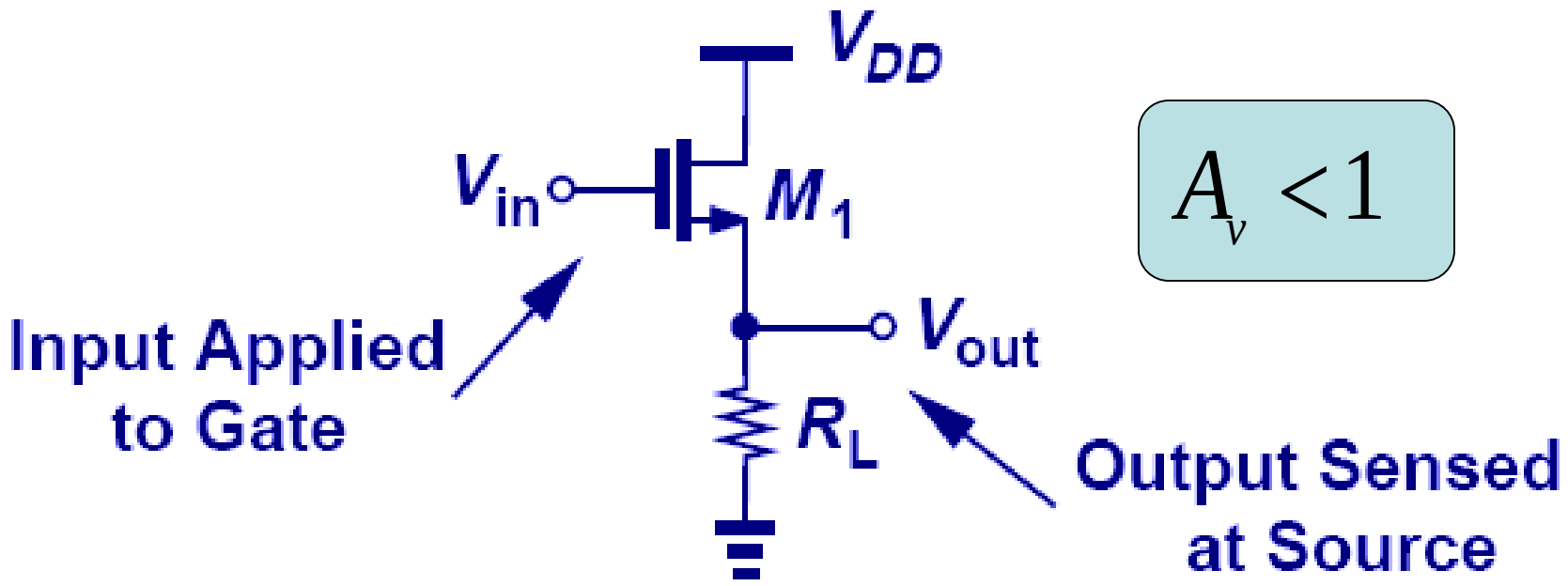
CG Stage with Biasing



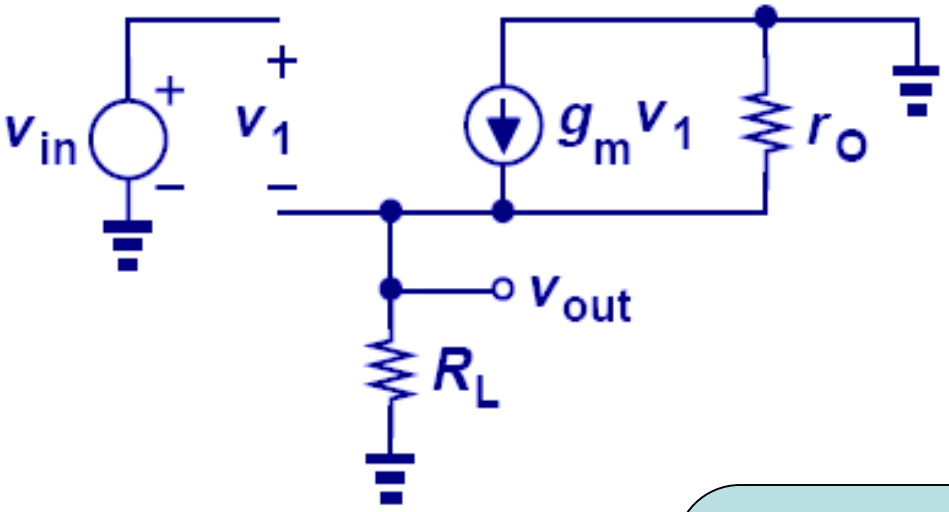
$$\frac{v_{out}}{v_{in}} = \frac{R_3 \| (1/g_m)}{R_3 \| (1/g_m) + R_S} \cdot g_m R_D$$

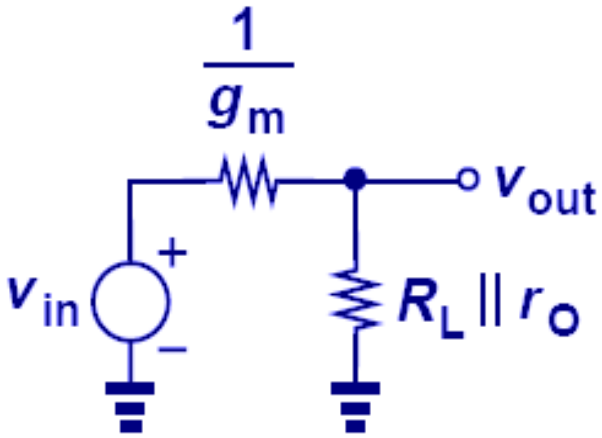
- R_1 and R_2 provide gate bias voltage, and R_3 provides a path for DC bias current of M_1 to flow to ground.

Source Follower Stage



Source Follower Core





$$\frac{v_{out}}{v_{in}} = \frac{r_O \| R_L}{\frac{1}{g_m} + r_O \| R_L}$$

- **Similar to the emitter follower, the source follower can be analyzed as a resistor divider.**

Example 7.17

Example 7.17

Design a source follower to drive a 50-Ω load with a voltage gain of 0.5 and a power budget of 10 mW. Assume $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{TH} = 0.5\,\text{V}$, $\lambda = 0$, and $V_{DD} = 1.8\,\text{V}$.

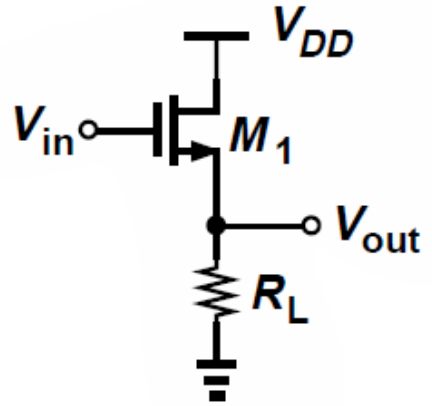


Figure 7.28 Source follower.

Solution With $R_L = 50\,\Omega$ and $r_O = \infty$ in Fig. 7.28, we have

$$A_v = \frac{R_L}{\frac{1}{g_m} + R_L}$$

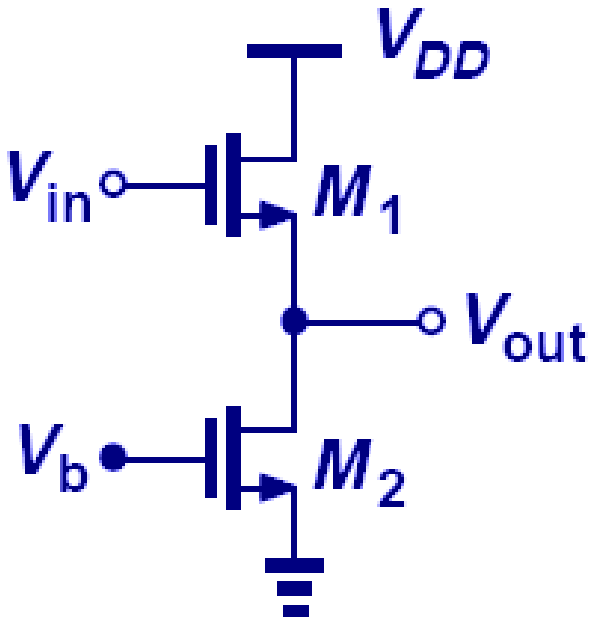
and hence

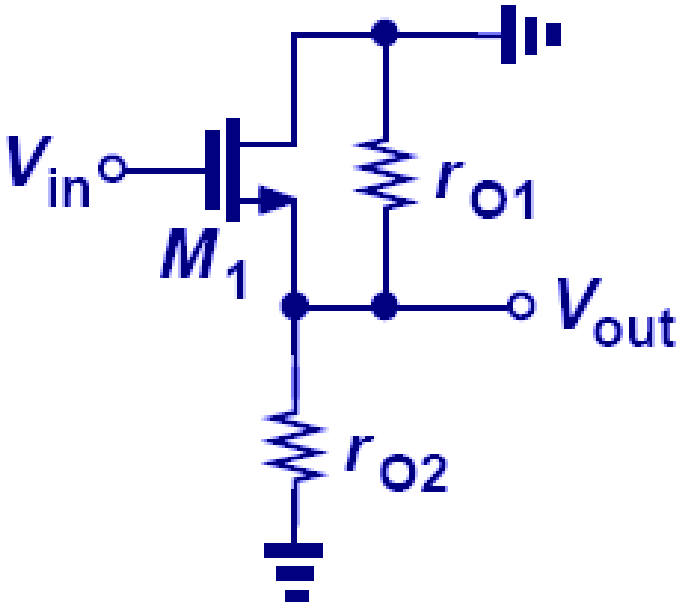
$$g_m = \frac{1}{50\,\Omega}. \tag{7.134}$$

The power budget and supply voltage yield a maximum supply current of 5.56 mA. Using this value for I_D in $g_m = \sqrt{2\mu_n C_{ox}(W/L)I_D}$ gives

$$W/L = 360. \tag{7.135}$$

Source Follower Example

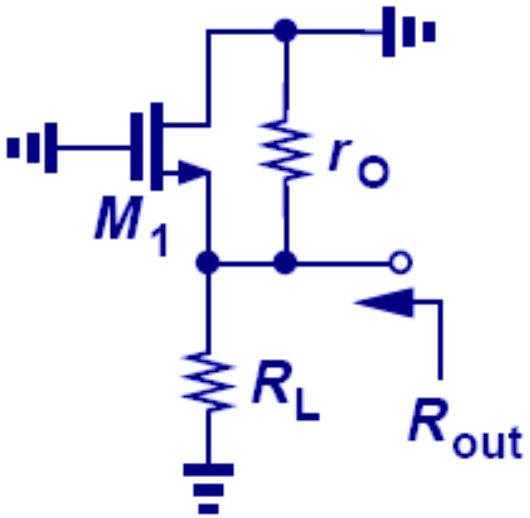


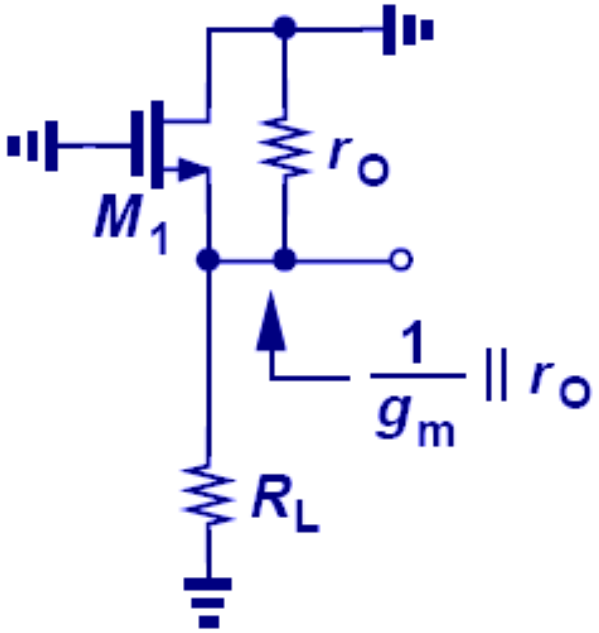


$$A_v = \frac{r_{O1} \parallel r_{O2}}{\dfrac{1}{g_{m1}} + r_{O1} \parallel r_{O2}}$$

- **In this example, M_2 acts as a current source.**

Output Resistance of Source Follower



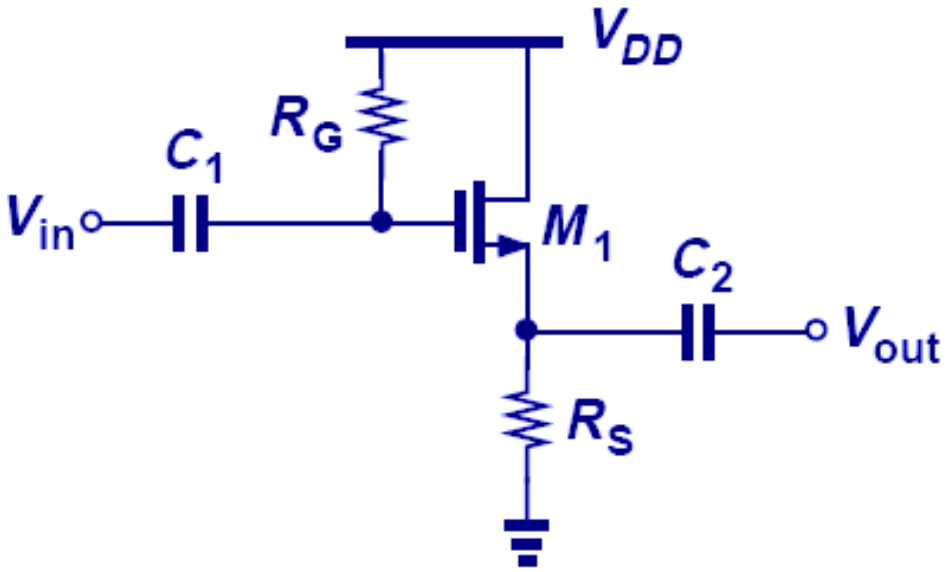


$$R_{out} = \frac{1}{g_m} \| r_O \| R_L \approx \frac{1}{g_m} \| R_L$$

$$R_o = \frac{1}{g_m} \| r_O + \frac{R_D}{1 + g_m r_O} \quad \text{if } R_D \neq 0$$

- **The output impedance of a source follower is relatively low, whereas the input impedance is infinite (at low frequencies); thus, a good candidate as a buffer.**

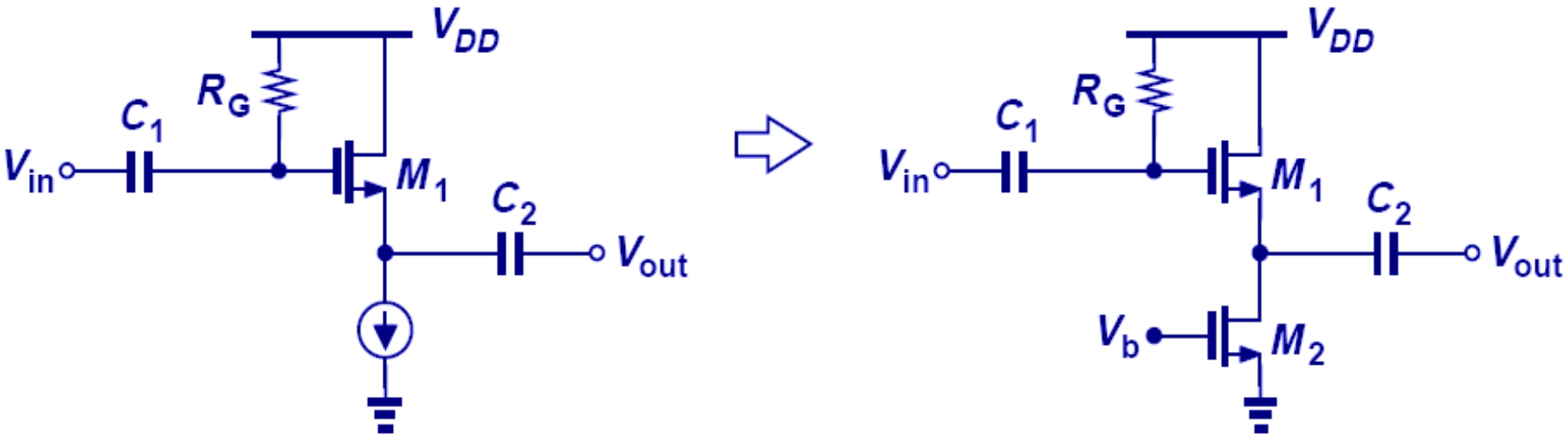
Source Follower with Biasing



$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{DD} - I_D R_S - V_{TH}\right)^2$$

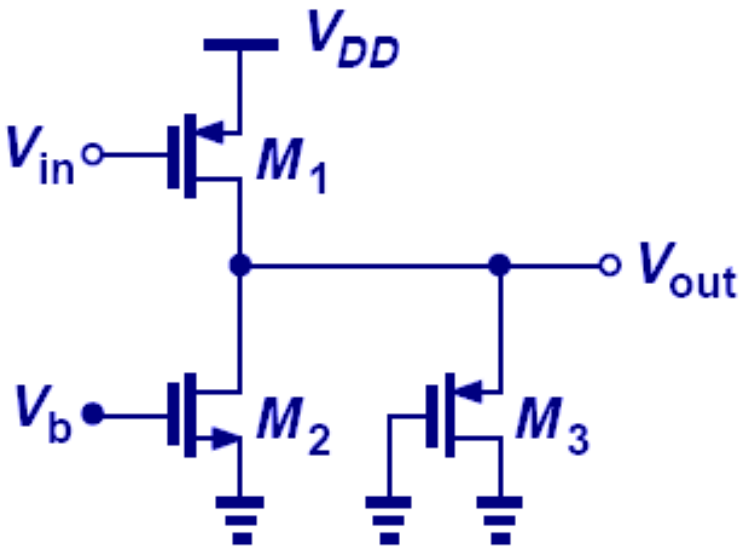
- R_G sets the gate voltage to V_{DD}, whereas R_S sets the drain current.
- The quadratic equation above can be solved for I_D.

Supply-Independent Biasing

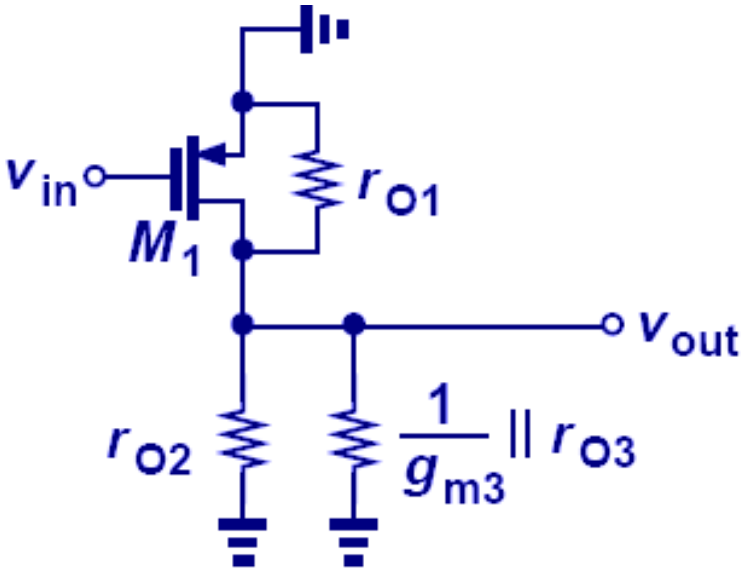


- If R_s is replaced by a current source, drain current I_D becomes independent of supply voltage.

Example of a CS Stage (I)



(a)



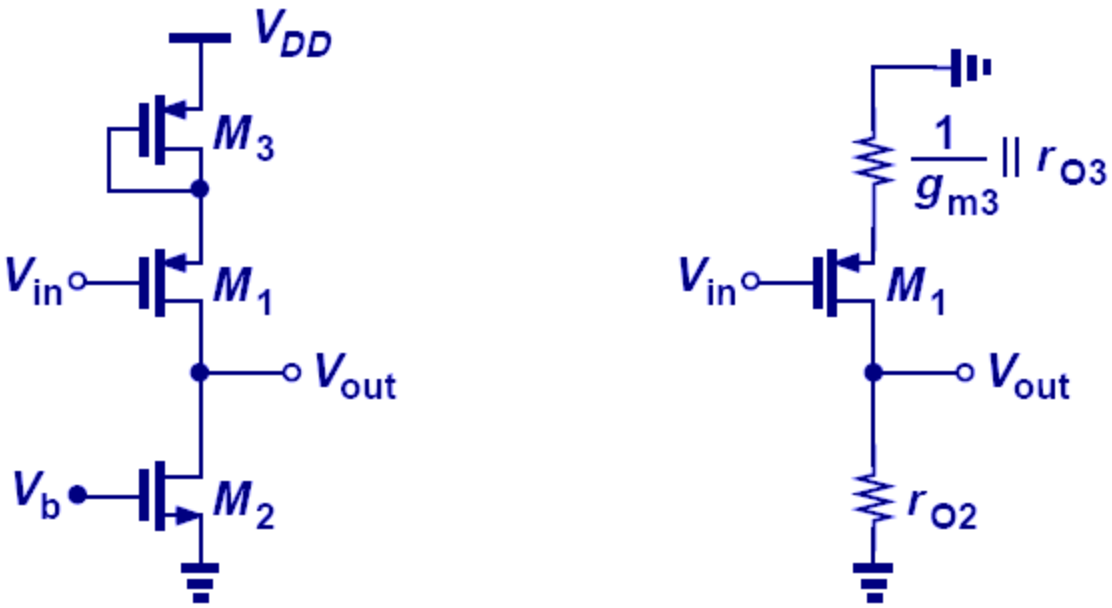
(b)

$$A_v = -g_{m1}\left(\frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}\right)$$

$$R_{out} = \frac{1}{g_{m3}} \| r_{O1} \| r_{O2} \| r_{O3}$$

- **M_1 acts as the input device and M_2, M_3 as the load.**

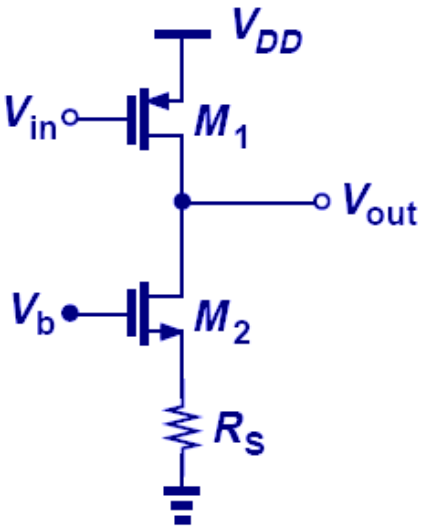
Example of a CS Stage (II)



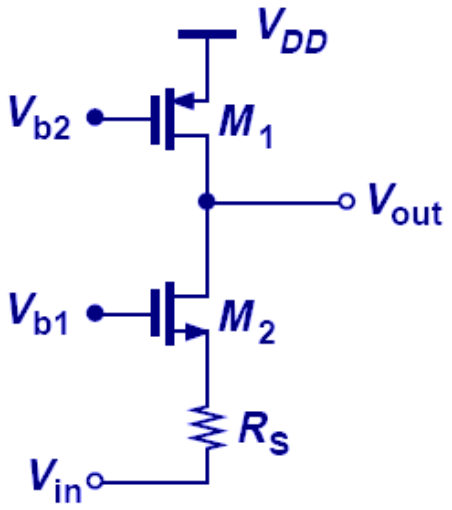
$$A_v = -\frac{r_{O2}}{\frac{1}{g_{m1}} + \frac{1}{g_{m3}} \| r_{O3}}$$

- **M_1 acts as the input device, M_3 as the source resistance, and M_2 as the load.**

Examples of CS and CG Stages



(a)



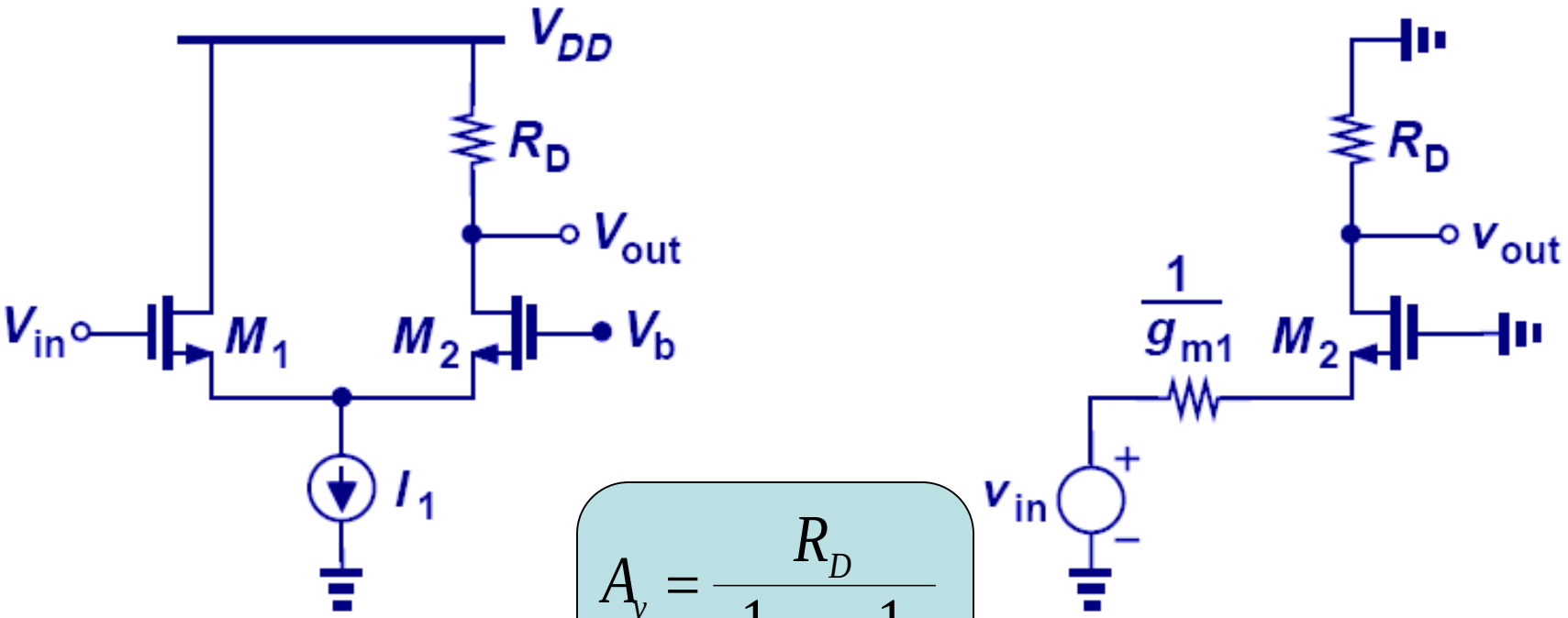
(b)

$$A_{v\_CS} = -g_{m1}\left[(1+g_{m2}r_{O2})R_S + r_{O2}\right] \| \, r_{O1}$$

$$A_{v\_CG} = \frac{r_{O1}}{\dfrac{1}{g_{m2}} + R_S}$$

- **With the input connected to different locations, the two circuits, although identical in other aspects, behave differently.**

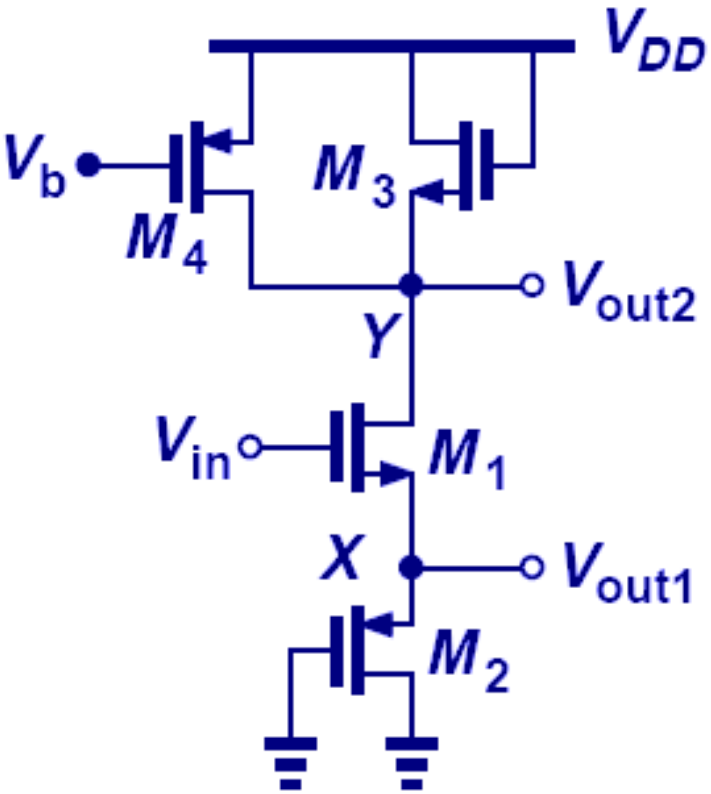
Example of a Composite Stage (I)



$$A_v = \frac{R_D}{\frac{1}{g_{m1}} + \frac{1}{g_{m2}}}$$

- **By replacing the left side with a Thevenin equivalent, and recognizing the right side is actually a CG stage, the voltage gain can be easily obtained.**

Example of a Composite Stage (II)



$$\frac{v_{out2}}{v_{in}} = -\frac{\frac{1}{g_{m3}} \| r_{O3} \| r_{O4}}{\frac{1}{g_{m2}} \| r_{O2} + \frac{1}{g_{m1}}}$$

- This example shows that by probing different places in a circuit, different types of output can be obtained.
- V_{out1} is a result of M_1 acting as a source follower whereas V_{out2} is a result of M_1 acting as a CS stage with degeneration.