Chapter 9 Cascode Stages and Current Mirrors

- 9.1 Cascode Stage
- 9.2 Current Mirrors
Boosted Output Impedances

\[ R_{out1} = \left[ 1 + g_m \left( R_E \parallel r_\pi \right) \right] r_O + R_E \parallel r_\pi \]

\[ R_{out2} = \left( 1 + g_m R_S \right) r_O + R_S \]
Bipolar Cascode Stage

\[ R_{out} = [1 + g_{m1}(r_{O2} \parallel r_{\pi1})]r_{O1} + r_{O2} \parallel r_{\pi1} \]

\[ R_{out} \approx g_{m1}r_{O1}(r_{O2} \parallel r_{\pi1}) \]
Example 9.1

If $Q_1$ and $Q_2$ in Fig.9.2(a) are biased at a collector current of 1mA, determine the output resistance. Assume $\beta = 100$ and $V_A = 5V$ for both transistors.

\[
g_m = \frac{I_C}{V_T}, \quad r_O = \frac{V_A}{I_C},
\]

\[
r_\pi = \frac{\beta V_T}{I_C}
\]

\[
R_{out} \approx \frac{I_{C1}}{V_T} \cdot \frac{V_{A1}}{I_{C1}} \cdot \frac{V_{A2}}{I_{C2} + \frac{\beta V_T}{I_{C1}}}
\]

\[
\approx \frac{1}{I_{C1}} \cdot \frac{V_A}{V_T} \cdot \frac{\beta V_A V_T}{V_A + \beta V_T},
\]

$I_C = I_{C1} = I_{C2}$ and $V_A = V_{A1} = V_{A2}$

$R_{out} \approx 328.9 \, k\Omega.$
The maximum output impedance of a bipolar cascode is bounded by the ever-present $r_\pi$ between emitter and ground of $Q_1$.

$$R_{\text{out, max}} \approx g_m r_0 r_{\pi 1}$$

$$R_{\text{out, max}} \approx \beta_1 r_{O1}$$
Example 9.2

Suppose in Example 9.1, the Early voltage of $Q_2$ is equal to 50V. Compare the resulting output impedance of the cascade with the upper bound given by Eq.(9.12).

Since $g_{m1} = (26 \ \Omega)^{-1}$, $r_{\pi 1} = 2.6 \ \text{k}\Omega$, $r_{O1} = 5 \ \text{k}\Omega$, and $r_{O2} = 50 \ \text{k}\Omega$, we have

$$R_{out} \approx g_{m1} r_{O1} (r_{O1} || r_{\pi 1})$$

$$\approx 475 \ \text{k}\Omega.$$

The upper bound is equal to 500 k\Omega, about 5% higher.
We wish to increase the output resistance of the bipolar cascade of Fig. 9.2(a) by a factor of two through the use of resistive degeneration in the emitter of $Q_2$. Determine the required value of the degeneration resistor if $Q_1$ and $Q_2$ are identical.

\[ R_{outA} = [1 + g_m(R_E||r_{\pi 2})]r_{O2} + R_E||r_{\pi 2}. \]

\[ R_{out} \approx g_m r_{O1}(R_{outA}||r_{\pi 1}). \]

\[ R_{outA}||r_{\pi 1} = 2(r_{O2}||r_{\pi 1}). \]

\[ R_{outA} = \frac{2r_{O2}r_{\pi 1}}{r_{\pi 1} - r_{O2}} \]

Typically $r_{\pi}$ is smaller than $r_O$, so in general it is impossible to double the output impedance by degenerating $Q_2$ with a resistor.
$$R_{out} = [1 + g_m (r_{O2} \parallel r_{\pi1})]r_{O1} + r_{O2} \parallel r_{\pi1}$$

$$R_{out} \approx g_m r_{O1} \left( r_{O2} \parallel r_{\pi1} \right)$$
Another Interpretation of Bipolar Cascode

Instead of treating cascode as $Q_2$ degenerating $Q_1$, we can also think of it as $Q_1$ stacking on top of $Q_2$ (current source) to boost $Q_2$’s output impedance.

$V_{b2}$ determines the current level.

$R_{out} \approx g_{m1} r_{o1} \left( r_{o2} \parallel r_{\pi1} \right)$
False Cascodes

When the emitter of Q₁ is connected to the emitter of Q₂, it’s no longer a cascode since Q₂ becomes a diode-connected device instead of a current source.

\[ R_{out} = \left[ 1 + g_{m1} \left( \frac{1}{g_{m2} \parallel r_{O2} \parallel r_{\pi1}} \right) \right] r_{O1} + \frac{1}{g_{m2} \parallel r_{O2} \parallel r_{\pi1}} \]

\[ R_{out} \approx \left( 1 + \frac{g_{m1}}{g_{m2}} \right) r_{O1} + \frac{1}{g_{m2}} \approx 2r_{O1} \]
MOS Cascode Stage

\[ R_{\text{out}} = (1 + g_{m1} r_{O2}) r_{O1} + r_{O2} \]

\[ R_{\text{out}} \approx g_{m1} r_{O1} r_{O2} \]
Example 9.5

Design an NMOS cascade for an output impedance of 500kΩ and a current of 0.5mA. For simplicity, assume $M_1$ and $M_2$ in Fig 9.8 are identical (they need not be). Assume $\mu_n C_{ox} = 100 \mu A/V^2$ and $\lambda = 0.1 V^{-1}$.

We must determine $W/L$ for both transistors such that

$$g_{m1} r_{O1} r_{O2} = 500 \text{ kΩ}.$$  

Since $r_{O1} = r_{O2} = (\lambda I_D)^{-1} = 20 \text{ kΩ}$, we require that $g_{m1} = (800 \text{ Ω})^{-1}$ and hence

$$\sqrt{2 \mu_n C_{ox} \frac{W}{L} I_D} = \frac{1}{800 \text{ Ω}}.$$  

It follows that

$$\frac{W}{L} = 15.6.$$  

We should also note that $g_{m1} r_{O1} = 25 \gg 1$. 

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Another Interpretation of MOS Cascode

- Similar to its bipolar counterpart, MOS cascode can be thought of as stacking a transistor on top of a current source.
- Unlike bipolar cascode, the output impedance is not limited by $\beta$.

$$R_{out} \approx g_{m1} r_{O1} r_{O2}$$

$R_{out} = r_{O2}$
PMOS Cascode Stage

\[ R_{out} = \left(1 + g_{m1} r_{O2}\right) r_{O1} + r_{O2} \]

\[ R_{out} \approx g_{m1} r_{O1} r_{O2} \]
Example 9.6

During manufacturing, a large parasitic resistor, \( R_P \), has appeared in a cascode as shown in Fig. 9.11. Determine the output resistance.

\( R_P \) is in parallel with \( r_{O1} \).

\[
R_{out} = g_{m1}(r_{O1} \parallel R_P)r_{O2}.
\]

If \( g_{m1}(r_{O1} \parallel R_P) \) is not much greater than unity, we return to the original equation, (9.22),

\[
R_{out} = (1 + g_{m1}r_{O2})(r_{O1} \parallel R_P) + r_{O2}
\]

\( R_P \) will lower the output impedance, since its parallel combination with \( r_{O1} \) will always be lower than \( r_{O1} \).
The short-circuit transconductance of a circuit measures its strength in converting input voltage to output current.

\[ G_m = \left. \frac{i_{out}}{v_{in}} \right|_{v_{out}=0} \]
Example 9.7

Calculate the transconductance of the CS stage shown in Fig. 9.13(a).

\[ G_m = \frac{i_{out}}{v_{in}} \]

\[ = \frac{i_{D1}}{v_{GS1}} \]

\[ = g_{m1} \]

\[ G_m = g_{m1} \]
Derivation of Voltage Gain

By representing a linear circuit with its Norton equivalent, the relationship between $V_{out}$ and $V_{in}$ can be expressed by the product of $G_{m}$ and $R_{out}$.

$$v_{out} = -i_{out} R_{out} = -G_{m} v_{in} R_{out}$$

$$v_{out}/v_{in} = -G_{m} R_{out}$$
Example 9.8

Determine the voltage gain of the common-emitter stage shown in Fig. 9.15(a).

\[ i_{\text{out}} \text{ is simply equal to the } g_{m1}v_{\text{in}}, \text{ i.e., } r_O \text{ does not carry a current} \]

\[ G_m = \frac{i_{\text{out}}}{v_{\text{in}}} \quad \Rightarrow \quad G_m = g_{m1}. \]

\[ R_{\text{out}} = \frac{v_X}{i_X} \quad \Rightarrow \quad R_{\text{out}} = r_{O1}. \]

It follows that

\[ A_v = -G_mR_{\text{out}} = -g_{m1}r_{O1}. \]
Comparison between Bipolar Cascode and CE Stage

Since the output impedance of bipolar cascode is higher than that of the CE stage, we would expect its voltage gain to be higher as well.
Voltage Gain of Bipolar Cascode Amplifier

Since $r_O$ is much larger than $1/g_m$, most of $I_{C,Q1}$ flows into the diode-connected $Q_2$. Using $R_{out}$ as before, $A_v$ is easily calculated.
Example 9.9

The bipolar cascade of Fig.9.16(b) is biased at a current of 1mA. If $V_A=5V$ and $\beta=100$ for both transistors, determine the voltage gain. Assume the load is an ideal current source.

$$g_{m1} = (26 \, \Omega)^{-1}, \, r_{\pi1} \approx r_{\pi2} \approx 2600 \, \Omega, \quad r_{O1} \approx r_{O2} = 5 \, k\Omega.$$ Thus,

$$g_{m1}(r_{O1} || r_{\pi2}) = 65.8$$

$$G_m \approx g_{m1}$$

$$A_v \approx -g_{m1}r_{O2}g_{m2}(r_{O1} || r_{\pi2})$$

$$|A_v| = 12,654.$$ 

Cascoding thus raises the voltage gain by a factor of 65.8.
A bipolar cascode amplifier is also a CE stage in series with a CB stage.
Since no current source can be ideal, the output impedance drops.

$$R_{out} \approx r_{O3} \parallel g_{m2}r_{O2}(r_{O1} \parallel r_{\pi2})$$
In order to preserve the high output impedance, a cascode PNP current source is used.

\[ R_{out} \approx g_{m3} r_{O3} \left( r_{O4} \parallel r_{\pi3} \right) \parallel g_{m2} r_{O2} \left( r_{O1} \parallel r_{\pi2} \right) \]
Example 9.10

Suppose the circuit of Example 9.9 incorporates a cascode load using $pnp$ transistors with $V_A = 4V$ and $\beta = 50$. What is the voltage gain?

\[ R_{on} \approx g_{m2}r_{O2}(r_{O1}||r_{\pi2}) \]
\[ R_{op} \approx g_{m3}r_{O3}(r_{O4}||r_{\pi3}). \]

The load transistors carry a collector current of approximately 1 mA. Thus,
\[ R_{op} = g_{m3}r_{O3}(r_{O4}||r_{\pi3}) \]
\[ = 151 \text{ k}\Omega \]
\[ R_{on} = 329 \text{ k}\Omega. \]
\[ |A_v| = g_{m1}(R_{on}||R_{op}) \]
\[ = 3,981. \]

Compared to the ideal current source case, the gain has fallen by approximately a factor of 3 because the $pnp$ devices suffer from a lower Early voltage and $\beta$. 
MOS Cascode Amplifier

\[ A_v = -G_m R_{out} \]

\[ A_v \approx -g_{m1} \left[ (1 + g_{m2}r_{O2})r_{O1} + r_{O2} \right] \]

\[ A_v \approx -g_{m1}r_{O1}g_{m2}r_{O2} \]
Improved MOS Cascode Amplifier

- Similar to its bipolar counterpart, the output impedance of a MOS cascode amplifier can be improved by using a PMOS cascode current source.

\[ R_{on} \approx g_{m2}r_{O2}r_{O1} \]
\[ R_{op} \approx g_{m3}r_{O3}r_{O4} \]
\[ R_{out} = R_{on} \parallel R_{op} \]
Temperature and Supply Dependence of Bias Current

Since $V_T$, $I_S$, $\mu_n$, and $V_{TH}$ all depend on temperature, $I_1$ for both bipolar and MOS depends on temperature and supply.

For bipolar transistor $Q_1$:

\[
R_2 V_{CC} / (R_1 + R_2) - I_1 / \beta \cdot (R_1 \parallel R_2) = V_T \ln(I_1 / I_S)
\]

For MOS transistor $M_1$:

\[
I_1 = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left( \frac{R_2}{R_1 + R_2} V_{DD} - V_{TH} \right)^2
\]
The motivation behind a current mirror is to sense the current from a “golden current source” and duplicate this “golden current” to other locations.
The diode-connected \( Q_{REF} \) produces an output voltage \( V_1 \) that forces \( I_{copy1} = I_{REF} \), if \( Q_1 = Q_{REF} \).
Without shorting the collector and base of $Q_{REF}$ together, there will not be a path for the base currents to flow, therefore, $I_{copy}$ is zero.
Although a path for base currents exists, this technique of biasing is no better than resistive divider.
Multiple copies of $I_{REF}$ can be generated at different locations by simply applying the idea of current mirror to more transistors.

\[ I_{\text{copy}, j} = \frac{I_{S,j}}{I_{S,REF}} I_{REF} \]
By scaling the emitter area of $Q_j$ $n$ times with respect to $Q_{REF}$, $I_{copy,j}$ is also $n$ times larger than $I_{REF}$. This is equivalent to placing $n$ unit-size transistors in parallel.

$$I_{copy,j} = nI_{REF}$$
Example 9.14: Scaled Current

A multistage amplifier incorporates two current sources of values 0.75mA and 0.5mA. Using a bandgap reference current of 0.25mA, design the required current sources. Neglect the effect of the base current for now.
Fractional Scaling

- A fraction of $I_{REF}$ can be created on $Q_1$ by scaling up the emitter area of $Q_{REF}$.

$$I_{copy} = \frac{1}{3} I_{REF}$$
Example 9.15 : Different Mirroring Ratio

- It is desired to generate two currents equal to 50uA and 500uA from a reference of 200uA. Design the current mirror circuit.

- Using the idea of current scaling and fractional scaling, $I_{\text{copy}2}$ is 0.5mA and $I_{\text{copy}1}$ is 0.05mA respectively. All coming from a source of 0.2mA.
Mirroring Error Due to Base Currents

\[ I_{\text{copy}} = \frac{nI_{\text{REF}}}{1 + \frac{1}{\beta} (n+1)} \]

In the circuit diagram, \( V_{CC} \) is connected to the top of the transistor \( Q_{REF} \), and \( I_{\text{REF}} \) flows through it. The current \( I_{\text{copy}} \) is mirrored through two transistors \( Q_{REF} \) and \( Q_1 \), with the base currents affecting the mirroring accuracy.
Improved Mirroring Accuracy

Because of $Q_F$, the base currents of $Q_{REF}$ and $Q_1$ are mostly supplied by $Q_F$ rather than $I_{REF}$. Mirroring error is reduced $\beta$ times.

$$I_{copy} = \frac{nI_{REF}}{1 + \frac{1}{\beta^2(n+1)}}$$
Example 9.16: Different Mirroring Ratio Accuracy

- Compute the $I_{\text{copy}1}$ and $I_{\text{copy}2}$ in this figure before and after adding a follower.

Before:

\[
I_{\text{copy}1} = \frac{I_{\text{REF}}}{4 + \frac{15}{\beta}}
\]

\[
I_{\text{copy}2} = \frac{10I_{\text{REF}}}{4 + \frac{15}{\beta}}
\]

After:

\[
I_{\text{copy}1} = \frac{I_{\text{REF}}}{4 + \frac{15}{\beta^2}}
\]

\[
I_{\text{copy}2} = \frac{10I_{\text{REF}}}{4 + \frac{15}{\beta^2}}
\]
Example 9.17: Different Mirroring Ratio Accuracy

Design this circuit for a voltage gain 100 and a power budget of 2mW. Assume $V_{A,npn} = 5V$, $V_{A,pnp} = 4V$, $I_{REF} = 100uA$, and $V_{CC} = 2.5V$.

$$A_v = -g_{m1} \frac{r_{O1}}{r_{O2}}$$

$$= - \frac{1}{V_T} \cdot \frac{V_{A,npn} V_{A,pnp}}{V_{A,npn} + V_{A,pnp}}$$

$$= -85.5.$$  

The gain is smaller than 100 because low Early voltages and $V_T$, a fundamental constant of the technology, independent of the bias current.
PNP current mirror is used as a current source load to an NPN amplifier stage.
Generation of $I_{\text{REF}}$ for PNP Current Mirror

\[ I_{\text{REF}} \quad Q_{\text{REF1}} \quad Q_{\text{REF2}} \quad Q_1 \quad Q_2 \]

\[ I_{C,M} \quad X_1 \quad X_2 \quad V_{\text{CC}} \quad V_{\text{out}} \quad v_{\text{in}} \]
Let $Q_{REF}$ and $Q_1$ be discrete NPN devices. $I_{REF}$ and $I_{copy1}$ can vary in large magnitude due to $I_S$ mismatch.
The same concept of current mirror can be applied to MOS transistors as well.
Bad MOS Current Mirror Example

- This is not a current mirror since the relationship between \( V_X \) and \( I_{REF} \) is not clearly defined.
- The only way to clearly define \( V_X \) with \( I_{REF} \) is to use a diode-connected MOS since it provides square-law I-V relationship.
Example 9.20: Current Mirror?

Is this current mirror? Explain what happens.

This circuit is not a current mirror because the gates of $M_{REF}$ and $M_{1}$ are floating.
Example 9.21: Current Scaling

Similar to their bipolar counterpart, MOS current mirrors can also scale $I_{\text{REF}}$ up or down ($I_1 = 0.2\text{mA}$, $I_2 = 0.5\text{mA}$).
The idea of combining NMOS and PMOS to produce CMOS current mirror is shown above.