Analog Electronic Circuits
Department of Electrical and Computer Engineering
Seoul National University

2014 Fall D.K. Jeong

PSPICE Assignments #4

- Due: 2014/12/03(Wed) 3:30 PM
- Submit a hardcopy report.
- For any questions, send an e-mail to jhhwang@isdl.snu.ac.kr

1. Use the Model listed below. It is all included in the basic library.
The emitter follower of Fig.2 must be designed to drive R_L=4 ohms with a voltage gain of 0.8. Use Q2N2222 model for NPN bipolar junction transistor model. Use IDC (Ideal Current Source) for I_1.
V_{CC}=1.8V, V_{EE}=0V, $V_{BE,on}$=0.8V, I_S=7.3X10^{-15}A, V_A=∞, β>100.

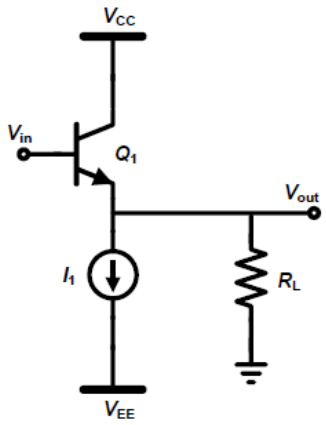
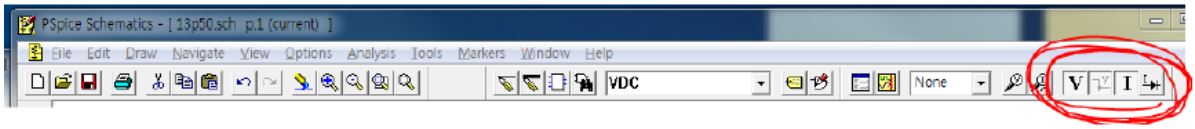


Fig.2

a) Assuming I_{C1}=I_1, find I_1 that make the circuit satisfy the given voltage gain condition.
b) Assuming V_{in} is limited by V_{CC} and V_{EE} (i.e. 0~1.8V), find the followings.
1) V_{out} range,
2) the most reasonable offset voltage value for V_{out}, (HINT: When output range is 0~400mV, the most reasonable offset voltage would be 200mV to have the maximum swing.)
3) input offset voltage when taking the result from 2) into account,
4) input swing when taking voltage gain and the result from 1) into consideration.
5) Verify 2) and 3) using Bias Voltage/Current Display from the button shown below.



c) By using VSIN to have sinusoidal voltage input, show that the required conditions from a) and b) are satisfied. You may use 'transient' simulation. You need to set proper VOFF(=offset), VAMPL(=amplitude) and FREQ(=frequency) values for VSIN.

<End of PSPICE Assginments #4>