Special Topics on Communication: FPGA based Communication System Design

Homework #1

Due: March 25th(Tue) before class begins Prof. Wonyong Sung

This homework is a basic exercise of Simulink using an AM (amplitude modulation) system. This problem seems simple, but will be advanced to more complex ones, such as including the carrier recovery and low-complexity lowpass filtering, next time.

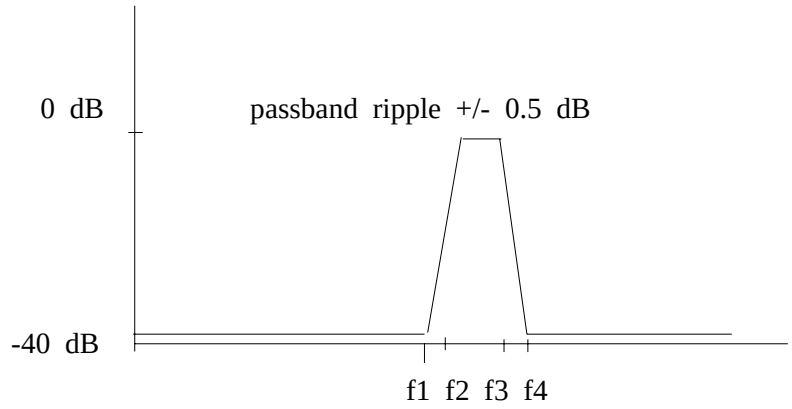
Before doing this homework, you should read the material for lab1, lab2, and lab3, which I downloaded from University of Toronto. This material shows step by step introductions to Simulink including the filter design software. However, there is a difference. These downloaded lab materials are intended to implement communication algorithms using Texas Instruments' programmable digital signal processors, for which the Code Composer Studio is used as the tool for implementation. We will instead use the System Generator for FPGA based implementation. Anyway, you do not need to use System Generator for doing this homework. Just, Simulink is OK. I asked our department to install the Simulink at the computer lab. As for the data type, this homework is intended for algorithm simulation, so floating-point would be OK.

1. Study AM (amplitude modulation), especially AM signal generation and demodulation method. You need to explain the ordinary AM-DSB (which has double side bands with enough strength of carrier so that envelope detection (with diode) is possible), AM-DSB-SC (suppressed carrier), AM-SSB (single side band which has only one sideband, no carrier). Please discuss the spectral efficiency, power efficiency, and demodulation complexity of these methods.

2. Develop a Simulink based design of AM-DSB modulator as given in page 1~3 of lab3 material. As for the message signal, use a 1.5 KHz 0.5 peak Voltage (1Vpp) sinusoid, and the carrier is 1 peak Voltage, 12 KHz, sinusoid. Use 48KHz as the sampling rate of this system. You need to show (a) your Simulink based design of your AM-DSB, (2) time-domain results that shows all three signals (message, modulation signal, output signal), (3) frequency domain results of all three signals.

3. Develop an AM-DSB-SC modulator using Simulink, and show the results at the same way. You need to show your Simulink based design, time-domain, and frequency domain plots. You may just need to change the above design very slightly.

4. Develop an AM-SSB modulator using Simulink. There are a few methods for generating SSB signal. Here you try to use a bandpass filter. The filter specification that I suggest is a bandpass filter having the following specification. This filter is designed assuming that the message signal has the frequency range of 0.2KHz ~ 3.8KHz.



f1: stopband edge: 11.8KHz

f2: passband edge: 12.2KHz

f3: passband edge: 15.8KHz

f4: stopband edge: 16.2KHz

Passband ripple: -0.5dB~+0.5dB, stopband attenuation: 40dB

To do this problem, you first need to design a filter using Matlab.

5. Develop an envelope detector for AM-DSB using Simulink, and show the results at the same way. As for the envelope detector, this does not mean that you use a diode. You try to use a DSP block that can conduct envelope detection - one possible way is to take the absolute value and then apply lowpass filtering. The message signal has the frequency range of 0.2KHz ~ 3.8KHz. You may need to design a filter.

6. Check if your detector also works with AM-DSB-SC. You just add your detector to the AM-DSB-SC, and observe the results.

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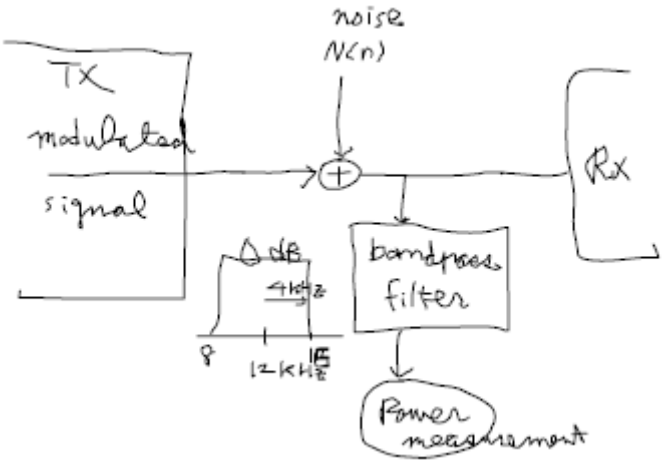
Homework #2

Due: April 8th(Tue) before class begins.

Prof. Wonyong Sung

This homework is the continuation of the previous AM modulation/demodulation examples.
In this problem, we will consider the SNR (Signal to Noise power Ratio) in the channel and that in the demodulator in the AM scheme. Note that a good communication system should yield high SNR at the demodulator even with weak signal at the channel (or low SNR in the channel). At the DSB-AM modulator/demodulator (HW#1, Prob. 5), you add the channel noise and signal measurement block at the output of the modulator (this corresponds to the channel). This looks like as follows.



We add noise to the output of the transmitter. The noise is random Gaussian with the r.m.s. (root mean square) value of 0.01. You should be able to find this noise generation block at the Simulink.
1. Measure the signal power at the channel. To meausre the signal power, you set the noise power as '0.0,' and measure the bandpass filtered signal power. The bandpass filter should pass 8.2 KHz to 15.8 KHz signal with the gain of 0 dB. You can choose the stopband attenuation and transition bandwidth with some reasonable one. Here you need a power measurement block (I'm not sure if this is in the Simulink block). If not, you can simply make it by designing a block that calculates the mean square value of the input.
Your answer should contain: (i) the filter design result, (ii) the power measurement block in Simulink or Matlab code, if not supported at the library, (iii) measured signal power.

2. Measure the noise power at the channel. At the similar way, you set the signal power to zero, but apply the noise with the rms value of 0.01, and measure the bandpass filtered noise power using the power measurement block. If you are clever enough, you can guess the value of the filtered noise power without simulation. If you can derive this in analysis, please note the derivation and discuss if the two (measured and analyzed) are the same.

3. From the results of (a) and (b), please calculate the SNR (Signal to Noise Ratio) in the channel.

4. You demodulate the signal using the envelope detector, and measure the SNR (signal and the noise

power). Of course, you can use the envelope detector you already developed. Here, you need to filter the demodulated signal with the lowpass filter of 0.2KHz ~ 3.8KHz. Since the envelope detection process is a non-linear process, I suggest you to calculate the signal and noise power at the spectral domain. The signal frequency will be near 1 KHz, while the other components are something low level but spreaded at the entire frequency range of 0.2 ~ 3.8KHz. The noise power can be calculated by summing the square of all the frequency components except for the 1.0 KHz component.

5. You demodulate the signal using the carrier (synchronous detector), not the envelope detection. Here you assume that you can use the same carrier used for modulation (we skip the carrier recovery process now). Find the SNR of the demodulated signal in this case.

6. Is there any SNR difference of the two, envelope and synchronous detection, methods? Please consult any communication texts to support your finding, and explain if they (the text and the experiments) are the same or different.

7. You do the same thing (1~6) for the DSB-SC (double side band - suppressed carrier) modulator/demodulator. Of course, you cannot use the envelope detector. You just use the synchronous detection. Here you need to answer (1) SNR measured in the channel (2) SNR measured in the demodulator.

8. You do the same thing (1~6) for the SSB modulator/demodulator. You should use the synchronous detector. The bandpass filter for the measurement of the channel signal and the noise should be redesigned, it needs to pass 12.2KHz ~ 15.8KHz. Here you need to answer (1) SNR measured in the channel (2) SNR measured in the demodulator.

9. Discuss what you have found when you compare the DSB-AM, DSB-SC and the SSB schemes. You should explain the difference of the SNR measured in the channel and that in the demodulator. Which one is better, and the worst? Where is the difference originated from? Please consult any communication texts to support your explanation.

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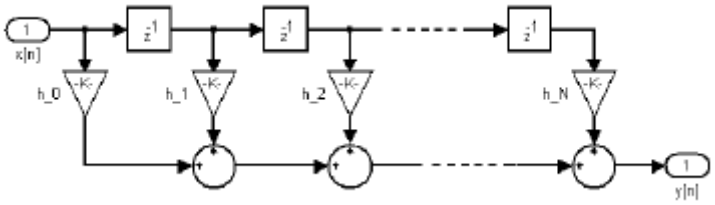
Homework #3

Due: April 24th(Thu) before class begins. Doing this homework is exactly preparing your quiz.

Prof. Wonyong Sung

1. We have a digital FIR filter having a following structure.



a) Please design a lowpass FIR filter having a stopband ripple of -30dB, passband ripple 2 dB, wp = 0.2 π, ws = 0.4π. Please generate floating-point coefficients in Matlab. The sampling frequency is asssumed as 48KHz.

b) You round the coefficients so that they have the word-length of 4 bits, 8bits, and 12bits. You'd better make a simple program for coefficients rounding. You need to give the same binary-points to all the coefficients - hence the largest coefficient value determines the binary-point; this is convenient for time-multiplexed hardware implementation. Then, you draw the filter responses (for 4bits, 8bits, 12 bits) using the rounded coefficients.

(Example: assume h0 = 0.24, h1 = -0.49, h2 = 0.02 -> 4bits ->

The integer wordlength with this example is -1 since h1 is less than 2^{-1}.

This means the weight of the 4bit number is (-1/2 for sign, 1/4, 1/8, 1/16)

0.24 => (0, 0, 1, 1) real value = 0.1874

-0.49 => (1, 0, 0, 0) real value = -0.5

end of Example)

c) Assume that the input is between -1 to 1 (the range of 1). What is the maximum possible range of the output? Then what is the integer word-length of the adders? We assume to assign the same word-length/integer word-length to all the adders for time-multiplexed implementations.

d) Please apply an input speech sample represented in the fractional format (the range is between -1 to 1). What is the output range when you simulate it in Matlab. The input file is given at the website. What is the integer word-length of the adders? Note that give the same integer word-length to all the adders.

e) With the range information obtained in c, please design an FIR filter with full-array architecture. Use 8-bit for the coefficients. So, the multipliers you use will be 8bit signed x 16bit signed, which result in 23 bits signed output. Please use 24 bits for the adder. You need to exactly give how the output bits of the multipliers are connected to that of the adders.

f) With the range information obtained in c, please design an FIR filter with a time-multiplexed implementation (you just need to use one multiplier and one adder). What is your system clock frequency?

2. You do the same work (a ~ e, not f) assuming that your design is based on the direct form IIR filter.

3. Please retime your direct form IIR filter so that it has the minimum critical delay for a full array implementation.

4. You are going to implement two same FIR filters having the specification shown in Prob. 1, for the application to stereo audio processing. Please design a time-multiplexed implementation (similar to 1-f, but need to process stereo) that uses only one multiplier and one adder for stereo processing. What is the system clock frequency of your filter?

5. You need to implement an 8 channel IIR filter having the same characteristic with the IIR filter you have designed in Prob. 2. By adding some more registers and switches to your full array IIR filter, please develop the hardware for an 8 channel IIR filter. What is your system clock frequency? You do not need to show the exact bit-positions; this problem is focused on interleaved hardware design, not fixed-point conversion.

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Homework #4

Due: May 8th(Thu) before class begins.

Prof. Wonyong Sung

This homework is the continuation of the previous AM modulation/demodulation examples. In Prob. 1 ~ 3, we will observe the finite word-length effects of ADC and other digital circuits. Prob. 4 is for designing a PLL.

In HW1 and 2 we already have developed a Simulink based design of AM-DSB modulator/demodulator. (Detailed specifications: As for the message signal, use a 1.5 KHz 0.5 peak Voltage (1Vpp) sinusoid, and the carrier is 1 peak Voltage, 12 KHz, sinusoid. Use 48KHz as the sampling rate of this system.).

1. (This is the extension of HW2 - Prob. 7) We will check the effects of ADC resolution for the synchronous detection of DSB-SC signal.
- Build a DSB-SC modulator in Simulink (you already have done it).
- Do not add noise at the channel.
- First develop a floating-point version of the demodulator (you use the same carrier used at the modulator). And, store the demodulated signal at a file (this will be called the 'reference demodulation').
- Then, add an 8-bit quantizer (this models 8bit Analog to Digital Converter) at the forefront of the demodulator. And conduct floating-point processing for the rest of the demodulator. Then, compare the demodulated signal with the 'reference demodulation' in terms of SNR (Signal to Noise Ratio). The noise here is due to the 8bit ADC. Now, increase the 8-bit ADC to 10-bit ADC, and obtain the SNR again. You need to consider scaling when using the quantizer (format converter).

2. (a) Now, you remove the 8-bit quantizer (just directly connect) to ignore the effects of the ADC. And, implement the demodulator using 8-bit multiplications and 16-bit additions. Then, conduct demodulation (fixed-point processing) and compare the results with the 'reference demodulation' in terms of SNR (Signal to Noise Ratio). Please scale appropriately. What is the SNR?
(b) What is the SNR if you use 10-bit multiplications and 20-bit additions.

3. Now observe the SNR when you use 10-bit ADC, 10-bit multiplications, and 20-bit additions.

4. Please develop a PLL based carrier recovery circuit for the use in the AM-DSB demodulator. Please do not directly use the PLL block, but you can use sine, cosine function blocks as well as multiplication, addition and delay blocks. Please use a simple low pass filter, and try to observe the locking time when you change the parameters. Please use floating-point arithmetic.

1. (a) Calculate the number of multiplications per second for the implementation of the bandpass filter for SSB generation at the previous homework. This can be easily calculated by considering the sampling frequency, the filter order, and the structure (linear phase or not).

(b) Now assume that the carrier frequency is increased to 1,000 KHz (and the sampling frequency is 4,000 KHz). Please design a bandpass filter for SSB generation, and then calculates the number of multiplications per second.