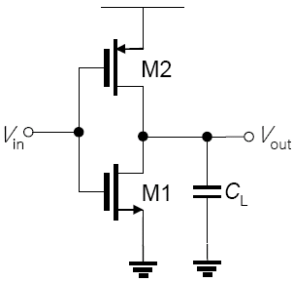
Quiz 12	Subject	Professor	Student ID#	Student Name	Score
Date: 2009.12.02	Microelectronics 2	Jong-Ho Lee			

1. Following figure depicts a CMOS inverter. Assume both transistors M1 and M2 have exactly the same current drivability and the same threshold voltage. Answer for the following questions.



$$I_{D,lin} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]$$

$$I_{D,sat} = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_{TH})^2$$

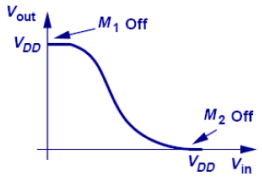
(a) Briefly describe the advantage of a CMOS inverter compared to an NMOS inverter which is composed of NMOS FET and a load resistance. (4)

Answer)

A CMOS inverter has following advantages.

i) The output low level is exactly equal to zero because $V_{in}=V_{DD}$ ensures that M_2 remains off.

ii) The circuit consumes zero static power for both high and low output levels.



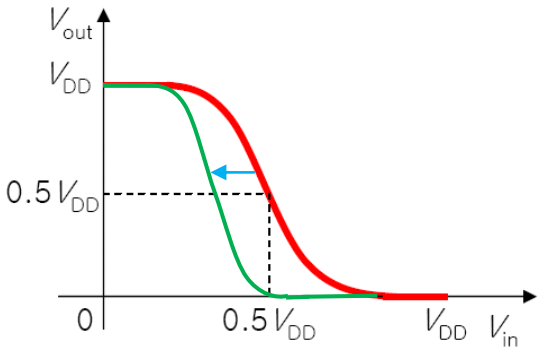
However, a NMOS inverter has drawbacks from the passive nature of the load resister.

i) M_1 must "fight" R_D while establishing a low level at the output node and hence R_{on1} must remain much smaller than R_D.

ii) After M_1 turns off, only R_D can pull the output node up toward V_{DD}.

iii) The circuit draws a current of approximately V_{DD}/R_{DD} from the supply when the output is low.

(b) When the channel width (W) of M1 is doubled, sketch schematically the behavior of the VTC curve shown below. And explain briefly the reason. (3)



Answer)

Both M_1 and M_2 operate in saturation around the trip point.

When the width of M_1(W) is doubled, NMOS device is made stronger. Therefore, the circuit requires a lower input voltage to establish $I_{D1} = |I_{D2}|$.

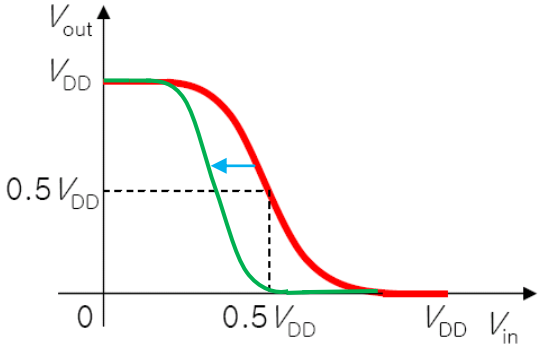
$$\frac{1}{2}\mu_n C_{ox}\left(\frac{2W}{L}\right)_1 (V_{in} - V_{TH1})^2(1+\lambda_1 V_{out})$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{in} - |V_{TH2}|)^2[(1+\lambda_2(V_{DD} - V_{out})]$$

For $V_{out} = V_{DD}/2$, as $(W/L)_1$ increases, V_{in} must also decrease so that $(V_{DD} - V_{in} - |V_{TH2}|)^2$ on the right-hand side increases and $(V_{in} - V_{TH1})^2$ on the left-hand side decreases.

Moreover, the current drive of M2 increases and the circuit therefore exhibits a faster falling transition($1/2R_{on1}$). Consequently, the characteristic is shifted to the left and the fall time is halved.

(c) An NMOS FET which has the same current drivability as that of M1 is connected between the output terminal and the ground. Now sketch schematically the behavior of the VTC curve shown below. And explain briefly the reason. (3)



Answer)

$$\frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{TH1})^2(1+\lambda_1 V_{out}) + \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_3 (V_{in} - V_{TH3})^2(1+\lambda_3 V_{out})$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{DD} - V_{in} - |V_{TH2}|)^2[(1+\lambda_2(V_{DD} - V_{out})]$$

$$\left[\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_3, V_{TH1} = V_{TH3}, \lambda_1 = \lambda_3\right]$$

This circuit requires a lower input voltage to establish $I_{D1}+I_{D3} = |I_{D2}|$ around the trip point. This case is the same as problem 1.(b) because adding one more NMOS FET connected with M1 in parallel shows the same effect as doubling the channel width of M1(2W) .

Use front side only