Special Topics on Communication: FPGA based Communication System Design

March 18, 2008 [20 minutes]   Prof. Wonyong Sung

1. The NRE (non Recurring Engineering) cost for VLSI development with 90nm technology is about $1million. This will increase to $1.5M with 60nm. The chip cost for each will be $10 with 90nm, and it is down to $7 with 60nm. The chip cost of FPGA will be about 10 times higher, but it needs no NRE. What would be the minimum quantities of devices to choose custom VLSI based designs, instead of FPGA, in 90nm and 60nm, respectively?

Ans: 90nm: ASIC cost $1,000,000 + 10 x$ $>= 100 x$ <- FPGA cost

$$x >= 11,111$$

   60nm: $1,500,000 + 7x >= 70x$

$$x >= 23,809$$

2. We are going to implement a 128 tap digital filter supporting about 16MHz sampling rate, while using a system clock of 128MHz. Please give the digital filter using (1) behavioral description (2) RTL description. The design does not need to be very accurate; you just need to show the approximate behavioral and RTL designs.

Ans: <u>Behavioral description</u>: a signal flow graph of a 128 tap FIR filter containing 127 z-1(sample delay) and 128 multiplication operations.

<u>RTL description</u>: time-multiplexing factor = 128M/16M = 8

     The number of multipliers needed = 128 tap / 8 time multiplexing = 16

You use 16 hardware multipliers, each z^{-1} is replaced by 8-tap shift registers.

3. In FPGA based system implementation, you have three choices for memory: distributed RAM, block RAM, external DRAM. Please compare them in terms of bandwidth and available memory capacity.

Ans: distributed RAM: highest bandwidth, but very limited size memory capacity.

     Block RAM: medium bandwidth, fairly good capacity.

     external DRAM: low bandwidth, very large capacity.

4. Please show the <u>approximate</u> plot (graph) that the following Matlab code would make. I am suggesting you to find out the pole and zero locations of the given function.
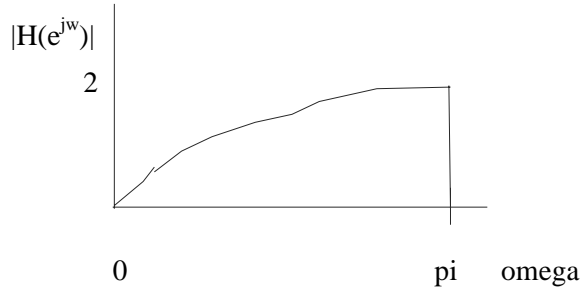
```
>> num=[1.0 0.0 -1.0];
>> den=[1.0 0.9999];
>> om=[0:pi/256:pi];
>> H=freqz(num,den,om);
>> figure(1)
>> plot(om/pi,abs(H),'LineWidth',2)
>> xlabel(' \omega/ \pi')
>> ylabel('|H(e^ {j \omega })|')
```

$H(z) = (1-z^{-2})/(1+0.9999z^{-1}) =\sim 1-z^{-1}$

This has no gain in when w = 0, or D.C. ($z^{-1} = 1$), has a gain of 2 when w = pi.
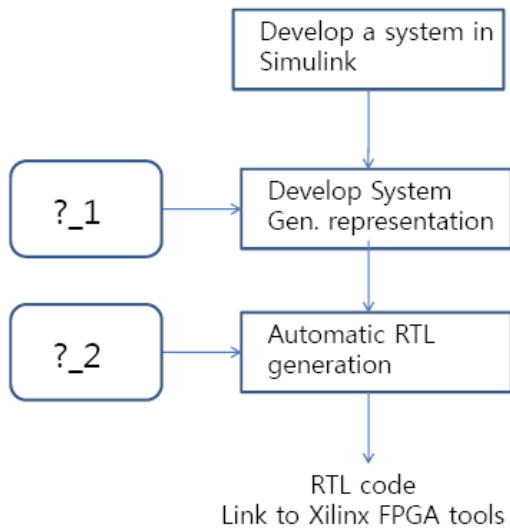
Quiz #2

Special Topics on Communication: FPGA based Communication System Design

April 8, 2008 [20 minutes]   Prof. Wonyong Sung

1.   The figure below shows the model-based communication system design flow for Xilinx FPGA, starting from Simulink. Please fill in the appropriate terms for [?_1] and [?_2] in this figure.

Answer: ?_1 (Xilinx) DSP blockset,   ?_2 Xilinx Coregen

2. (a) What are the advantages of the model based design (top-down design flow) when compared with the down-top based design? Please give two or three answers.   (b) What are the disadvantages, if any? You need to answer at least one. Note that these are not appropriate answers, e.g. 'We need expensive tools. We need to learn some other tools. Our design is tied to some specific tools.'
(a) 1. Top level design is more conceptual and algorithm oriented, with less details. So, you can quickly try different algorithms and check the performance by manipulating smaller number of functional blocks. Because of the similar reason, the top-level design requires less time for simulation. 2. The down-level design involves much detailed description in hardware, so it is desired to generate the down-level designs automatically from the high-level designs. 3. You can try different implementations, such as using TI VLIW programmable DSP, Xilinx FPGA, Altera FPGA, or TSMC ASIC, from one top level design. (b) When you have existing hardware, it would not be bad to implement some additional hardware to the existing one.

3.   We want to design a multiplierless filter using a comb filter structure.   Please develop a multiplierless filter having the frequency response shown below. Note that this is a high-pass filter. X-axis represent the angular frequency in the sampled signal domain (2pi corresponds to the sampling frequency). You should give the exact number of delays, if needed.

Comb filter order = 16.   The integrator should have a pole at w=pi.
So, $H(z) = (1-z^{-16})/(1+z^{-1})$

Magnitude
response
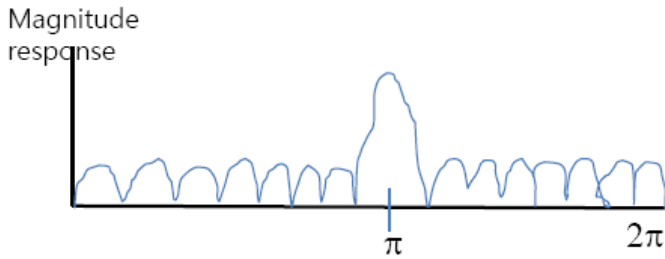
4. We have a video signal whose bandwidth is from 0 to 4.5MHz, and this video is originally sampled at 10MHz. Now we need to increase the sampling rate to 40MHz (four times sampling rate increase).
(a) What is the filter order (assume linear phase FIR filter) for the sampling rate change. We assume that the needed filter order is determined as $N_{FIR} = 2 * f_{sampling} / (f_{stop} - f_{pass})$.
You first need to determine the transition bandwidth (fstop-fpass) of the filter.

Answer) The spectrum after inserting 3 zeros between the input samples is as follows.
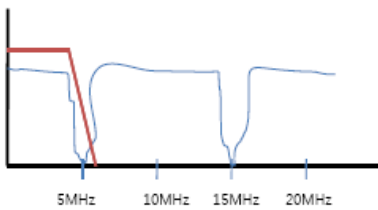
The filter specification: fsampling = 40MHz, fpass = 4.5MHz, fstop = 5.5Mz -> N (filter order) = 80.

(b) How many 'multiplications per second' do we need for the sampling rate change? Do not count the unneeded multiplications.
Answer) You cannot utilize the linear filter property because the location of zero input samples are not symmetric. Anyway, among 80 taps, only 20 taps are not zeroes.
So, the number of multiplications per second = 20*40M (Hz) = 80M multiplications per second.
(Some students may consider that fpass = 4.5MHz, fstop=5MHz -> N =160. 160M multiplications per second. This answer is also regarded 'right' one.)

Special Topics on Communication: FPGA based Communication System Design

April 29th, 2008 [20 minutes]   Prof. Wonyong Sung

4차 IIR 필터
4th order IIR filter

1. [10 points] What is the maximum operating clock frequency of the 4th order IIR filter shown above when this filter is implemented in the full-array architecture as shown exactly in the signal flow graph. You first need to figure out the critical path. Please assume that the delay of the multiplier is 10ns, that of the adder is 5ns, but ignore the delay of flip-flops and interconnections.

Answer: Critical path: M3->A2->A1->M4->A3->a5->M9->A7   55ns -> 18.18 MHz

2. [10 points] Please retime the above signal flow graph so that you can maximize the operating clock frequency. Please use the cut-set retiming, which is the simplest method. Please show the retimed signal flow graph and the operating clock frequency.   Ans: D1, D3 are removed. Instead 6 Delays are added (at the outputs of A1, M5, M6, A5, M10, M11). Critical path: M3->A2->A1   20ns -> 50MHz.

3. [10 points + 10 points bonus] You are going to implement the 4th order IIR filter for stereo channels. Please show the hardware block diagram by modifying the design in Prob. 1.

Answer: add a multiplexer at the input, add a demux at the output, D1, D2, D3, D4 -> change each

delay into two delays.

[Extra question for bonus] Please apply retiming to your above answer to maximize the operating clock frequency. Then, what is the operating clock frequency?
Answer: We can conduct retiming further because there are two delays at the location of D1, D2, D3, D4. New delays are added by new retiming at the output of M2, M3, A4, M4, A4, ...
The critical path delay is 10ns (just M2 or A2->A1). We need to insert a delay at the output of M1.
Max operating freq is 100MHz.
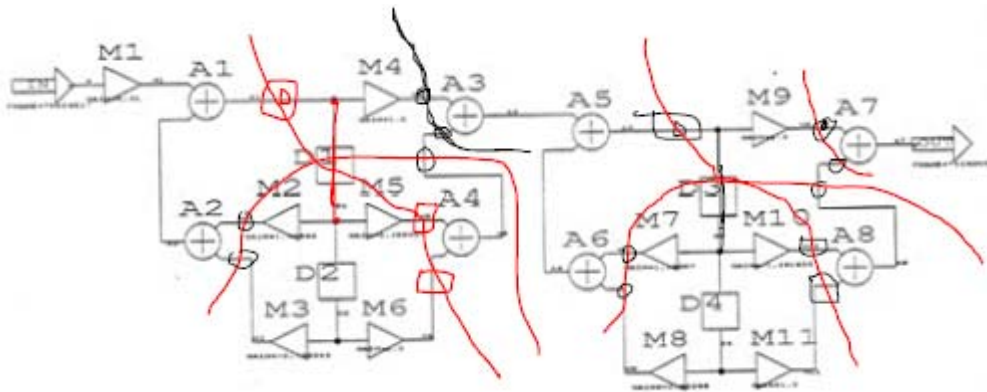
4. [10 points] We are going to determine the word-length for the above IIR filter. As you may know, the first step in the word-length optimization is 'grouping.' Please explain your strategy of how to group this signal flow graph. There can be a few different answers. So, your logic or idea is important. Note that the input and the output word-lengths of this filter are given, hence you do not need to determine them. Please try to make the number of groups not be greater than 6. As for the multiplier, you just need to group the multiplier input word-length (for example M4in, M5in, M9in, ...) because the multiplier output word-length is automatically determined by the input and the coefficient wordlength. You also need to consider that the input and output word-lengths for an adder is the same.
Ans: Signals connected by delays are grouped. At the output of A1, A5, add quantizers to shorten the wordlength of the multipliers.
Group1: A1, A2   Group2: M2, M3, M4, M5, M6   Group3: A3, A4, A5, A6
Group4: M7, M8, M9, M10, M11   Group5: A7, A8

Quiz 3 (15 minutes)   - CORDIC algorithm (Xilinx DSP Primer)   - Timing and synchronization (Timing issues Xilinx DSP Primer)   - Reading: 06_multirate (Xilinx material)
- VHDL, HDL cosimulation for MAC filter verification   - Adaptive filtering (Xilinx DSP Primer)
- Digital Down Converter (DDC)   - Midterm

Special Topics on Communication: FPGA based Communication System Design

May 15th, 2008 [75 minutes] 1:00~2:15 pm   Prof. Wonyong Sung

1. [5 points for each] Please say yes(O) or no(x) on the following questions with short explanations.

(1) For very low-throughput applications, the CORDIC based digital frequency synthesizer is more advantageous in hardware size than the one using ROM table. (Yes, No), explain in short.

Ans: Yes. CORDIC architecture can reduce the chip area very much by adopting a bit serial logic for low frequency applications. ROM based architecture needs the same amount of ROM regardless of the throughput.

(2) We are going to implement a digital filter using time-multiplexed architecture. Obviously, we can reduce the number of multipliers and adders by increasing the time-multiplexing ratio. I wonder if the chip area for storage (sequential logic) is also reduced by increasing the time-multiplexing ratio. Is it right? Also explain in short.

Ans: No. The memroy area for information storage is constant regardless of the time-multiplexing ratio.

(3) At the above problem (time-multipelxed implementation of a digital filter), I also wonder if the dynamic power decreases as the time-multiplexing ratio increases. Is it true? Also explain in short.

Ans: No. Time-multiplexing reduces the total capacitance, but increases the switching frequency of the capacitance. As a result, power is not reduced.

(4) Explain the flow of fixed-point optimization; this consists of 4 to 6 steps. Give short explanation for each step.

Ans: 1) Range estimation and integer wordlength determnination

2) Grouping

3) Minimum word-length determination for each group.

4) Cost optimum search while satisfying the performance.

2. [20 points] We are going to implement an adaptive filter in VLSI with the time-multiplexing ratio of 8. The equations for the adaptive filtering are shown below, where x(n) is the input, $c_k(n)$ is the filter coefficient (k = 0,1, ... , 15), y(n) is the output, d(n) is the reference, and e(n) is the error signal, and μ is the step size factor. The filter length of this filter is 16. You do NOT need to show the bit-positions in hardware design (this question is for time-multiplexed implementation, not fixed-point design)

$$y(n) = \sum_k c_k(n)x(n-k)$$
$$e(n) = y(n) - d(n)$$
$$c_k(n+1) = c_k(n) - \mu\, e(n)x(n-k)$$

(a) Please show the hardware block diagram for implementing this filter. Note that the filter length is

16, and the time-multiplexing ratio is 8.
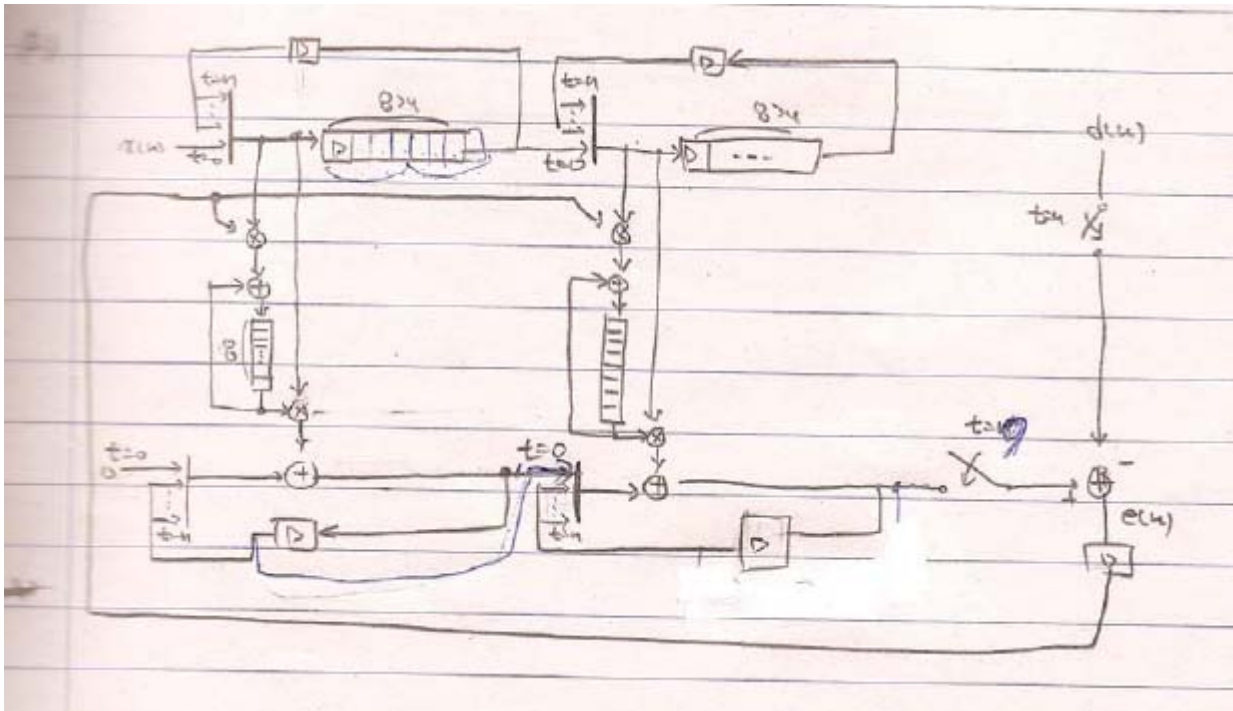
(b) Please show the timing diagram (0~7, because the time-multiplexing ratio is 8) of the hardware that you've designed.

time0: x[n]*h0[n]   x[n-8]*h8[n]

time1: x[n-1]*h1[n]   x[n-9]*h9[n]

...

time7: x[n-7]*h7[n]   x[n-15]*h15[n]

time8(next time0): x[n+1]*h0[n+1]   x[n-7]*h8[n+1]

   ....

3. [20 points] We are going to implement a VLSI for an FIR filter having a length of 8.   The time-multiplexing ratio of 8 is used (this means that we need only one multiplier and one adder).   The input signal has the range of -1 to 1 (so, Integer Word Length of 0 can be used).   The coefficients are all between -1 to 1 (the IWL is 0).   The intermediate signal (the signal being added at the adder chain) is between -4 and 4 (the IWL of 2).   Please design the hardware for this filter.   The multiplier is 8bit signed * 8bit signed -> 15 bit signed.   The adder to use is 12 bit.   You need to show the

interconnection of bits as precisely as possible (this question is about the fixed-point hardware design).
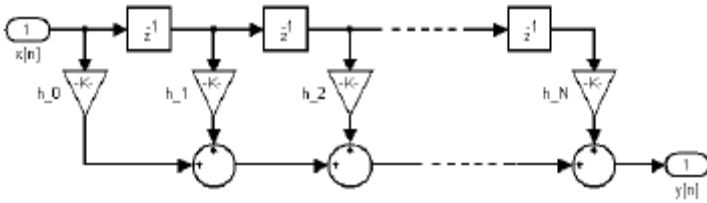
Ans: The IWL of input data 0, IWL of coefficients 0, the IWL of adder is 2.

This means that the multiplier output needs to be 2 bit sign extended to be added. Lower 5 bits of the multiplier output are truncated.
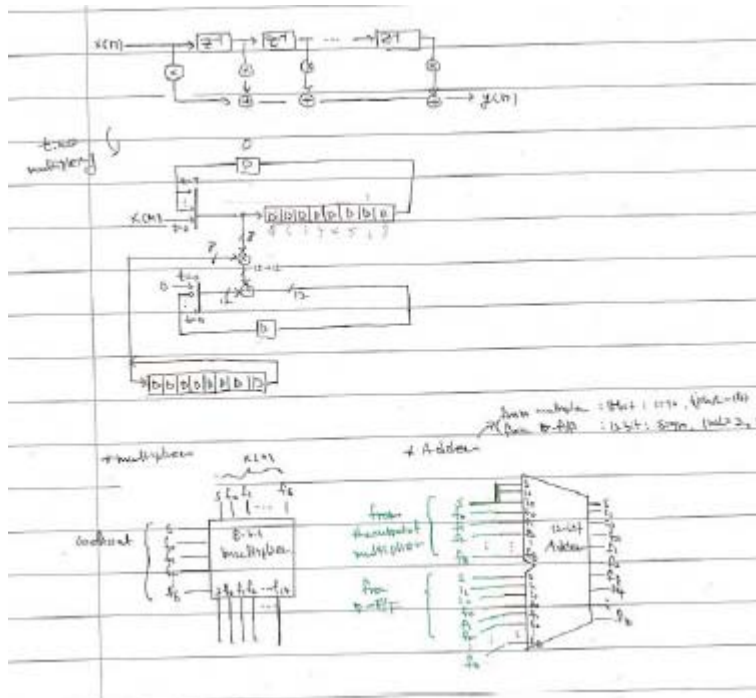
4. [20 points] We are going to implement a digital down converter (I, Q channels) for a digital receiver. The signal to down convert has a .625 MHz band of interest that is centered at 20 MHz, and is sampled at 61.44 MHz. The input signal is multiplied with cosine (I) and sine (Q) waves, and then low-pass filtered and decimated by 25. We will obtain two baseband terms (I, Q) after the down-conversion. The final sample rate will be 61.44/25= 2.4576MHz. The low-pass filter has the filter length of 184. The figure shows the overall block diagram (the detail is not clear - this is intentional).

(a) What is the system clock rate (that corresponds to z^{-1}) in this block diagram?

Ans: 61.44*2 (I, Q bands) = 122.88 MHz

(b) What is the order of the delay connecting the blocks (in the figure, Order?)?

The decimation ratio is 25. However, we need to process I, Q bands. So, the order of the delay is 50.

(c) Please show (explain) the circled part in detail. You need to show the name of the blocks, the coefficient ROM size, and explain the function of those blocks.

The ROM size is 25 (decimation ratio). "Slice" and "Reinterpret" for fixed-point format conversion.

"Upsampler"s for I, Q processing in alternate clocks.

Pipelined Polyphase Decimator Using Memory and Multipliers

Order? Question b

Cos, Sin wave

ROM

Question C