Advanced Embedded Systems (Autumn 2008)

Final Exam (Closed Book)

2008/12/10
4:00 P.M. – 5:15 P.M.

Total Points: 100

Problem 1. [10]
Consider ARM-based embedded systems. What are differences between MPU and MMU? Which one is more useful in supporting virtual memory? Why?

Problem 2. [10]
Explain what the fast context switch extension is in ARM-based systems. Describe in detail how it works.

Problem 3. [10]
In ARM architectures, explain how exceptions and associated modes are used. For the FIQ mode, explain why it is called *fast*.

Problem 4. [10]
The following techniques are recommended for efficient programming for ARM-based systems. ***Briefly*** explain why each technique is recommended:
(a) [5] Countdown to 0
(b) [5] Blocking

Problem 5. [10]
Discuss main differences between the Thumb instruction set and IBM's CodePack architecture.

Problem 6. [10]
Describe two examples of compiler-level low power techniques other than an intra-task DVS technique.

Problem 7. [15]
We have studied various techniques that affect execution times, power/energy or memory size throughout this course. Among them, choose one technique from each category below and explain why it belongs to a particular category.

Category I techniques: improve execution times but increase the memory size required.
Category II techniques: do not change execution times but reduce energy consumption.
Category III techniques: reduce memory size but increase execution times.

Problem 8. [5]
In order to overcome the power wall of modern high-performance CPUs, multicore architectures were proposed as an attractive alternative. Explain why multicore architecturs are better in terms of the energy efficiency while supporting the same performance.

Problem 9. [10]
Describe what the break-even time is. Express it using *Pw*, *Ps*, *To*, and *Eo* where *Pw* and *Ps* are the power consumed in the working state and sleeping state, respectively, and *To* and *Eo* indicate the state transition delay and state transition energy (including both shutdown and wake-up), respectively.

Problem 10. [10]
Suppose that you were asked to design a low-power cache whose main goal is to reduce the subthreshold leakage. Describe your cache organization in detail. Show the overall block diagram of your cache and explain how it works.