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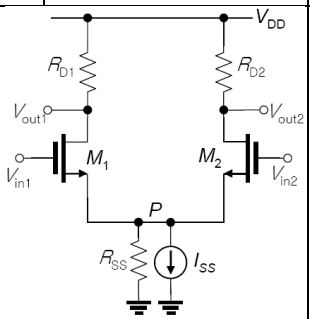
1. For the circuit on the right, answer for the following questions. Assume γ=0 (no back-bias effect), λ=0, and $g_{m1}=g_{m2}=g_m$ for M_1 and M_2 transistors. Also assume $R_{D1}=R_{D2}=R_D$. (30)



(a) Briefly describe key advantages of fully symmetric differential amplifier. (4)

(b) Prove that P is a virtual ground for small, differential inputs. (5)

(c) Derive the expression for differential mode gain. (V_{in2}=-V_{in1}) (4)

(d) Derive the expression for the common mode gain. (4)
(R_{D1}=0 Ω)

(e) Derive CMRR expression. How can you improve the CMRR. (3)
(R_{D1}=0 Ω)

(f) When R_{D1} is 0 Ω, derive the expression for differential mode gain. (5)

(g) In the circuit, V_{CM}=1 V, I_{SS}=1 mA, and R_D=1 kΩ. What is the minimum allowable supply voltage if the transistors must remain in saturation? Assume $V_{TH,n}$=0.5 V and R_{SS}=∞. (5)

Answer)

(a) i) If V_{DD} fluctuates, it can be canceled out.
(high rejection of supply noise)
ii) the swing of V_{out1}-V_{out2} can reach 2{V_{DD} - (V_{GS}-V_{th})} which is double the swing in a single CS amplifier.
etc.

(b) $V_{in1}=-V_{in2}$

$V_{in1}=V_{CM}+\Delta V$, $V_{in2}=V_{CM}-\Delta V$

$I_{D1}=\frac{I_{ss}}{2}+\Delta I$, $I_{D2}=\frac{I_{ss}}{2}-\Delta I$

$\Delta I=g_m\Delta V$

$I_{D1}=g_m(\Delta V-\Delta V_p)$, $I_{D2}=g_m(\Delta V+\Delta V_p)$

$\Delta I_{D1}=-\Delta I_{D2}$

$g_m(\Delta V-\Delta V_p)=g_m(\Delta V+\Delta V_p)$

$\therefore$ $\boldsymbol{\Delta V_p=0}$ (V_P is a virtual ground)

There can be other answers for this problem.

(c) Using half circuit analysis,

$$\boldsymbol{A_v=-g_mR_D \quad (r_o=\infty)}$$

(d) If $R_{D1}=0$, $R_{D2}=R_D$,

$\Delta V_{CM}=\Delta V_{GS}+2\Delta I_D R_{ss}$

$=\Delta I_D(\frac{1}{g_m}+2R_{ss})$

$$\Delta I_D=\frac{\Delta V_{CM}}{\frac{1}{g_m}+2R_{ss}}$$

$$V_{out}=\Delta V_{out1}-\Delta V_{out2}=\Delta I_D R_D=\frac{\Delta V_{CM}}{\frac{1}{g_m}+2R_{ss}}R_D$$

$$A_{CM-DM}=\frac{\Delta V_{out}}{\Delta V_{CM}}=\frac{R_D}{\frac{1}{g_m}+2R_{ss}}\approx\frac{R_D}{2R_{ss}}$$

(f) V_{in2}=-V_{in1}

$V_{out1}=0$, $V_{out2}=-g_mR_Dv_{in2}$

$$A_v=\frac{v_{out1}-v_{out2}}{v_{in1}-v_{in2}}=\frac{g_mR_Dv_{in2}}{-2v_{in2}}=-\frac{g_mR_D}{2}$$

(e) $$CMRR=\left|\frac{A_{DM}}{A_{CM-DM}}\right|=\frac{1+2g_mR_{ss}}{2}$$

From this result, you can improve the CMRR by increasing g_m and R_{ss}.

(g) $V_{DD}-I_DR_D=V_{DS}$

$V_{DS}\geq V_{GS}-V_{TH}(sat)$

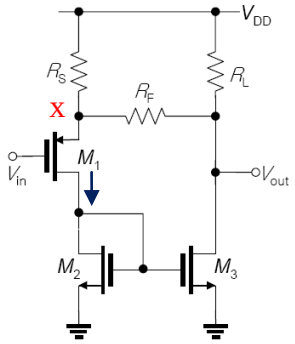
$V_{DD}-I_DR_D\geq 1-0.5$

$V_{DD}-0.5\geq 0.5$

$V_{DD}\geq 1$

$\therefore$ **minimum allowable supply voltage is 1[V].**

2. For the circuit on the right, answer for the following questions. Assume $(W/L)_2$ and $(W/L)_3$ are different. Assume λ=0 for all transistors, and γ=0 for M_1. (12)



(a) Assume R_F is much larger than R_S and R_L. Also assume R_S=0 Ω. Calculate small signal voltage gain. (7)

(b) Determine the polarity of feedback when R_S is finite. (5)

Answer)

(a) $(\frac{W}{L})_2=(\frac{W}{L})_3$, $r_o=\infty$

$R_F \gg R_S, R_L$ means R_F path is opend.(open loop)

$I_{D1}=I_{D2}$

$$I_{D3}=\frac{(W/L)_3}{(W/L)_2}I_{D2}$$

$$V_{out}=\frac{(W/L)_3}{(W/L)_2}I_{D2}R_D=\frac{(W/L)_3}{(W/L)_2}g_{m1}v_{in}R_L$$

$$A_v=\frac{v_{out}}{v_{in}}=\frac{(W/L)_3}{(W/L)_2}g_{m1}R_L$$

(b) $V_{in}\uparrow\Rightarrow I_{D1}\downarrow\Rightarrow I_{D2}\downarrow I_{D3}\downarrow\Rightarrow V_{out}\uparrow V_X\uparrow\Rightarrow I_{D1}\uparrow$

or

$V_{in}\uparrow\Rightarrow V_Y\downarrow\Rightarrow I_{D3}\downarrow\Rightarrow V_{out}\uparrow V_X\uparrow\Rightarrow V_Y\uparrow$

Thereby opposing the effect produced by V_{in}, the feedback is therefore **negative**.

(1/2) Check if your name and ID are written or correct.

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3. Assume that the MOSFETs (M_1 and M_2) have the same output resistance r_o (λ>0). Load capacitance C_L is connected to output. Neglect other capacitances. M_1 and M_2 are n- and p-type MOSFETs, respectively. Answer for the following questions. (8)

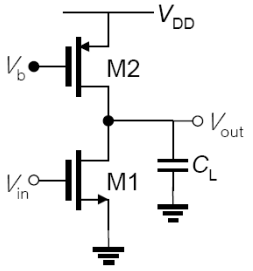


Fig. 1

(a) Assume that there is a capacitance (C_F) between the gate and the drain of M_1. By using Miller theorem, calculate the input and output capacitances. (3)

(b) Estimate the -3 dB bandwidth in (a) as the r_o goes to infinite (λ=0). Here assume that there is a finite input resistance connected with V_{in} in series. (2)

(c) Assume that V_{in} and V_b are exchanged. That is to say, V_{in} is connected to the gate of M_2 and V_b is connected to the gate of M_1. Compute voltage gain at low frequency. (3)

Answer)

(a) low frequency gain, $A_v = -g_m(r_o \| r_o) = -\frac{g_m r_o}{2}$

Using Miller's Theorem,

$$C_{F,in} = (1+\frac{g_m r_o}{2})C_F$$

$$C_{F,out} = (1+\frac{2}{g_m r_o})C_F + C_L$$

(b) $r_o = \infty$, a finite input resistance = R_S

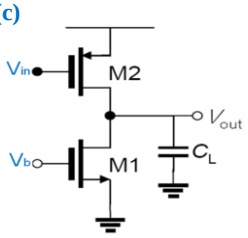
Since $C_{F,in}$ is infinite, the input pole is zero $(w_{pin} = 1/R_s C_{F,in} = 0)$.

The output pole is also zero because r_o is infinite.

$(W_{p,out} = 1/(r_o/2)(C_L + C_{F,out}) = 0)$

$\therefore$ $BW \cong 0$

(c)



Including the impedance of C_L $(\frac{1}{jwC_L})$,

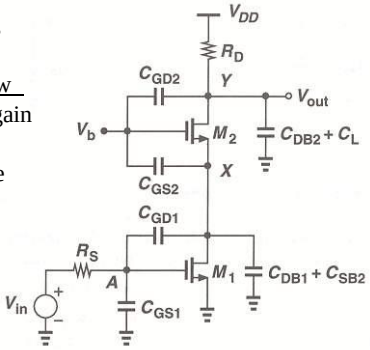
$$R_{out} = r_o \| r_o \| \frac{1}{jwC_L}$$

So the gain of the circuit is $-g_m(r_o \| r_o \| \frac{1}{jwC_L})$.

At a low frequency, we can ignore C_L (opened).

$$\therefore \quad A_v = -g_m \frac{r_o}{2}$$

4. For the following cascade stage, answer for the following questions. Assume $\gamma_n = \lambda_n = 0$. (20)



(a) Describe briefly key features of the amplifier. (5)

(b). Derive an expression for low frequency small signal voltage gain between nodes *A* and *X*. (5)

(c) Using Miller theorem, derive expressions of capacitances at nodes *A* and *X*. (5)

(d) Suppose a resistor R_G appears in series with the gate of M_2. Including only C_{GS2}, neglecting other capacitances, determine the transfer function (5)

Answer)

(a) Compared with the Miller approximation results obtained in CS stage, the input pole has risen considerably and hence the cascode band width is larger.

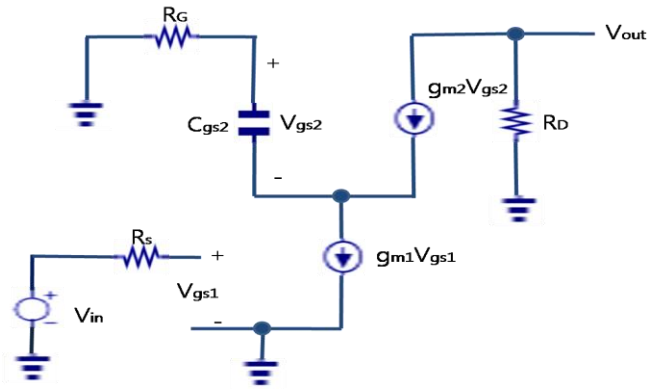
(b) A low frequency gain from A to X is

$$A_v = -\frac{g_{m1}}{g_{m2}} \quad (r_{o1}, r_{o2} = \infty)$$

(c) $C_A = C_{GS1} + (1+\frac{g_{m1}}{g_{m2}})C_{GD1}$

$$C_X = C_{DB1} + C_{GS2} + (1+\frac{g_{m2}}{g_{m1}})C_{GD1} + C_{SB2}$$

(d)



$$\frac{V_{out}}{V_{in}} = \frac{V_{gs2}}{V_{in}} \cdot \frac{V_{out}}{V_{gs2}}, \quad V_{in} = V_{gs1}$$

$$g_{m1}V_{in} = g_{m2}V_{gs2} + jwC_{gs2}V_{gs2} = V_{gs2}(g_{m2} + jwC_{gs2})$$

$$\frac{V_{gs2}}{V_{in}} = \frac{g_{m1}}{g_{m2} + jwC_{gs2}}, \quad \frac{V_{out}}{V_{gs2}} = -g_{m2}R_D$$

$$\therefore \frac{V_{out}}{V_{in}} = \frac{-g_{m1}g_{m2}R_D}{g_{m2} + jwC_{gs2}}$$

(2/2) Check if your name and ID are written or correct.

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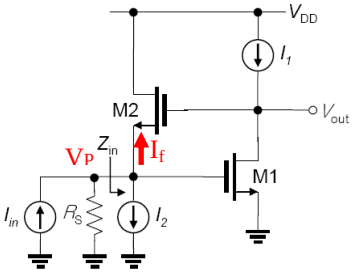
5. Assume that MOS transistors M_1 and M_2 have a finite r_{o1} and infinite r_{o2}, respectively. It is also assumed that current sources I_1 and I_2 are ideal. Answer for the following questions. (30)

(a) Identify the sense and return mechanisms. (3)

(b) Determine the polarity of feedback. (4)

(c) Calculate open-loop Z_{in} and Z_{out}. (3)

(d) The feedforward system in the circuit above is a transimpedance amplifier. Calculate the gain of feedforward system. (4)



(e) Calculate the feedback factor K. (4)

(Hint: Note the direction or polarity of feedback quantity (I_F or V_F)

(f) Calculate open-loop and closed-loop gains. (4)

(g) Calculate closed loop Z_{in} and Z_{out}. When ro1 goes to infinite, calculate again closed loop Z_{in} and Z_{out}. (4)

(h) When p-type MOSFET substitutes for n-type MOSFET M_2, determine the polarity of the feedback. Note the source of PMOS is connected to V_{DD}. (4)

Answer)

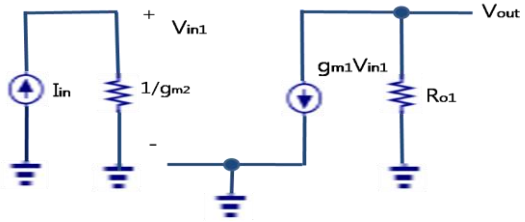
(a) This topology employs a transimpedance amplifier as the forward system. The feedback network sense the output voltage and return a current to the subtractor.
(voltage-current feedback)
M_2 both senses the output voltage and returns a current to the input. M_2 also serves as the feedback network.

(b) If I_{in} increases, V_p increases and I_{D1} increases. As a result, V_{out} decreases(like inverter), thereby decreasing I_{D2}. Finally, V_p decreases. Since the current injected by M_2 into the input node change in opposite directions, **the feedback is negative**.
$I_{in}\uparrow \rightarrow V_p\uparrow \rightarrow I_{D1}\uparrow V_{out}\downarrow \rightarrow I_{D2}\downarrow \rightarrow V_p\downarrow$

(c) $Z_{in} = \dfrac{1}{g_{m2}} \quad (r_{o2} = \infty)$

$Z_{out} = r_{o1}$

(d) the gain of feedforward system => open loop gain



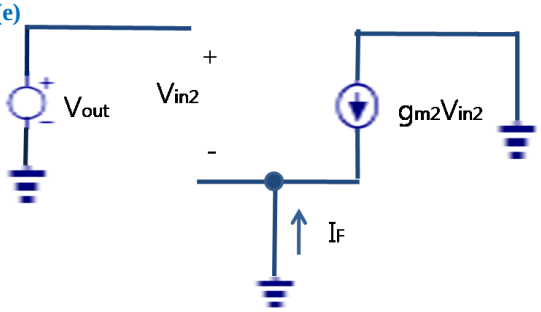
$V_{out} = -g_m V_{in1} r_{o1}$

$V_{in1} = \dfrac{1}{g_{m2}} I_{in}$

$V_{out} = -\dfrac{g_{m1}}{g_{m2}} r_{o1} I_{in}$

$\therefore R_o = \dfrac{V_{out}}{I_{in}} = \dfrac{-g_{m1} r_{o1}}{g_{m2}}$

(e)



$I_F = -g_{m2} V_{in2}$

$V_{in2} = V_{out}$

$I_F = -g_{m2} V_{out}$

$\therefore K = \dfrac{I_F}{V_{out}} = -g_{m2}$

(f) open loop gain = $R_o = \dfrac{-g_{m1} r_{o1}}{g_{m2}}$

closed loop gain $\dfrac{V_{out}}{I_{in}} = \dfrac{R_o}{1 + KR_o} = \dfrac{-g_{m1} r_{o1} / g_{m2}}{1 + g_{m1} r_{o1}}$

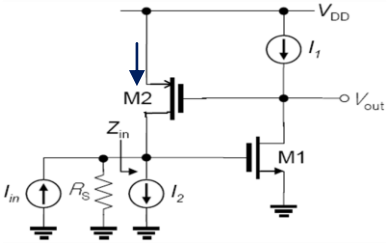
$= -\dfrac{g_{m1} r_{o1}}{g_{m2}(1 + g_{m1} r_{o1})}$

(g) $Z_{in,closed} = \dfrac{R_{in}}{1 + KR_o} = \dfrac{1/g_{m2}}{1 + g_{m1} r_{o1}} \cong 0$

$Z_{out,closed} = \dfrac{R_{out}}{1 + KR_o} = \dfrac{r_{o1}}{1 + g_{m1} r_{o1}} \cong \dfrac{1}{g_{m1}}$

$(r_{o1} = \infty)$

(h)



$I_{in}\uparrow \rightarrow V_p\uparrow \rightarrow I_{D1}\uparrow V_{out}\downarrow \rightarrow I_{D2}\uparrow \rightarrow V_p\uparrow$
Since the returned signal enhances the effect produced by I_{in}, The polarity of feedback is **positive**.