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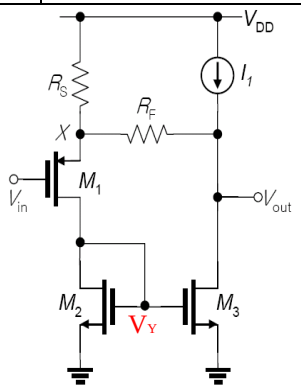
1. For the circuit on the right, answer for the following questions. Assume $(W/L)_2$ and $(W/L)_3$ are the same. Assume $\lambda=0$ for all transistors, and $\gamma=0$ for M_1. (20)



(a) Identify the sense and return mechanisms. (2)

Answer)

R_F senses the output voltage and serves as the feedback network. R_F also returns a voltage to the input.

(b) Determine the polarity of feedback. (2)

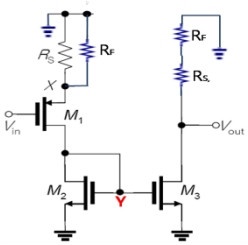
Answer)

$$V_{in}\uparrow \Rightarrow V_Y \downarrow \Rightarrow I_{D3}\downarrow \Rightarrow V_{out}\uparrow V_X \uparrow \Rightarrow V_Y \uparrow$$

Since this shows a counteractive effect of the change in V_{in}, the feedback is therefore **negative**.

(c) Calculate open-loop gain. (3)

Answer)



$$\frac{V_{out}}{V_{in}}=\frac{V_Y}{V_{in}}\cdot\frac{V_{out}}{V_Y},\quad \left(\frac{W}{L}\right)_2=\left(\frac{W}{L}\right)_3,\quad r_o=\infty$$

$$\frac{V_Y}{V_{in}}=-\frac{\frac{1}{g_{m2}}}{\frac{1}{g_{m1}}+R_S\parallel R_F},\quad \frac{V_{out}}{V_Y}=-g_{m3}(R_S+R_F)$$

$$A_o=\frac{V_{out}}{V_{in}}=\frac{\frac{g_{m3}}{g_{m2}}(R_S+R_F)}{\frac{1}{g_{m1}}+R_S\parallel R_F}=\frac{(R_S+R_F)}{\frac{1}{g_{m1}}+R_S\parallel R_F}$$

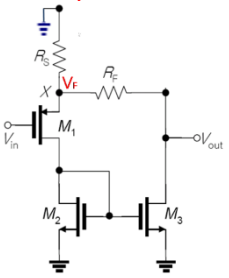
(d) Calculate open-loop Z_{in} and Z_{out}. (3)

Answer)

$$Z_{in,opened}=\infty,\quad Z_{out,opened}=R_S+R_F$$

(e) Calculate the feedback factor K. (3)

Answer)



$$K=\frac{V_F}{V_{out}}=\frac{R_S}{R_F+R_S}$$

(f) Calculate closed-loop gain. (3)

Answer)

$$A_{v,closed}=\frac{A_o}{1+KA_o}=\frac{\frac{R_S+R_F}{\frac{1}{g_{m1}}+R_S\parallel R_F}}{1+\frac{R_S}{\frac{1}{g_{m1}}+R_S\parallel R_F}}=\frac{R_S+R_F}{\frac{1}{g_{m1}}+R_S\parallel R_F+R_S}$$

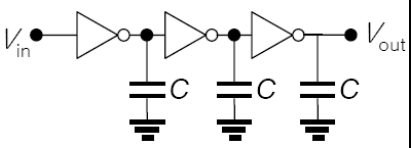
(g) Calculate closed loop Z_{in} and Z_{out}. (4)

Answer)

$$Z_{in,closed}=Z_{in,opened}(1+KA_o)=\infty$$

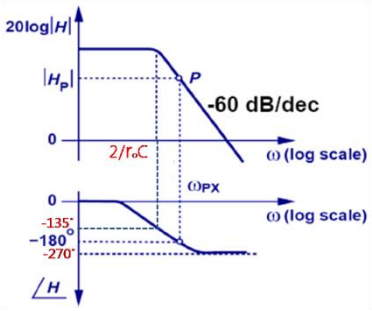
$$Z_{out,closed}=\frac{Z_{out,opened}}{(1+KA_o)}=\frac{R_S+R_F}{1+\frac{R_S}{\frac{1}{g_{m1}}+R_S\parallel R_F}}$$

2. For the circuit on the right, answer for the following questions. Each inverter consists of one PMOS and one NMOS connected in series. Three stages are identical. Assume both PMOS and NMOS are biased in saturation region and the same finite output impedance r_o. We wish to apply negative feedback with K=1 around the three-stage amplifier shown above. Neglect other capacitances. (10)



(a) Plot the frequency response of the circuit. (5)

Answer)



The circuit exhibits a low-frequency gain of $\left((g_{mN}+g_{mP})\frac{r_o}{2}\right)^3$ and three coincident poles given by w_p, $\left(\frac{r_o}{2}C\right)^{-1}$.

(b) Determine the condition for stability. (5)

$$H(s)=\frac{\left((g_{mN}+g_{mP})\frac{r_o}{2}\right)^3}{\left(1+\frac{s}{w_p}\right)^3},\quad w_p=\left(\frac{r_o}{2}C\right)^{-1},\quad \angle H(jw)=-3\tan^{-1}\frac{w}{w_p}$$

The phase crossover occurs if $\tan^{-1}(w/w_p)=60^\circ$ and hence $w_{PX}=\sqrt{3}w_P$.

$$\frac{\left((g_{mN}+g_{mP})\frac{r_o}{2}\right)^3}{\left(\sqrt{1+\left(\frac{w_{PX}}{w_p}\right)^2}\right)^3}<1,\quad (g_{mN}+g_{mP})\frac{r_o}{2}<2\quad (stable)$$

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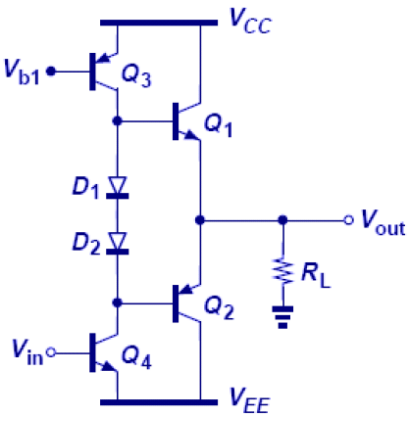
3. Following figure depicts improved push-pull stage to reduce crossover distortion. Turn-on voltages of Q_1 and Q_2 are V_{BE1} and V_{BE2}, respectively. Neglect the incremental resistance of D_1 and D_2. Answer for the following questions. (22)



(a) Two diodes (D_1 and D_2) are used to avoid thermal runway in above power amplifier stage. How can we solve the thermal runaway problem? Briefly explain the principle. (7)

Answer)

1)If the diodes experience the same temperature change as the output transistors, Thus $V_{D1}+V_{D2}$ will decrease at the same rate as $V_{BE1}+V_{BE2}$, with the result that the bias current remain constant.
(If the collector current is held constant, a rise in temperature in transistor results in a decrease in its V_{BE}.(≈ -2mV/˚C)
Alternately, if V_{BE} is held constant and the temperature increases, the collector current increases.)

2)Using diode biasing prevents thermal runaway since the currents in Q_1 and Q_2 will track those of D_1 and D_2 as long as there I_s's track with temperature.
Following equations show this accurately.

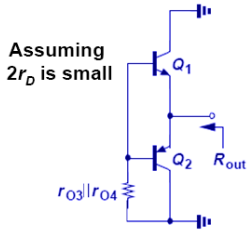
$$V_{D1}+V_{D2}=V_T\ln\frac{I_{D1}I_{D2}}{I_{S,D1}I_{S,D2}}$$

$$V_{BE1}+V_{BE2}=V_T\ln\frac{I_{C1}I_{C2}}{I_{S,Q1}I_{S,Q2}}$$

$$\therefore \frac{I_{D1}I_{D2}}{I_{S,D1}I_{S,D2}}=\frac{I_{C1}I_{C2}}{I_{S,Q1}I_{S,Q2}}\ (I_{D1}\approx I_{D2}, I_{C1}\approx I_{C2})$$

(b) Above push-pull stage employs a bias current of 1 mA in Q_3 and Q_4 and 10 mA in Q_1 and Q_2. If Q_3 and Q_4 suffer from the Early effect and V_{A3}=10 V and V_{A4}=15 V, calculate the small-signal output impedance of the circuit if β_1=40 and β_2=20. (8)

Answer)



$$g_{m1}=g_{m2}=\frac{I_{C1,2}}{V_T}=0.385A/V,\quad r_{\pi1}=\frac{\beta_1}{g_{m1}}=\frac{40}{0.385}=103.9\Omega$$

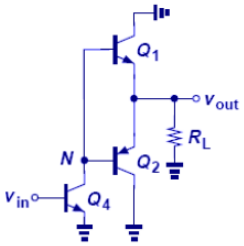
$$r_{\pi2}=\frac{\beta_2}{g_{m2}}=\frac{20}{0.385}=51.95\Omega,\quad r_{o3}=\frac{V_{A3}}{I_{C3}}=\frac{10}{0.001}=10k\Omega$$

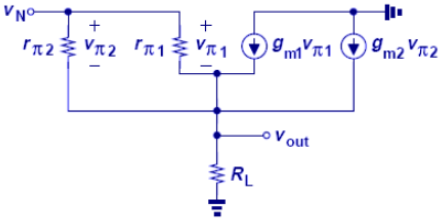
$$r_{o4}=\frac{V_{A4}}{I_{C4}}=\frac{15}{0.001}=15k\Omega$$

$$R_{out}=\frac{v_X}{i_X}=\frac{r_{\pi1}\|r_{\pi2}+r_{o3}\|r_{o4}}{1+(g_{m1}+g_{m2})(r_{\pi1}\|r_{\pi2})}=\frac{6\times10^3+34.63}{27.67}\cong218.1\Omega$$

(c) Using the result obtained in (b), determine the voltage gain if the stage drives a load resistance of 8 Ω. (7)

Answer)





$$\frac{v_N}{v_{in}}=-g_{m4}[(g_{m1}+g_{m2})(r_{\pi1}\|r_{\pi2})R_L+r_{\pi1}\|r_{\pi2}]\cong-9.42$$

$$\frac{v_{out}}{v_N}=\frac{1+(g_{m1}+g_{m2})(r_{\pi1}\|r_{\pi2})}{\frac{r_{\pi1}\|r_{\pi2}}{R_L}+1+(g_{m1}+g_{m2})(r_{\pi1}\|r_{\pi2})},\quad g_{m4}=\frac{I_{C4}}{V_{T4}}\cong0.038A/V$$

$$\cong0.84$$

$$\frac{v_{out}}{v_{in}}=\frac{v_N}{v_{in}}\bullet\frac{v_{out}}{v_N}\cong-7.91$$

4. We wish to design a Butterworth filter with a roll-off of 0.5dB at $\omega=0.8\omega_o$. Determine the required order. (7)

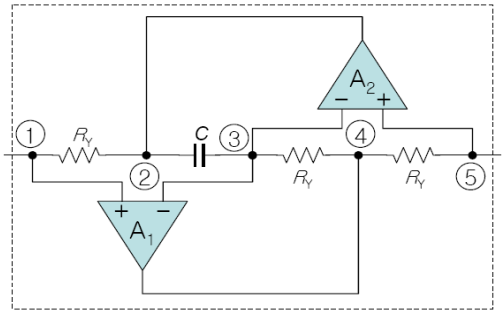
$$|H(j\omega)|=\frac{1}{\sqrt{1+\left(\frac{\omega}{\omega_o}\right)^{2n}}}$$

Answer)

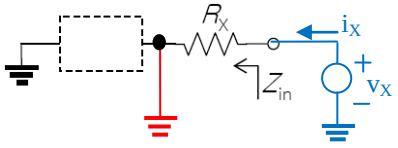
$$H(j0.8w_o)\cong0.94(-0.5dB),\quad \frac{1}{1+0.8^{2n}}=0.94^2,\quad n\cong4.57$$

$$\therefore n=5$$

5. Following figure depicts main part of general impedance converter (GIC). Assume all op amps are ideal. Answer for the following questions. (14)



(a) Using the circuit in the dashed box above, now we implement following circuit. Calculate the Z_{in}. (7)



Answer)

$$Z_{in}=\frac{v_X}{i_X}=R_X$$

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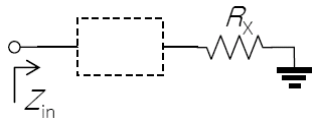
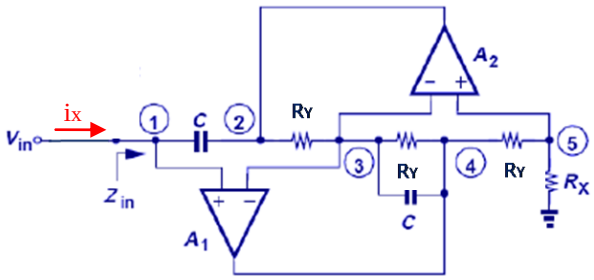
(b) In the dashed box, now RY between nodes 1 and 2 and C between nodes 2 and 3 are exchanged. A capacitor C is connected between nodes 3 and 4. Now calculate Z_{in} in the circuit configuration shown below. (7)



Answer)



$$V_X = V_1 = V_3 = V_5$$

$$\frac{V_X}{R_X} = \frac{V_4 - V_X}{R_Y}, \quad V_4 = \frac{V_X}{R_X} R_Y + V_X$$

$$I_{43} = \frac{V_4 - V_X}{R_Y \| \frac{1}{Cs}} = \frac{V_X(1+R_YCs)}{R_X}, \quad V_2 = V_3 - R_Y I_{43} = V_X - \frac{V_X R_Y (1+R_YCs)}{R_X}$$

$$I_X = Cs(V_1 - V_2) = \frac{CsV_X R_Y (1+R_YCs)}{R_X}$$

$$\therefore Z_{in} = \frac{v_X}{i_X} = \frac{R_X}{CsR_Y(1+R_YCs)}$$

6. The figure on the right depicts a CMOS inverter. Assume both transistors M1 and M2 have exactly the same threshold voltage. Answer for the following questions. (27)

$$I_{D,lin} = \mu_n C_{ox} \frac{W}{L}[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}]$$

$$I_{D,sat} = \mu_n C_{ox} \frac{W}{2L}(V_{GS} - V_{TH})^2$$

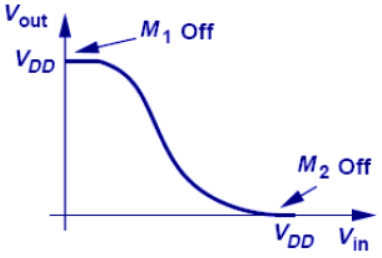
(a) Briefly describe the advantage of a CMOS inverter compared to an NMOS inverter which is composed of NMOS FET and a load resistance. (5)

Answer)

A CMOS inverter has following advantages.

i) The output low level is exactly equal to zero because $V_{in}=V_{DD}$ ensures that M_2 remains off.

ii) The circuit consumes zero static power for both high and low output levels.



However, a NMOS inverter has drawbacks from the passive nature of the load resister.

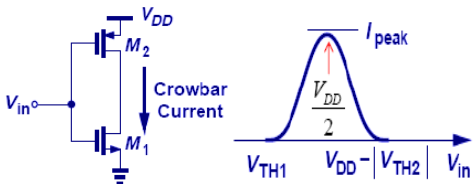
i) M_1 must "fight" R_D while establishing a low level at the output node and hence R_{on1} must remain much smaller than R_D.

ii) After M_1 turns off, only R_D can pull the output node up toward V_{DD}.

iii) The circuit draws a current of approximately V_{DD}/R_{DD} from the supply when the output is low.

(b) Prove that when both transistors M1 and M2 have exactly the same current drivability, we can observe the maximum crowbar current at V_{in} of 0.5 V_{DD}.
(hint: $V_G=V_{in}$, $V_D=V_{out}$, V_S(PMOS)$=V_{DD}$). (6)

Answer)



The crowbar current reaches a maximum when both transistors enter saturation.

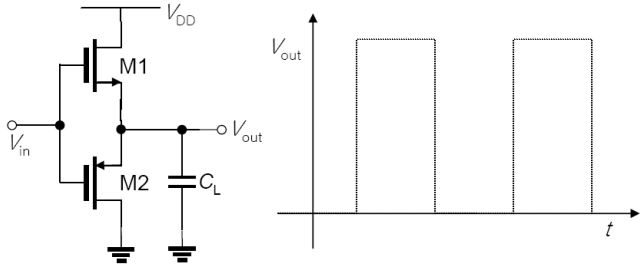
$$I_{peak} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left(\frac{V_{DD}}{2} - V_{TH1}\right)^2\left(1+\lambda_1\frac{V_{DD}}{2}\right)$$

$$= \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2\left(\frac{V_{DD}}{2} - V_{TH2}\right)^2\left(1+\lambda_2\frac{V_{DD}}{2}\right)$$

(M1 and M2 have exactly the same current drivability.)

$$\left(1+\lambda_1\frac{V_{DD}}{2} \approx 1+\lambda_2\frac{V_{DD}}{2}, \quad \frac{W_2}{W_1} \approx \frac{\mu_n}{\mu_p}, \quad V_{TH1} \approx |V_{TH2}|\right)$$

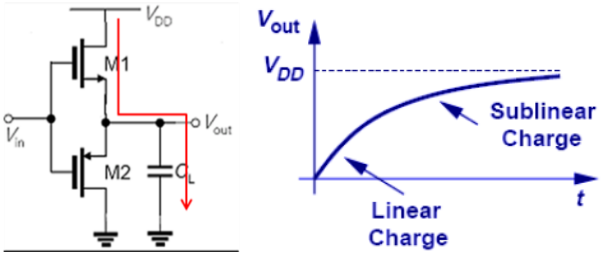
c) When PMOS M2 and NMOS M1 are exchanged as follows, sketch schematically output waveform for a given input waveform. Describe briefly the reason. (6)



Answer)

i)V_{in} varies from zero to V_{DD}

.



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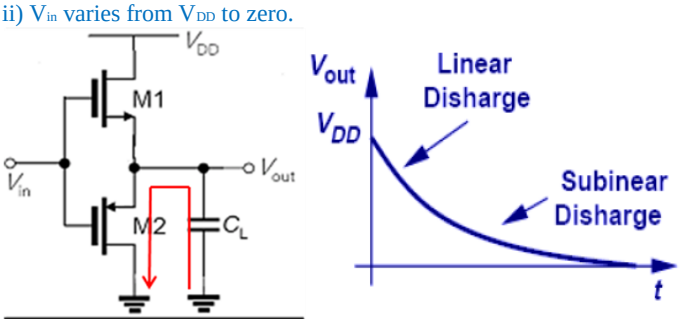
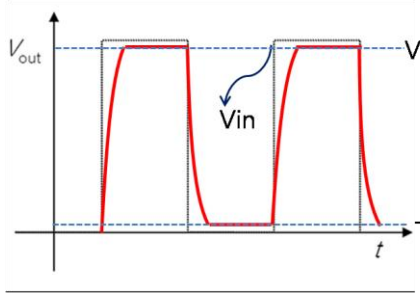
V_{in} jumps from 0 to V_{DD} at t=t1 and V_{out} begins to from 0. Transistor M1 turns on in saturation and M2 turns off, charging C_L toward VDD-V_{TH1}. With the relatively constant current provided by M1, V_{out} rises linearly until M1 enters the triode region and hence supplies a smaller current. The output voltage continues to rise, almost as if M1 acts as a resister, eventually approaching V_{DD}-V_{TH1} and forcing the drain current of M1 to zero.

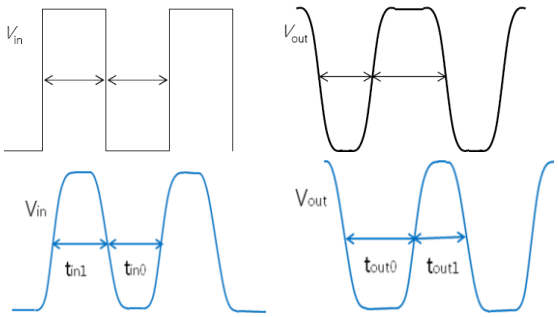
ii) V_{in} varies from V_{DD} to zero.



M1 turns off and M2 turns on beginning to discharge C_L from V_{DD}-V_{TH1} toward -V_{TH2}. Transistor M2 operates in saturation until V_{DD} falls by -V_{TH2} above the gate voltage(=0), upon which I_{D2} begins to decrease, slowing down the discharge. V_{out} then gradually approaches -V_{TH2}.



(d) For a given input waveform (square wave, t(logic 1) / t(logic 0) =1), following output waveform (t(logic 1) / t(logic 0) < 1) is observed. Estimate what the cause is. (5)



Answer)

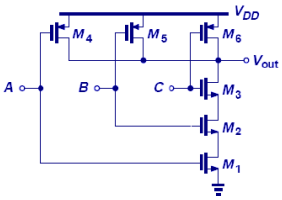
For example, when NMOS and PMOS have the same current drivability, as $(W/L)_1$ increases, the current drive of M1 increase. The circuit will exhibit then faster falling transition. As s result, the circuit will show t_{out0} longer than t_{out1}. As an another case, when $(W/L)_2$ decreases, the current drive of M2 decrease. The circuit will exhibit then slower rising transition. Consequently, the circuit will also show t_{out0} longer than t_{out1}.(t_{out0}>t_{out1})

Thus, by varying $(W/L)_1$ and $(W/L)_2$, the current drivability of M1 and M2 can be changed and the transition time will be changed as well.

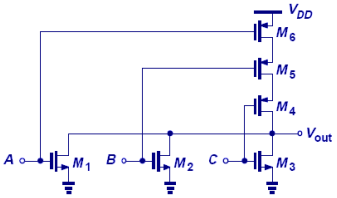
Of course, The Ron difference between NMOS and PMOS will show a rising and falling time(T_{PLH}, T_{PLH}) difference and then t_{out0} and t_{out1} are different.

(e) We normally use NAND gate more frequently than NOR gate when we design a logic function. Why? (5)

Answer)



(a)Three-input NAND gate



(b)Three-input NOR gate

The low mobility of holes requires a proportionally wider PMOS transistor to obtain a symmetric VTC and, more importantly, equal rise and fall time. Viewing the transistors in a three input NOR gate as resisters, we observe that the PMOS section suffers from three times the resistance of each PMOS device, quite larger than that of NAND gate because of the PMOS resistance NAND gate connected in parallel. Therefore, it creates a slower transition at the output that of NAND gate. On the other hand, to compare capacitance in the case of (a) with that of (b), (b) presents a capacitance of about $7WLC_{ox}$ at each input, smaller than that of (a)($5WLC_{ox}$). If wider PMOS transistors are employed to reduce R_{on}, then their gate capacitance increases and the situation even worsen. Consequently, the NAND gate less suffers from speed limitation.