Name: ____________________

Logic Design (Fall 2009)

Prof. Chang-Gun Lee

Time: 75 minutes

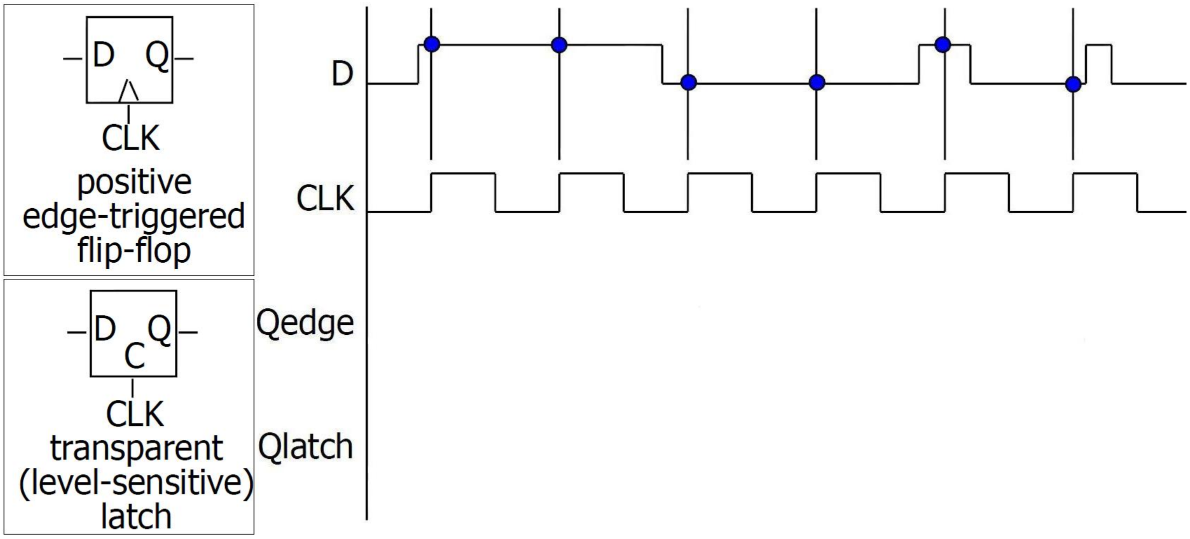
Instructions:

1. This is a closed book examination. Any form of cheating on the examination will result in a zero grade.
2. Do all your work inside this booklet, using the backs of pages if needed. The problems are of varying degrees of difficulty so please pace yourself and answer the questions in the order which best suits you. Answers to questions should be as brief and specific as possible.
3. Partial credit will be given even if your final solution is incorrect, if you show the intermediate steps you take in getting to the final solution. Clearly state any assumptions you make in your answers, and justify your assumptions.
4. Please write your answers neatly and, in case of numerical problems, *put the final answer in a box.* Good luck!

Problem No.	Max Points	Received Points
1	5	
2	5	
3	10	
4	10	
5	15	
6	15	
7	15	
Total	75	

1. [**5 points**] Briefly explain differencies between **combinational logic** and **sequential logic**.

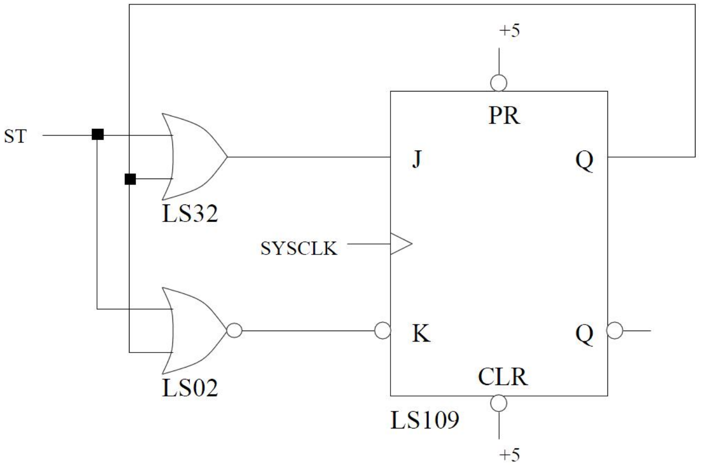
2. [**5 points**] Draw in the corresponding waveforms for the output Q_{edge} and Q_{latch}. Q_{edge} is the output of the positive edge-triggered D-FF and Q_{latch} is the output of the level-sensitive D-Latch. You can assume zero delays.



3. [**10 points**] Draw a state diagram for a clocked synchronous state machine with two inputs, $INIT$ and X, and one Moore-type output Z. As long as $INIT$ is asserted, Z is continuously 0. Once $INIT$ is negated, Z should remain 0 until X has been 1 for two successive ticks and 0 for three successive ticks. Then Z should go to 1 and remain 1 until $INIT$ is asserted again. In between two successive 1s and three successive 0s, there can be any sequence. Once $INIT$ is negated, it will not be asserted again until sometime after Z goes to 1.

4. [**10 points**] Answer the following questions.

(a) Analyze the following circuit using 3 step analysis approach by giving a complete state diagram for it with the format clearly shown.



(b) What is the maximum clock frequency? What are the setup and hold times for the input ST in your circuit? Use the following tables for the timing specifications for the chips.

Table 1: **Combinational parts**

Chip	t_{pLH} (ns)	t_{pHL} (ns)	Comments
'LS02	15	15	
'LS32	22	22	

Table 2: **'LS109 - $J-\bar{K}$ Type, Positive-edge-triggered flip/flops**

Data	t_{pLH}	t_{pHL}	t_s	t_h
$CLR, PR, CLK \rightarrow Q$	25	40		
J, K			35	5
$f_{max} = 25$ Mhz				

Max frequency = ____________

t^{ST}_{setup} = ____________

t^{ST}_{hold} = ____________

5. **[15 points]** Consider the following logic unit. It has three operation inputs (A, B, C), two data inputs (D_1, D_0), and a single output (Z). The logic unit is defined as follows: when $ABC = 000, Z = 0; ABC = 001, Z = D_0; ABC = 010, Z = D_1 AND D_0; ABC = 011, Z = D_1 NAND D_0; ABC = 100, Z = D_1 NOR D_0; ABC = 101, Z = D_1 OR D_0; ABC = 110, Z = D_1; ABC = 111, Z = 1$.

   (a) Implement to obtain a minimized implementation using the K-map method ($Note:$ This uses 5 variables!).

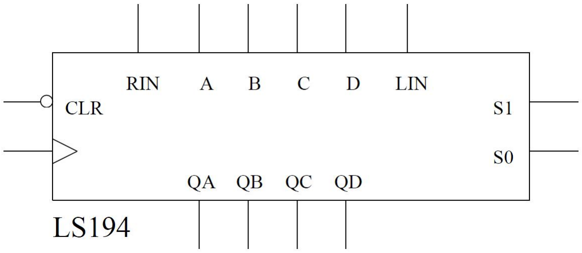
   (b) Implement using a 16:1 MUX (use A, B, C, D_1 as your MUX control inputs).

   (c) Implement using an 8:1 MUX plus whatever additional gate logic you need (use A, B, C as your MUX control inputs).

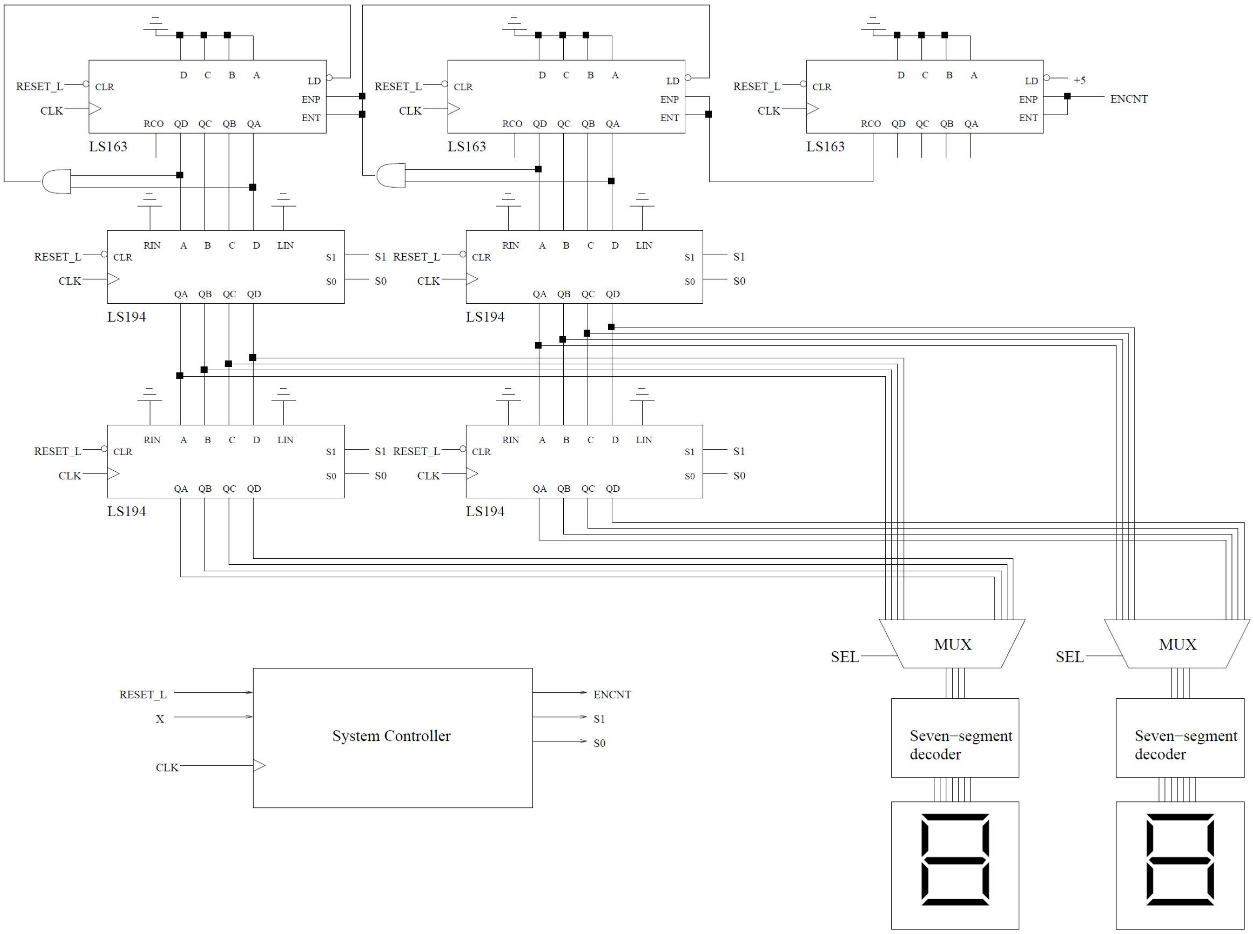
6. [**15 points**] Using a 74LS194, design a sequence generator which cycles through the following sequence(top to bottom and back again):

0000
1000
0001
0011
0110
1101
1110
1111

Have all unused states reset to 0000 (synchronously). Use the following block diagram for LS194.



7. [**15 points**] We have to design a digital stop watch with one push button X and one reset button $RESET$. Pushing $RESET$ resets everything including the timer, registers and flip flops (asynchronously). We can measuer the times taken for two events. If X is pushed once, the timer starts. If X is pushed again, the time taken to this first event is recorded in a different register and timer stops. The register values remain until $RESET$ is asserted. (We can view each register value before $RESET$ is asserted, by another control input SEL. But, ignore this part).
PROBLEM: Using the following system architecture, design the system controller.



Use the following assumptions in the design:

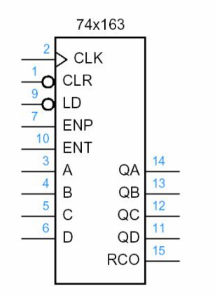
(a) CLK is 16 Hz.

(b) When X is asserted by pushing the button, it is negated immediately after it is detected by a CLK triggering edge.

(c) The stop watch can measure up to 99 sec. Assume that two events happen before 99 sec.

74LS163

- 4-bit, synchronous, parallel load, binary counter



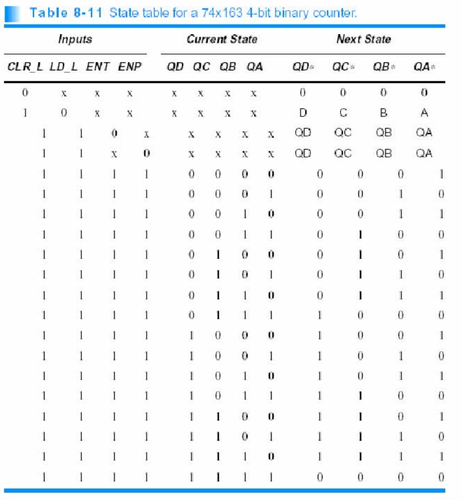


Table 8-11 State table for a 74x163 4-bit binary counter.

Inputs				Current State				Next State			
CLR_L	LD_L	ENT	ENP	QD	QC	QB	QA	QD*	QC*	QB*	QA*
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0

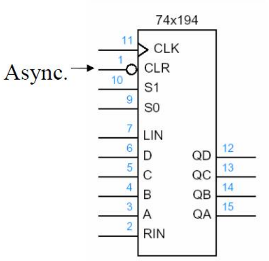
RCO

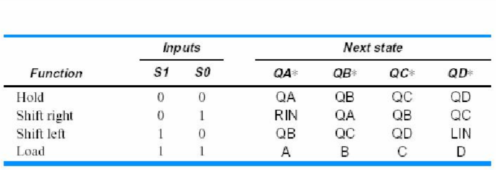
0

1

74LS194

- 4-bit, parallel in, parallel out, bi-directional shift register





Function	Inputs		Next state			
	S1	S0	QA*	QB*	QC*	QD*
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D