Topics in Integrated Circuit Design (Wireline Transceiver Design)
School of Electrical Engineering and Computer Science
Seoul National University

Fall 2020 D.K. Jeong

Final Exam

Dec. 7, 11:00 am-1:00 pm (in-class test)

Dec. 7, 1:00pm-Dec. 8, 11:00 am (take-home test, hand in to TA in the Room 218, Bldg. 104-1.)

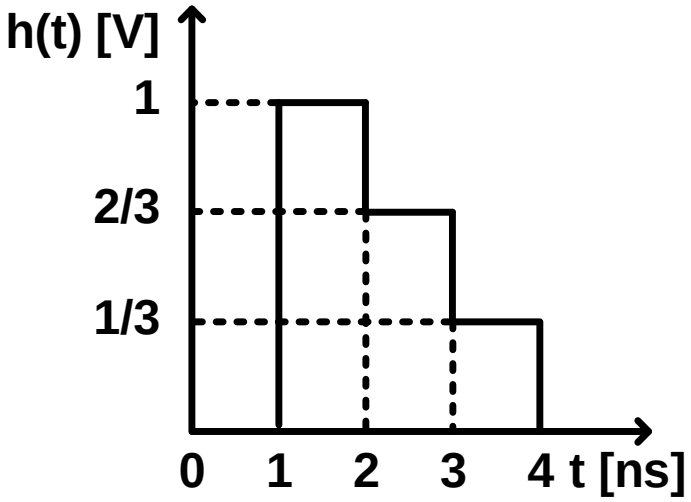
Books, notes, and tablets allowed in class.,

Take-home test 에 타인과 상의하지 않았음을 서약합니다.

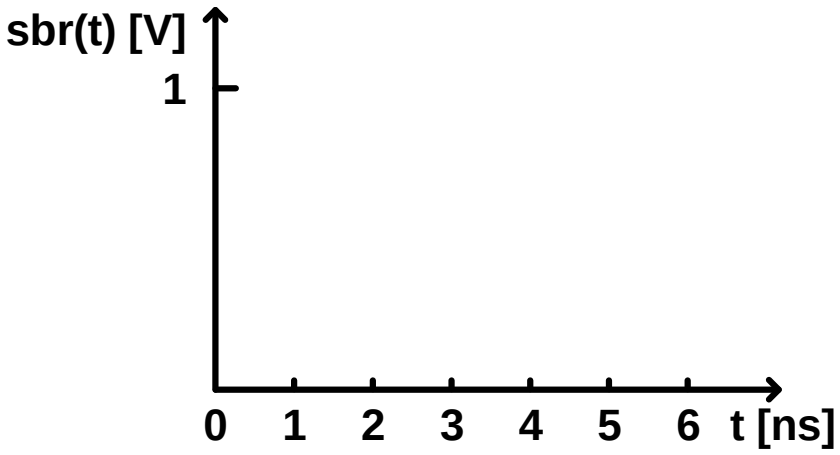
Name:_____ Signature:_____

Check one: In-Class Test ( ) Take-Home Test ( )	
Problem	Score
1	/35
2	/15
3	/25
4	/20
5	/35
Total	/130

1. Answer the questions on the channel with the following impulse response to a delta function $(1\text{nV})\cdot\delta(t)$.



A. Draw a single-bit response (1-bit, 1V-rectangular pulse) of a 1-Gbps NRZ transmission. (5 points)



B. What is the gain at the DC and at the Nyquist frequency including the effect of the ZOH of the rectangular pulse? (5 points)

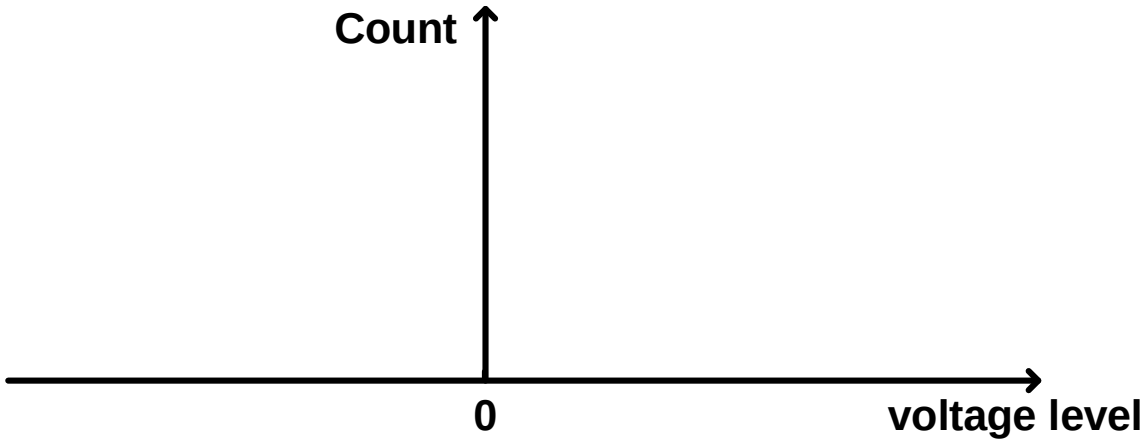
C. Find C_0 and C_1 of an TX FIR filter that minimize the mean square value of ISI. Assume that main cursor is maximized. (5 points)

D. What is the desired location of the zero of a CTLE for the flat response at the Nyquist frequency? (5 points)

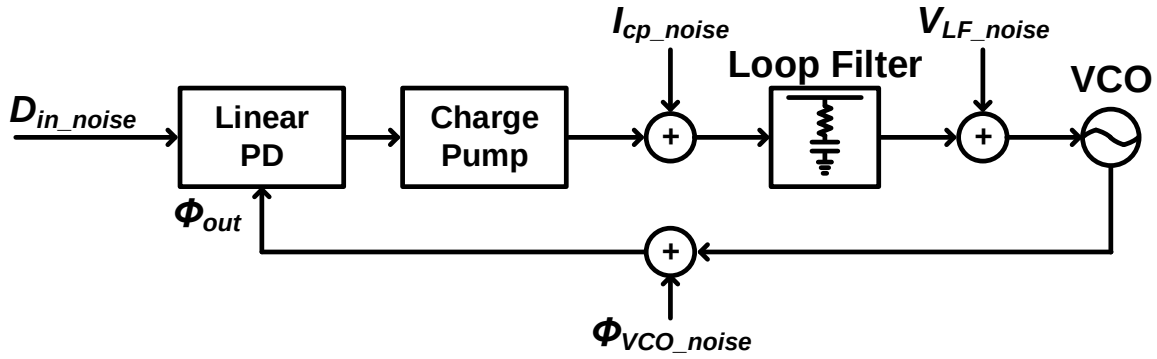
E. When an Alexander PD is used in the PLL-based timing loop, what is the optimum coefficient of a 2-tap DFE for the maximum eye height? Assume no edge equalization. (5 points)

F. How much gain boost at the Nyquist is expected with 2-tap DFE coefficient derived E? (5 points)

G. Sketch a histogram at sampling point for a equalized signal with 2-tap DFE with coefficient derived E. Assume that Gaussian noise is small enough. (5 points)



2. For the following PLL-based CDR for 1Gbps bandwidth, assume linear PD gain (K_{PD}) of 1, charge-pump current (I_{cp}) of 40 uA, loop filter resistor (R_{LF}) of 500 Ω, loop filter capacitor (C_{LF}) of 5 nF and VCO gain (K_{VCO}) of 0.5 GHz/V. Beware of units.



A. Find the open-loop gain H(s) and damping ratio ξ. (5 points)

B. Derive the transfer functions using H(s) for following input noise. Draw the Bode plot. (10 points)

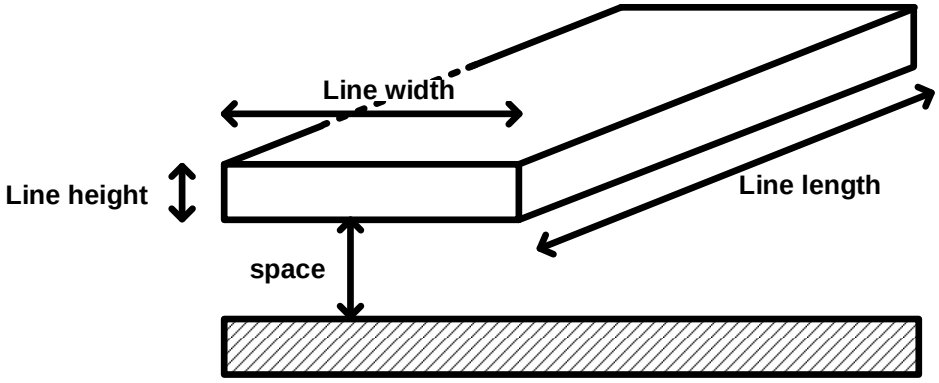
$\frac{\phi_{out}}{D_{in_{noise}}} =$

$\frac{\phi_{out}}{I_{CP_{noise}}} =$

$\frac{\phi_{out}}{V_{LF_{noise}}} =$

$\frac{\phi_{out}}{\phi_{VCO_{noise}}} =$

3. Goal is to sketch the attenuation characteristic for the following “microstrip” copper line with FR-4 medium of $e_r = 4.0$. [Line width – 200 um, line height – 20 um, space – 100um, line length = 1m, loss tangent = 0.01]



$$\rho = 1.7 \cdot 10^{-8}\ \Omega\ , e_0 = 8.854 \cdot 10^{-12}\ F/m\ , \mu_0 = 4\pi \cdot 10^{-7}\ H/m$$

A. What is its capacitance, DC resistance, inductance per meter? (5 points)

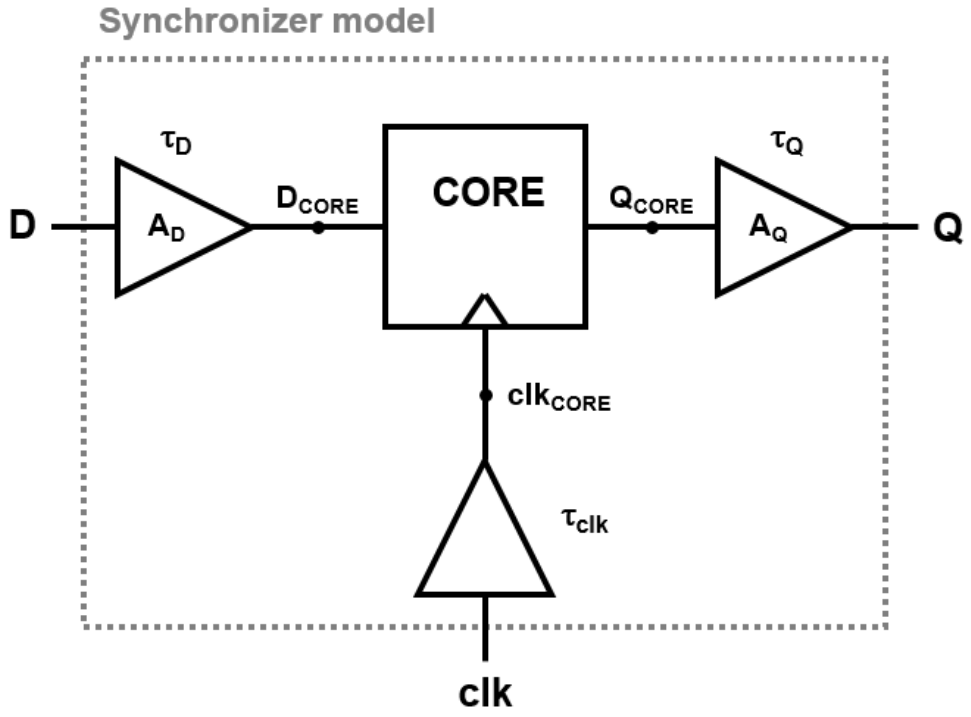
B. What is its characteristic impedance Z_0? (5 points)

C. Calculate the skin effect frequency f_s. (5 points)

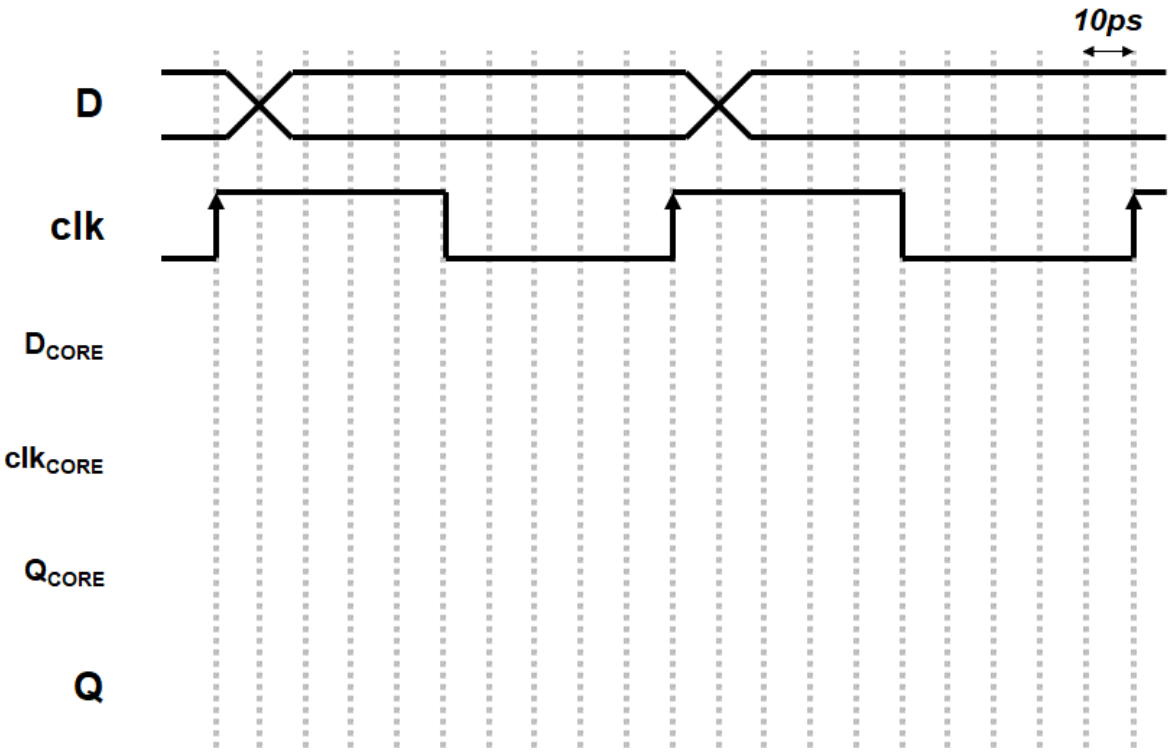
D. Find out the equation for the attenuation and sketch the attenuation in [dB] vs log f. (5 points)

E. Find the frequency that dielectric loss and skin effect loss are the same. (5 points)

4. For the following basic model of a synchronizer, assume $\tau_D = \tau_Q = 20$ ps, $\tau_{clk} = 30$ ps, $A_D = A_Q = 6$ dB, clk frequency = 10 GHz and rise/fall time of D = 15 ps. Beware of units.



(a) Draw the waveform of D_{CORE}, Q_{CORE}, clk_{CORE} and Q when close to metastability. (5 points)



(b) Draw the curve of T_{CQ} (clk-to-Q delay) vs. $T_{D\text{-}clk}$. (Note that $T_{D\text{-}clk}$ is the time difference between the transitions of D_{CORE} and clk_{CORE}.) (5 points)

(c) When the values of the curve obtained in (b) are as follows, calculate the time period of forbidden sampling window. (Note that forbidden sampling window means “setup time + hold time”.) (5 points)

- T_{CQ} = 0.15ns at $T_{D\text{-}clk}$ = 0.5ps
- T_{CQ} = 0.1ns at $T_{D\text{-}clk}$ = 2ps

(d) Calculate the error probability at Q node. (5 points)

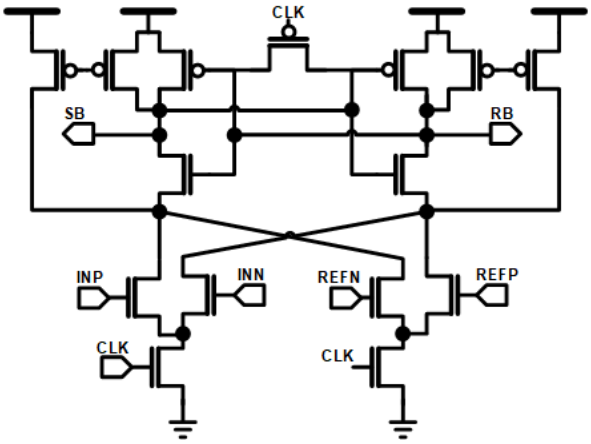
5. **다음 각각의 문제에 대해 설명하시오.** (Internet **에서** copy **하지 말고 나름대로 설명할 것**)

   a. DLL **에** PD **대신** PFD **를 사용할 경우 문제점은**? (5 points)

   b. DLL **의** harmonic locking **문제를 개선하기 위한 방법을 설명하시오.** (5 points)

   c. Optical receiver interface **에서** Si **을 사용하는 시도에 대한 장단점을 기술하시오.** (5 points)

d. **다음의** Strong arm latch **의** offset compensation **방법에 대해 두 가지 이상 설명하시오**. (5 points)



e. Phase interpolator **의** input slew rate **를 높이거나 낮추는 경우, 각각에 대한 문제점은? 그리고 그러한 문제가 발생하는 이유에 대해 설명하시오**. (5 points)

f. T-coil 을 input buffer 와 output driver 에 사용할 때의 회로를 각각 그리시오. T-coil 을 사용하여 얻을 수 있는 유용한 특성을 2 가지 이상 기술하시오. (5 points)

g. Low voltage (e.g. 1.0V) bandgap reference 를 만드는 방법을 그림과 함께 설명하시오. 그리고 해당 회로에서 start up 이 필요한 이유는 무엇인가? (5 points)

<End of Final exam>