Topics in Integrated Circuit Design (Wireline Transceiver Design)
School of Electrical Engineering and Computer Science
Seoul National University

Fall 2020 D.K. Jeong

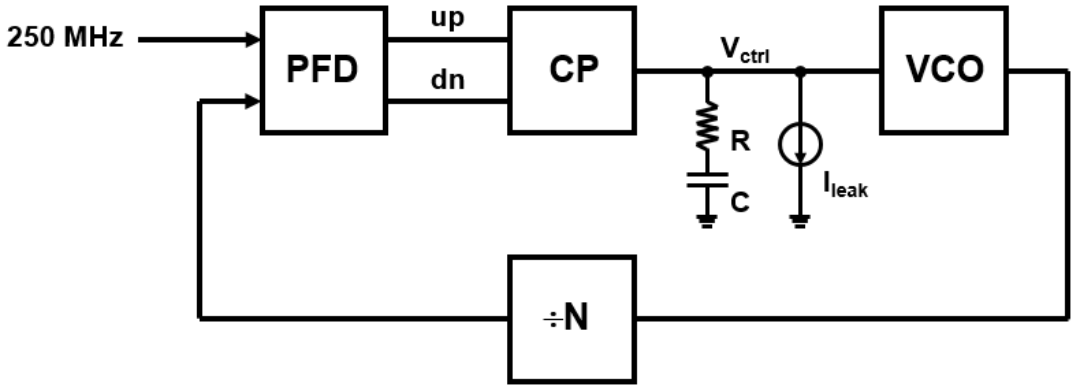
Midterm Exam
Oct. 26, 11:00 am-1:00 pm (in-class test)
Oct. 26, 1:00pm-Oct. 27, 11:00 am (take-home test, hand in to TA in the Room 218, Bldg. 104-1.)
Books, notes, and tablets allowed in class.,

Take-home test 에 타인과 상의하지 않았음을 서약합니다.

Name:_____ Signature:_____

| Check one: In-Class Test ( ) Take-Home Test ( ) | |
|---|---|
| Problem | Score |
| 1 | /25 |
| 2 | /20 |
| 3 | /15 |
| 4 | /15 |
| 5 | /25 |
| 6 | /15 |
| 7 | /30 |
| Total | /145 |

1. For the following charge-pump PLL, assume VCO gain ($K_{VCO}$) of 1 GHz/V, frequency division factor N of 16 and charge-pump current ($I_{cp}$) of 100 uA. Beware of units.



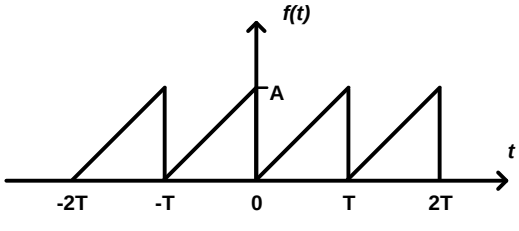

a. Determine loop filter parameters R and C that realize the loop bandwidth of 10 MHz and the damping factor $\zeta$ of 0.7. Assume $I_{leak} = 0$.

b. Find the open-loop gain T(s) and draw a Bode plot (both amplitude and phase).

c. Calculate the phase margin.

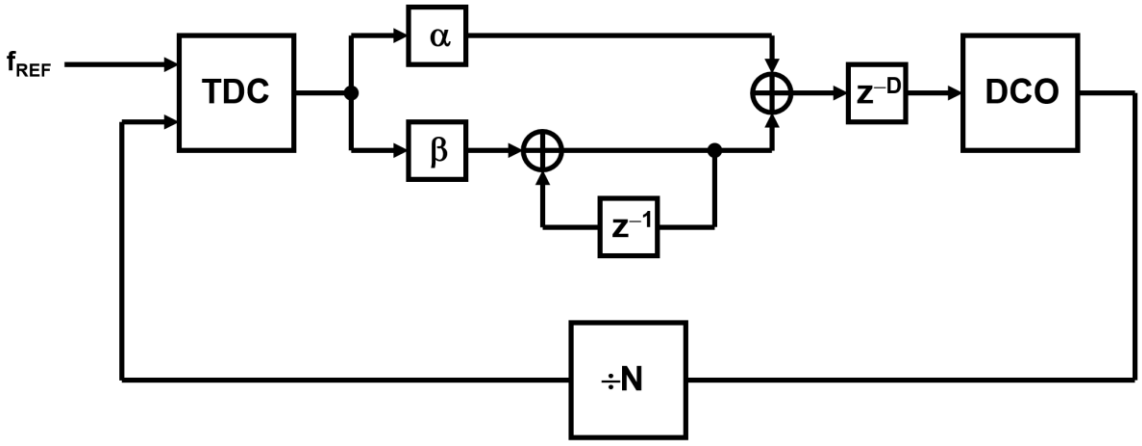
d. Assuming that $I_{cp,up}$=120 uA, $I_{cp,dn}$=80 uA and the PFD's reset delay is 1 ns, calculate the net pulse-width difference Δt between the two PFD output pulses (UP and DN) and plot the resulting $V_{ctrl}$ waveform expected at the steady state. For simplicity, you may ignore the $V_{ctrl}$'s change due to the resistor R.

e. When the $I_{leak}$ = 10 uA, plot the $V_{ctrl}$ waveform and calculate the reference spur. Assuming that charge-pump current ($I_{cp,up}$, $I_{cp,dn}$) is 100uA. For simplicity, you may ignore the $V_{ctrl}$'s microscopic change due to the resistor R. Use the Fourier series of a sawtooth waveform.




$$f(t) = \frac{A}{2} + \frac{A}{\pi}\sum_{n=1}^{\infty}\frac{\sin(n\omega_0 t)}{n}$$

2. Consider an ADPLL with the reference frequency ($f_{REF}$) of 250 MHz and division factor N of 16. The time-to-digital converter (TDC) has a resolution ($\Delta$tdc) of 2 ps/LSB and the digitally-controlled oscillator (DCO) has a resolution ($\Delta f_{DCO}$) of 1 MHz/LSB. Beware of units.



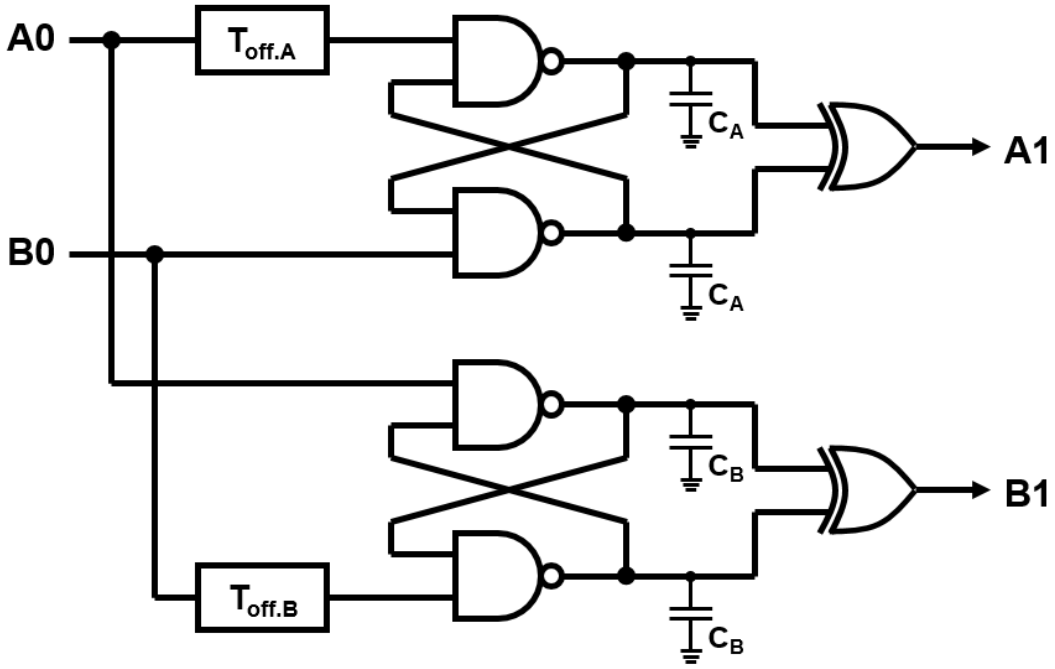

a. Determine $\alpha$ and $\beta$ which make the ADPLL have the open-loop bandwidth of 10 MHz and the phase margin of 60°. Assume $z^{-D} = z^{-0}$.

b. When the $z^{-D}$ exhibits the $z^{-2}$, how much does the phase margin change?

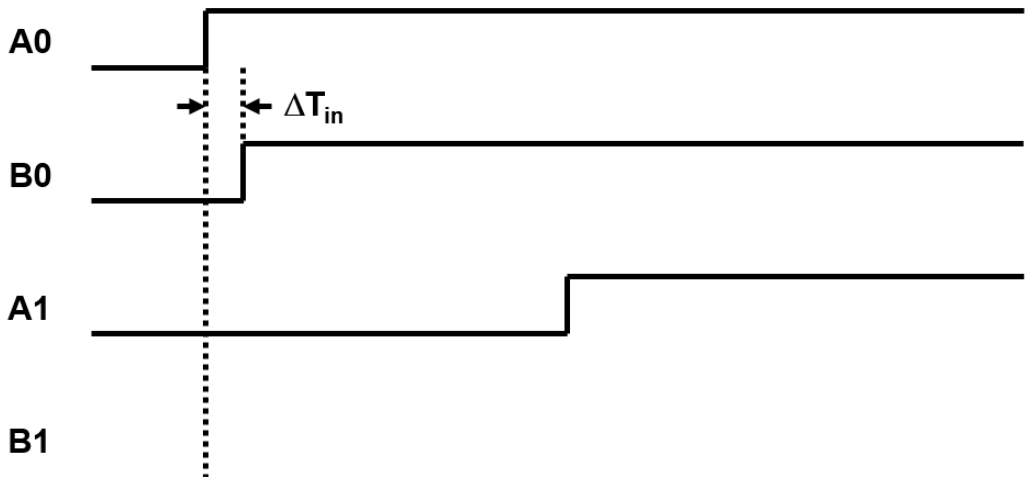
c. Derive the power spectral density function and sketch the phase noise of the output due to the TDC quantization noise.

d. Derive the power spectral density function and sketch the phase noise of the output due to the quantization noise by $\Delta f_{DCO}$.

3. Consider a time amplifier as follows.



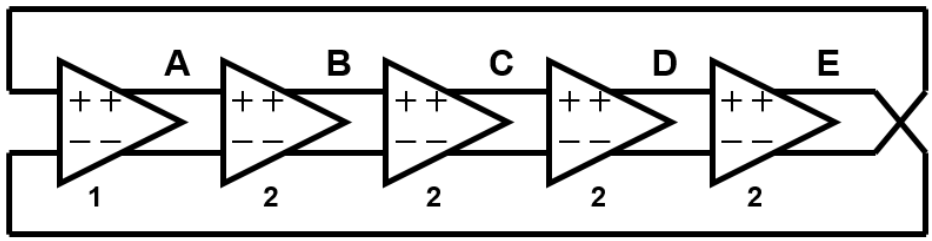

a. Draw the waveform of B1. Assume that $T_{off.B} = T_{off.A} = T_{off}$ and $C_B = C_A = C$. Also assume that the trans-conductance of the NAND output is $g_m$ at the metastable state.

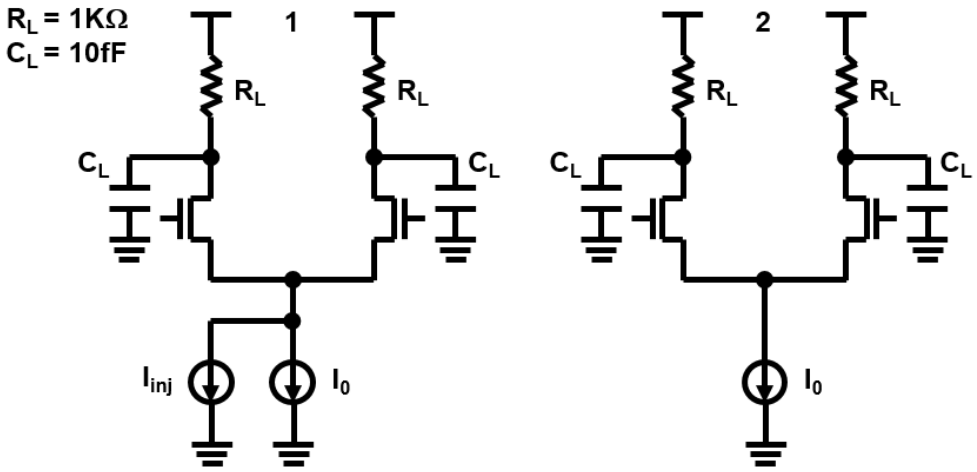


b. When the time offset of input A0 is doubled ($T_{off.A} = 2\ T_{off,}\ T_{off.B} = T_{off,}$), plot the curve ΔTout vs. ΔTin. Assume ΔTin = t(A0)–t(B0) and ΔTout = t(A1)–t(B1).

c. When the capacitance at A1 is doubled ($C_A$=2C), plot the ΔTout vs. ΔTin.

4. Consider a 5-stage ring oscillator. We are designing a divider with an injection-locked oscillator with differential CML inverters. Circuit schematic is as follows. Assume the transistors have ideal characteristics (infinite gain) and the delay is determined by only the resistors and input capacitors. [Ref: Slide 14 of Chapter 4.4]



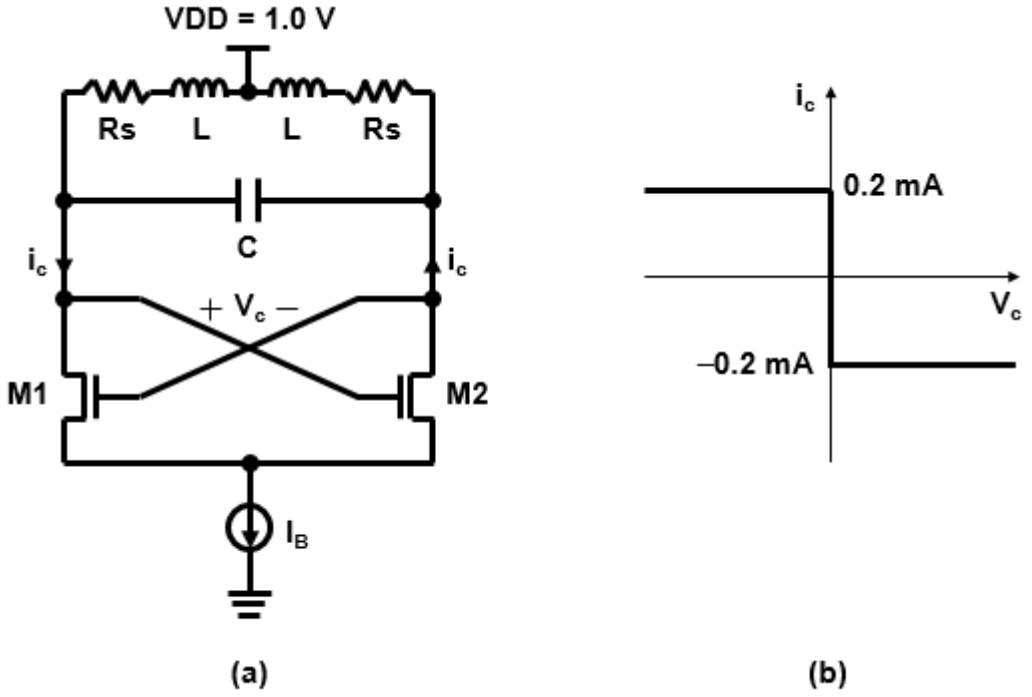

$$I_{inj}(t) = I_{inj0} \cdot \sin(\omega_0 t + \phi_{inj})$$

a. What is the free-running oscillation frequency ($f_{osc}$) of the ring oscillator? Assume $I_{inj} = 0$.

b. When dividing by 2, draw the phasor diagram of A, B, C, D, and E for $\omega_{inj} > 2\pi \cdot 2\, f_{osc}$. Assume $I_{inj0} << I_0$.

c. What is the lock range of this injection locked oscillator? Assume $I_{inj0} = 0.1 \times I_{osc}$.

5. You are to design following LC oscillator. Assume tank inductance (L) of 2 nH, series resistance (Rs) of 0.5 Ω and tank capacitance (C) of 0.25 pF. Beware of units.




a. What is the resonance frequency (fo) of the LC oscillator?

b. What is its equivalent Q factor?

c. Determine the minimum value of the gm of the transistors (M1, M2) to sustain oscillation.

d. When Vc - ic curve is given as (b), What is the amplitude of the output swing?

e. When the gm of M1 and M2 are set to the value calculated in 5.c, derive and plot the single-sideband noise spectral density L(Δf) in equilibrium. Use Leeson's model without flicker noise term and amplitude noise. Use Boltzmann constant of k=1.38064852 × $10^{-23}$ $m^2$ kg $s^{-2}$ $K^{-1}$ and temperature of T=300K. What is its rms period jitter?

6. Read paper “A General Theory of Phase Noise in Electrical Oscillators (Hajimiri)” and answer the question.

   a. ISF 개념을 도입한 이유는?

   b. 저주파에서 문제가 되는 1/f noise 가 high frequency clock 의 phase noise 에 영향을 주는 mechanism 에 대해 (sketch 와 함께) 설명하시오.

   c. 1/f noise 가 phase noise 에 미치는 영향을 줄이기 위한 방법은?

7. **다음 각각의 문제에 대해 설명하시오.** (Internet **에서** copy **하지 말고 나름대로 설명할 것**)

a. Spectrum analyzer **의** dynamic range **를 벗어나는 작은** phase noise **를 측정하는 방법을 설명하시오.**

b. Charge-pump PLL **에서** loop filter **에** $2^{nd}$ capacitor **를 추가로 사용하여** $3^{rd}$-order PLL **을 구성하는 이유는**?

c. DCO **의** quantization noise **를 줄이기 위한** delta-sigma modulator **의 동작 원리에 대해 상세히 설명하시오.**

d. Spread-Spectrum Clock Generator 를 만들 때 PLL 의 bandwidth 는 얼마가 되어야 하나? 그 값을 크게 하기 위한 방법은?

e. Jitter 가 있는 경우의 BBPD gain 을 구하는 방법에 대해 설명하시오.

f. Phase-domain response in injection locking 을 설명하시오.

<End of Mid-term exam>