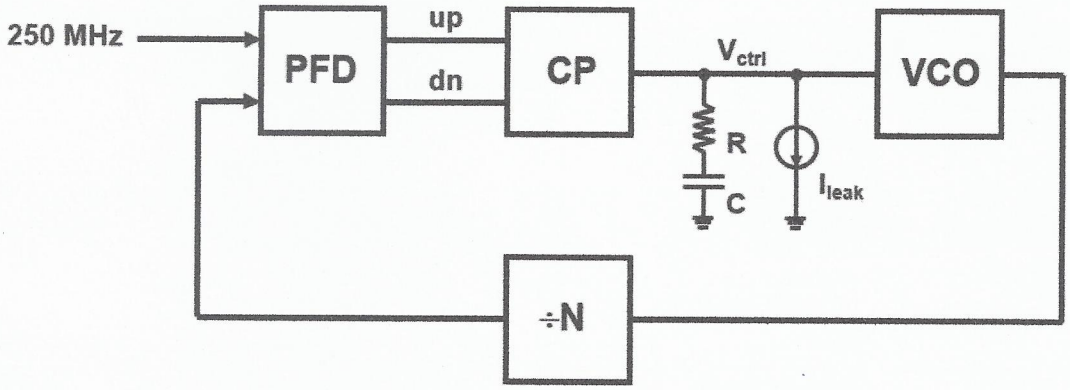
1. For the following charge-pump PLL, assume VCO gain (K_{VCO}) of 1 GHz/V, frequency division factor N of 16 and charge-pump current (I_{cp}) of 100 uA. Beware of units.



a. Determine loop filter parameters R and C that realize the loop bandwidth of 10 MHz and the damping factor ζ of 0.7. Assume $I_{leak} = 0$.

loop bandwidth 정의를 명확히 제시하지 않아,
wn (natural frequency), wc (open loop bandwidth) 중 어느 것으로 계산해도 정답 처리

$$\omega_c = \frac{I_{cp} \cdot K_{vco} \cdot R}{N} = 2\pi \cdot 10 \cdot 10^6$$

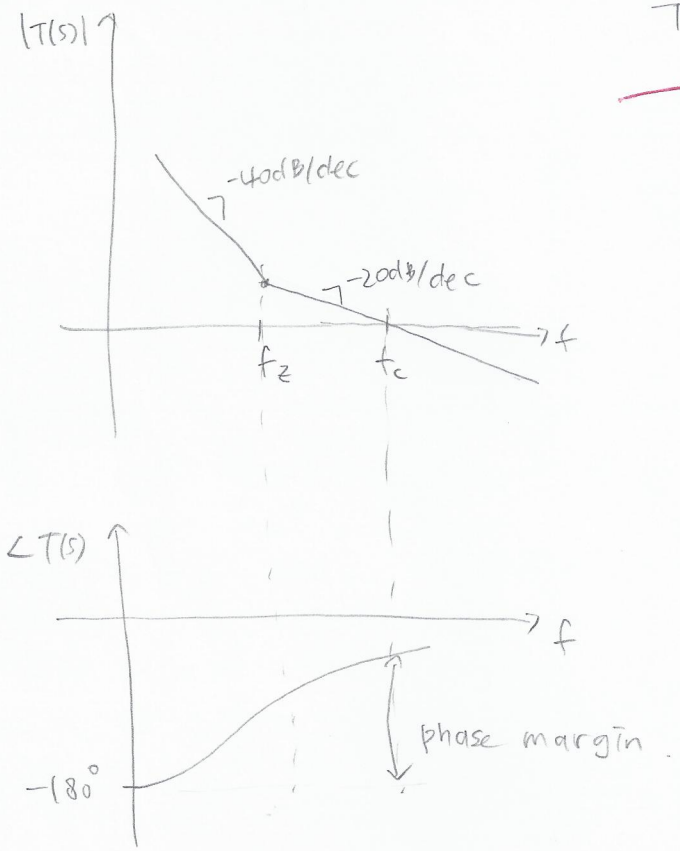
$$\therefore R = 10.05\,k\Omega$$

$$\zeta = \frac{\omega_n}{2} RC = \frac{1}{2}\sqrt{\frac{I_{cp} \cdot K_{vco}}{NC}} \cdot RC = 0.7$$

$$\therefore C = 3.1\,pF$$

수식에서 N 이 누락되거나,
Kvco 에 2pi 를 곱하지 않는 등의 계산 miss 가 많았습니다.

b. Find the open-loop gain T(s) and draw a Bode plot (both amplitude and phase).



$$T(s) = \frac{I_p}{2\pi}\left(R + \frac{1}{sC}\right) \cdot \frac{2\pi \cdot k_{VCO}}{s} \cdot \frac{1}{N}$$

$$= \frac{k_{VCO} \cdot I_p}{C \cdot N} \cdot \frac{s/\omega_z + 1}{s^2}$$

$$\omega_z = \frac{1}{RC} = 3.21 \times 10^7 \text{ rad}$$

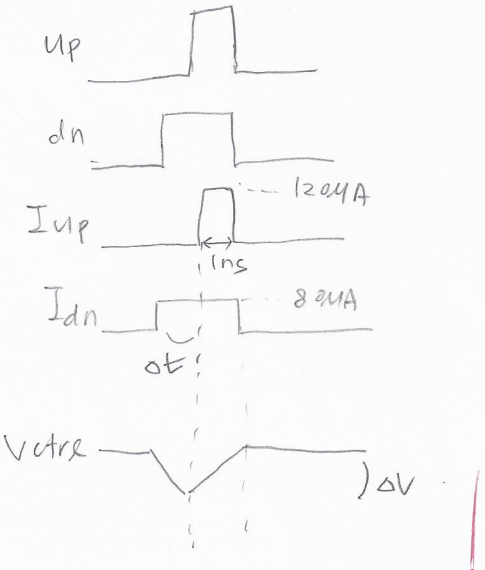
$$\rightarrow f_z = \omega_z / 2\pi = 5.11 \text{ MHz}$$

$$f_c = 10 \text{ MHz}$$

c. Calculate the phase margin.

$$PM = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) = 62.9°$$

d. Assuming that $I_{cp,up}$=120 uA, $I_{cp,dn}$=80 uA and the PFD's reset delay is 1 ns, calculate the net pulse-width difference Δt between the two PFD output pulses (UP and DN) and plot the resulting V_{ctrl} waveform expected at the steady state. For simplicity, you may ignore the V_{ctrl}'s change due to the resistor R.



$\Delta t \cdot 80\mu A = 1ns \cdot 120\mu A$

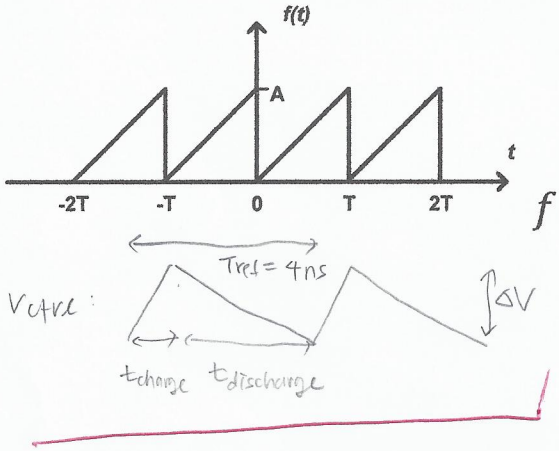
$\therefore \Delta t = 0.5ns$

$Q = C\Delta V = It$

$3.1p \cdot \Delta V = 80\mu \cdot 0.5ns$

$\therefore \Delta V = 12.9\ mV$

e. When the I_{leak} = 10 uA, plot the V_{ctrl} waveform and calculate the reference spur. Assuming that charge-pump current ($I_{cp,up}$, $I_{cp,dn}$) is 100uA. For simplicity, you may ignore the V_{ctrl}'s microscopic change due to the resistor R. Use the Fourier series of a sawtooth waveform.



$$f(t) = \frac{A}{2} + \frac{A}{\pi}\sum_{n=1}^{\infty}\frac{\sin(n\omega_0 t)}{n}$$

$(I_{cp} - I_{leak})\, t_{charge} = I_{leak} \cdot t_{discharge}$

$9 \cdot t_{charge} = t_{discharge}$

$\therefore t_{charge} = 0.4ns,\ t_{discharge} = 3.6ns$

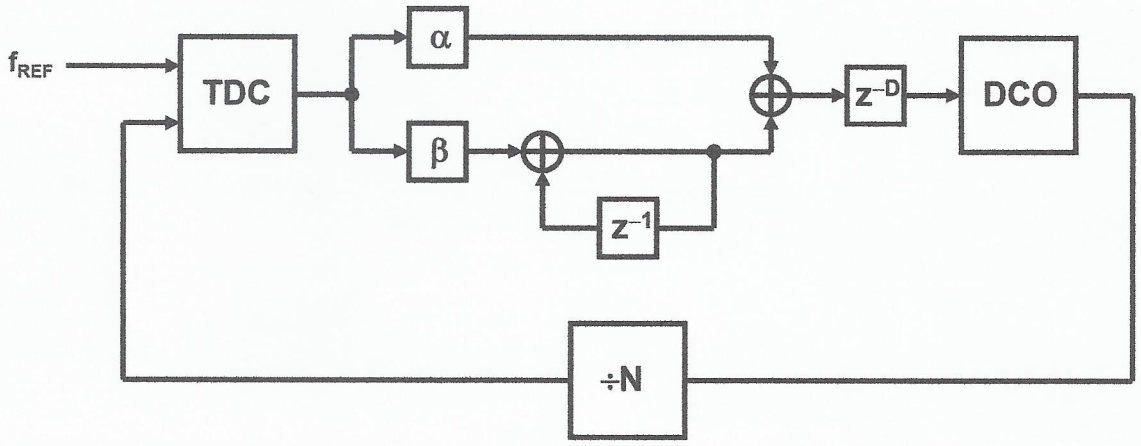
$\Delta V = \frac{90\mu \cdot 0.4n}{C} = 11.6\ mV$

$t_{discharge} \gg t_{charge}$ 가정.

$$\frac{ref\_spur\_fund}{carrier} = 20\log_{10}\left(\frac{K_{VCO} \cdot I_{leak}}{2\pi \cdot C \cdot f_{ref}^2}\right) = -41.71\ dBc$$

$$\frac{ref\_spur\_2nd}{carrier} = 20\log_{10}\left(\frac{K_{VCO} \cdot I_{leak}}{8\pi \cdot C \cdot f_{ref}^2}\right) = -53.75\ dBc$$

2. Consider an ADPLL with the reference frequency (f_{REF}) of 250 MHz and division factor N of 16. The time-to-digital converter (TDC) has a resolution (Δtdc) of 2 ps/LSB and the digitally-controlled oscillator (DCO) has a resolution (Δf_{DCO}) of 1 MHz/LSB. Beware of units.



a. Determine α and β which make the ADPLL have the open-loop bandwidth of 10 MHz and the phase margin of 60°. Assume $z^{-D} = z^{-0}$.

$$\theta = \frac{T_s}{f_{ref}} \cdot \frac{\Delta t_{TDC} \cdot N}{K_{DCO}} \cdot \frac{\omega_{UGBW}^2}{\sqrt{1+\tan^2(PM)}} = 0.063$$

$$\alpha = \beta \cdot \left(\frac{\tan(PM)}{T_s \cdot \omega_{UGBW}} - \frac{1}{2} \right) = = 0.4$$

b. When the z^{-D} exhibits the z^{-2}, how much does the phase margin change?

$z^{-2} \rightarrow e^{-2sT_{ref}}$ 의 delay 추가.

$e^{-2sT_{ref}} \approx 1-2sT_{ref} = 1 - s/f_{ref}/2$ 이게 곱해진다.

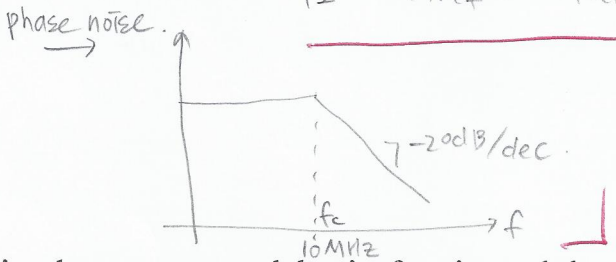
$\therefore \tan^{-1}\left(\frac{\omega_c}{f_{ref}/2}\right) = 26.1^\circ$ 만큼 열화된다.

c. Derive the power spectral density function and sketch the phase noise of the output due to the TDC quantization noise.

$$\sigma^2_{\Phi n,TDC} = \frac{(\sigma t_{TDC})^2}{12} \qquad S_{\Phi n,TDC}(f) = \frac{(\sigma t_{TDC})^2}{12} \cdot \frac{1}{f_{ref}}$$

$$S_{\Phi out,TDC}(f) = \left|\frac{2\pi}{T_{ref}} \cdot H(f)\right|^2 \cdot S_{\Phi n,TDC}(f)$$

$$= \frac{(2\pi)^2}{12} \cdot \left(\frac{\sigma t_{TDC}}{T_{ref}}\right)^2 \frac{1}{f_{ref}} \cdot |H(f)|^2 \quad (H(f): \text{closed loop gain})$$



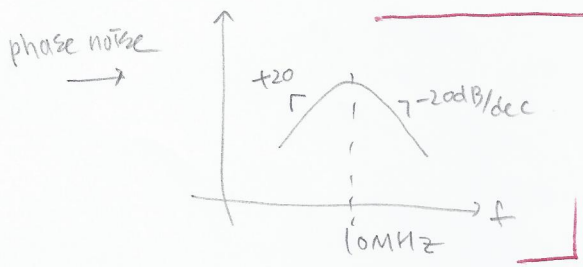
d. Derive the power spectral density function and sketch the phase noise of the output due to the quantization noise by Δf_{DCO}.

$$\sigma^2_{\Phi n,q} = \frac{1}{12} \qquad S_{\Phi n,q}(e^{j2\pi f T_{ref}}) = \sigma^2_{\Phi n,q}\left(\frac{\sin(\pi f T_{ref})}{\pi f T_{ref}}\right)^2$$

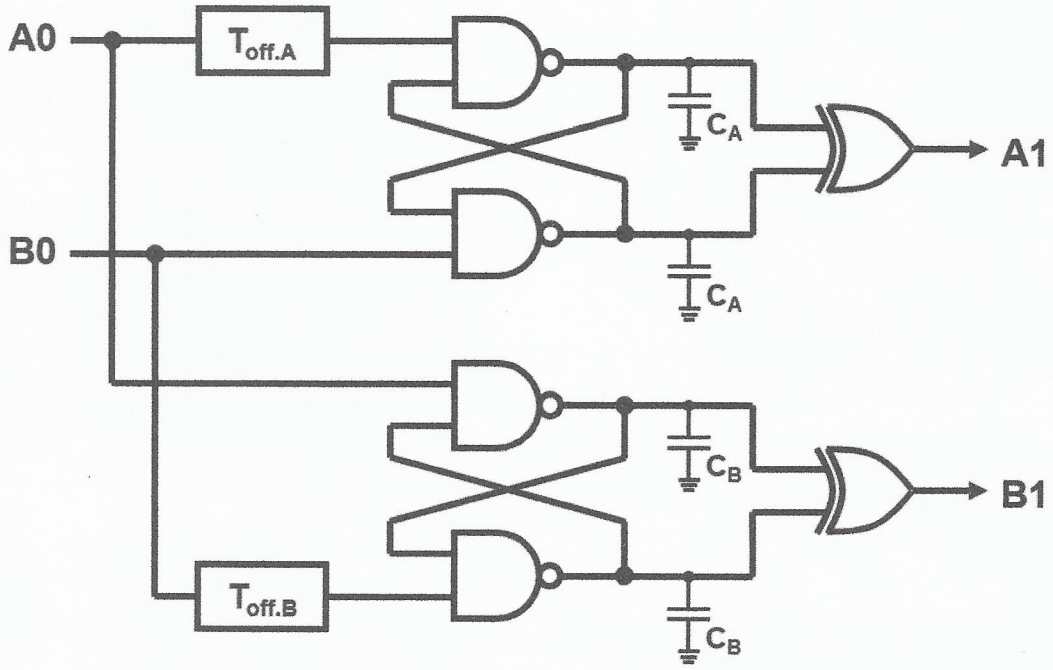
$$\rightarrow S_{\Phi out,q}(f) = \frac{1}{T_{ref}}\left|\left(\frac{T_{ref}\cdot\Delta f_{DCO}}{jf}\right)(1-G(f))\right|^2 \cdot S_{\Phi n,q}(e^{j2\pi f T_{ref}})$$

$$= \frac{1}{12}\cdot\left(\frac{\Delta f_{DCO}}{f}\right)^2 \cdot \frac{1}{f_{ref}} \cdot \left(\text{sinc}\left(\frac{f}{f_{ref}}\right)\right)^2 \cdot |1-G(f)|^2$$

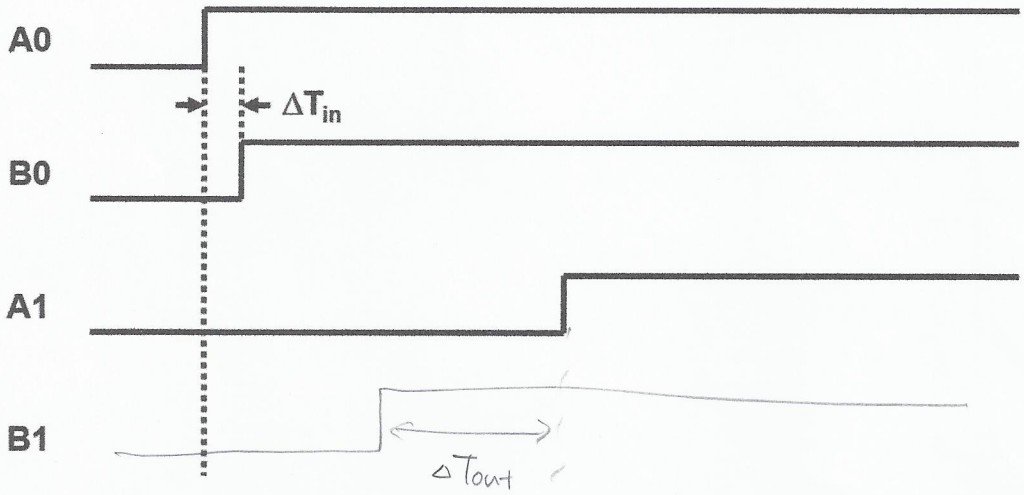
$(G(f) = \frac{1}{N}H(f))$



3. Consider a time amplifier as follows.

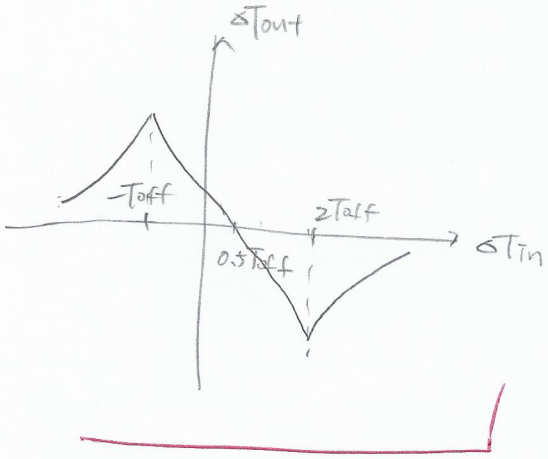


a. Draw the waveform of B1. Assume that $T_{off.B} = T_{off.A} = T_{off}$ and $C_B = C_A = C$. Also assume that the trans-conductance of the NAND output is g_m at the metastable state.

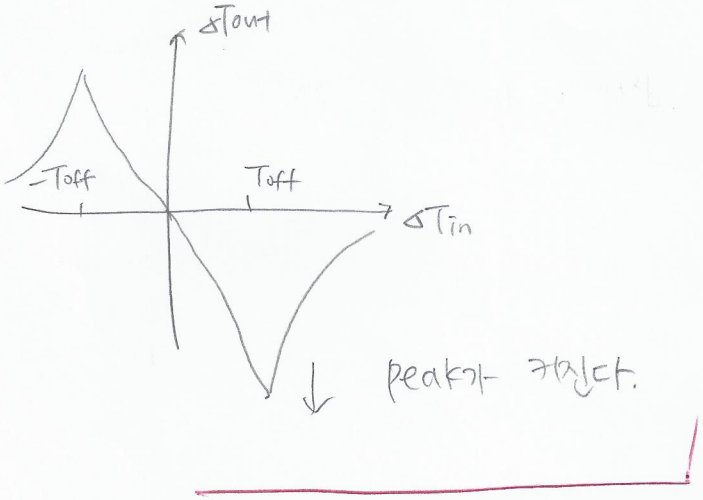


$$\Delta T_{out} = A_T \cdot \Delta T_{in} = \frac{2C}{g_m \cdot T_{off}} \cdot \Delta T_{in}$$

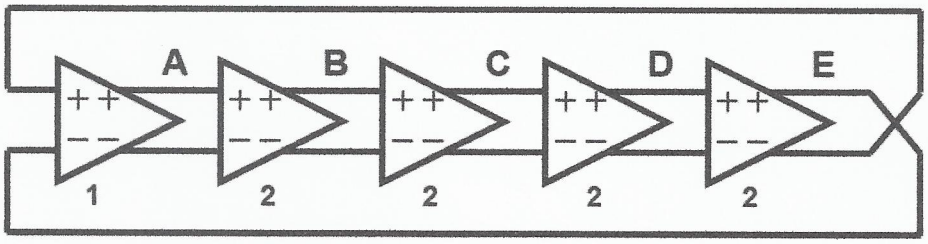
b. When the time offset of input A0 is doubled ($T_{off.A} = 2\ T_{off}$, $T_{off.B} = T_{off}$), plot the curve ΔTout vs. ΔTin. Assume ΔTin = t(A0)–t(B0) and ΔTout = t(A1)–t(B1).

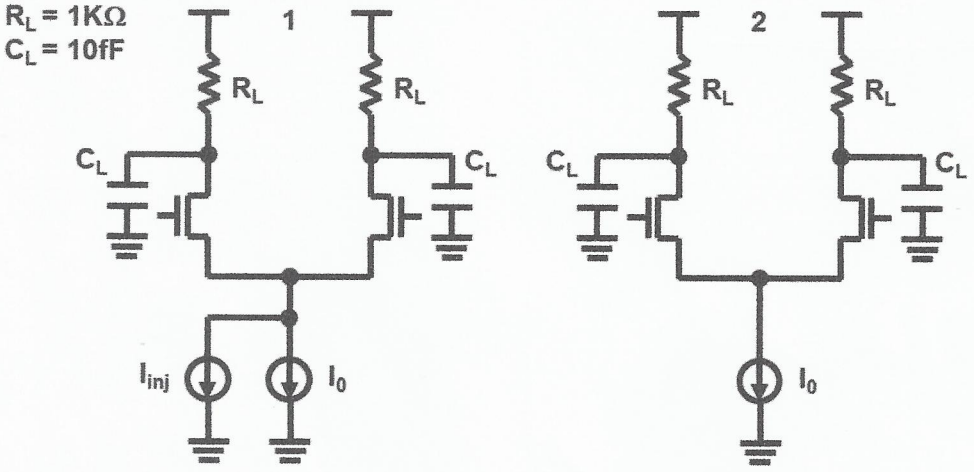


c. When the capacitance at A1 is doubled (C_A=2C), plot the ΔTout vs. ΔTin.



4. Consider a 5-stage ring oscillator. We are designing a divider with an injection-locked oscillator with differential CML inverters. Circuit schematic is as follows. Assume the transistors have ideal characteristics (infinite gain) and the delay is determined by only the resistors and input capacitors. [Ref: Slide 14 of Chapter 4.4]





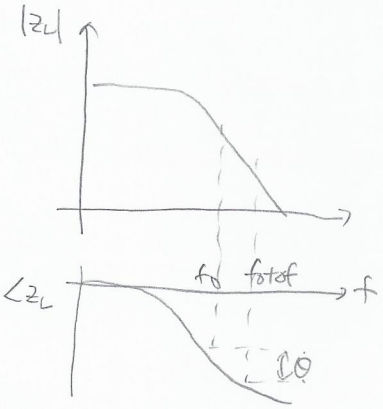
$$I_{inj}(t) = I_{inj0} \cdot \sin(\omega_0 t + \phi_{inj})$$

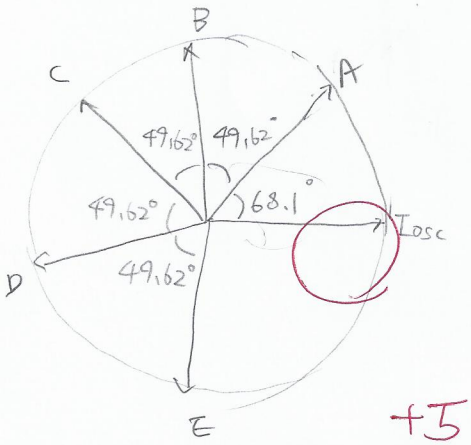
a. What is the free-running oscillation frequency (f_{osc}) of the ring oscillator? Assume $I_{inj} = 0$.

$$f_{osc} = \frac{1}{2N \cdot R_L C_L \ln 2} = 14.43 \text{ GHz}$$

+5

b. When dividing by 2, draw the phasor diagram of A, B, C, D, and E for $\omega_{inj} > 2\pi \cdot 2\, f_{osc}$. Assume $I_{inj0} << I_0$.





+5

$$\theta \approx \frac{\tan\frac{\pi}{N}}{1+\tan^2\frac{\pi}{N}} \cdot \frac{\Delta f}{f_0}$$

$\Delta f = \frac{1}{2} f_0$, $N = 5$

$\therefore \theta = 49.62°$

$\phi = -N\theta = -68.1°$

$\therefore \frac{\pi}{5} + \theta = 49.62°$

c. What is the lock range of this injection locked oscillator? Assume $I_{inj0} = 0.1 \times I_{osc}$.

$$\frac{\Delta f_{out}}{f_0} \le \frac{1}{N} \cdot \frac{1+\tan^2(\pi/N)}{\tan(\pi/N)} \left|\frac{I_{inj}}{I_{osc}}\right| \left(1-\left|\frac{I_{inj}}{I_{osc}}\right|^2\right)^{-\frac{1}{2}}$$

$$= \frac{1}{5} \cdot \frac{1+\tan^2(\pi/5)}{\tan(\pi/5)} \cdot 0.1 \left(1-0.1^2\right)^{-\frac{1}{2}}$$

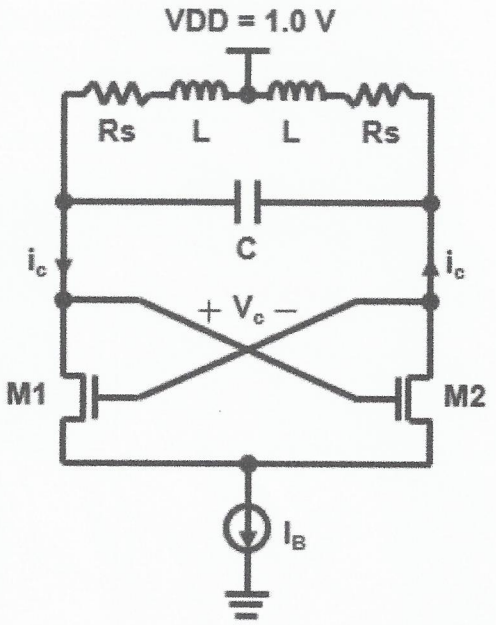
$= 0.042$

$\therefore \Delta f_{out} \le 0.042 \cdot 14.436 = 0.606$ GHz

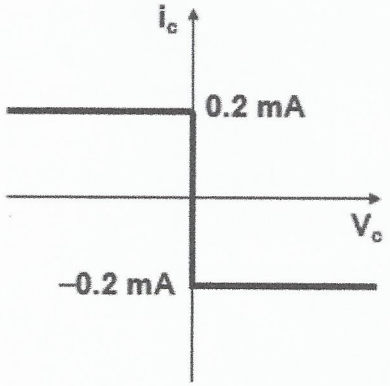
→ 0.606 GHz 이하로 차이 날 때 lock 가능하다.

+5

5. You are to design following LC oscillator. Assume tank inductance (L) of 2 nH, series resistance (Rs) of 0.5 Ω and tank capacitance (C) of 0.25 pF. Beware of units.

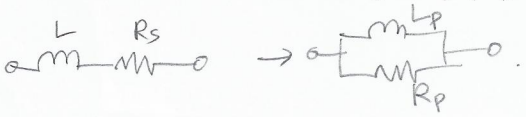


(a)



(b)

a. What is the resonance frequency (fo) of the LC oscillator?



$$sL + R_s = \frac{sL_pR_p}{sL_p + R_p}$$

$$L_p = \frac{R_s^2}{\omega_o^2 L} + L \qquad R_p = \frac{\omega_o^2 L L_p}{R_s}$$

$$\approx L \text{ (high Q)} \qquad \approx \frac{\omega_o^2 L^2}{R_s}$$

$$\therefore \omega_o = \frac{1}{\sqrt{L \cdot 2C}} = 3.16 \times 10^{10}$$

$$f_o = \frac{\omega_o}{2\pi} = 5.03 \text{ GHz}$$

+5

b. What is its equivalent Q factor?

$$Q = \frac{\omega_o L}{R_s} = 126.4$$

+5

c. Determine the minimum value of the gm of the transistors (M1, M2) to sustain oscillation.

$R_p = \frac{\omega_0^2 L^2}{R_s} = 8k\Omega$

$\frac{1}{g_m} < R_p \quad \therefore g_m \geq 0.125 mA/V$

$\therefore min.\ g_m = 0.125 mA/V$ +5

d. When Vc - ic curve is given as (b), What is the amplitude of the output swing?

$V_o = \frac{4}{\pi} I_o \cdot R_p$

$= 2.03 V$ +5

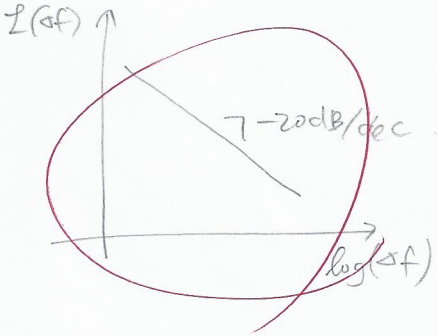
Izgtil maximum amplitude $= 2V_{dd} = 2V$ 이므로

2V

e. When the gm of M1 and M2 are set to the value calculated in 5.c, derive and plot the single-sideband noise spectral density L(Δf) in equilibrium. Use Leeson's model without flicker noise term and amplitude noise. Use Boltzmann constant of k=1.38064852 × 10^{-23} m^2 kg s^{-2} K^{-1} and temperature of T=300K. What is its rms period jitter?

$\frac{\overline{i_n^2}}{\Delta f} = 4kTG = \frac{4kT}{R}$

$\frac{\overline{v_n^2}}{\Delta f} = \frac{\overline{i_n^2}}{\Delta f} \cdot |Z|^2 = 4kTR\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2$



Equilibrium → amplitude & phase noise power 같다.

∴ The amplitude limiting mechanism present in any oscillator removes half the noise

$\Rightarrow L(\Delta f) = 10\log\left[\frac{2kT}{P_{sig}} \cdot \left(\frac{f_0}{2Q\Delta f}\right)^2\right]$ 이때 $P_{sig} = I_{bias}^2 \cdot R_p = 3.2\times10^{-4}$

($I_{bias} \approx 0.2mA$)

$= 10\log\left(\frac{c \cdot f_0^2}{\Delta f^2}\right) \quad (c = 4.05\times10^{-22})$

$\therefore J = \sqrt{cT} = 2.84\times10^{-10}\ s$ +5

6. Read paper "A General Theory of Phase Noise in Electrical Oscillators (Hajimiri)" and answer the question.

a. ISF 개념을 도입한 이유는?

impulsive input → phase noise에 step change가 생김

즉, oscillator는 time varying system.

∴ time varying system을 설명하기 위해 도입했다.

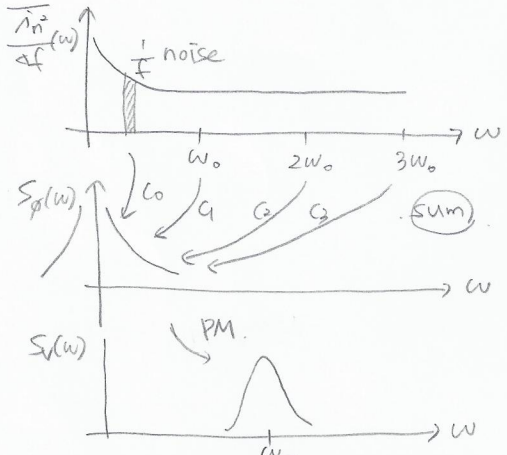
이때 ISF는 oscillator의 phase $w_0\tau$에 inject되는 impulse에 대한 sensitivity 정보를 나타낸다.

+5

b. 저주파에서 문제가 되는 1/f noise 가 high frequency clock 의 phase noise 에 영향을 주는 mechanism 에 대해 (sketch 와 함께) 설명하시오.

$$\Gamma(w_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(nw_0\tau + \theta_n)$$

$$\phi(t) = \frac{1}{q_{max}}\left[\frac{c_0}{2}\int_{-\infty}^{t} i(\tau)d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau)\cos(nw_0\tau)d\tau\right]$$



dn converting 시키고

up converting 시켜서

high frequency에 영향을 준다.

+5

c. 1/f noise 가 phase noise 에 미치는 영향을 줄이기 위한 방법은?

$$c_0 = \frac{1}{\pi}\int_0^{2\pi} \Gamma_{eff}(x)dx \quad \rightarrow \text{1/f noise} \propto c_0.$$

∴ c_0를 줄이자!

- rise/fall time을 똑같이 한다. (symmetry)
- 50% duty로 만든다.
- rise/fall time을 빠르게 한다.

+5

7. **다음 각각의 문제에 대해 설명하시오. (Internet 에서 copy 하지 말고 나름대로 설명할 것)**

a. Spectrum analyzer **의** dynamic range **를 벗어나는 작은** phase noise **를 측정하는 방법을 설명하시오.**

frequency 가 너무 큰 경우에는 divide 한 clock 을 넣어
그 clock 의 jitter 를 측정하고,
frequency 가 너무 작은 경우에는 multiply 한 clock 을 넣어
그 clock 의 jitter 를 측정한다.

divide or multiply 하면 phase noise 는 변하지만
jitter 는 유지되기 때문에 jitter 를 측정해서 적절하게
phase noise 로 변환한다. +5

b. Charge-pump PLL **에서** loop filter **에** 2nd capacitor **를 추가로 사용하여** 3rd-order PLL **을 구성하는 이유는?**

2nd order PLL 을 사용하는 경우 Vctrl 의 ripple 이 너무 심하다.
그래서 capacitor 를 추가하여 Vctrl 을 더 smooth 하게 만든다.

+5

c. DCO **의** quantization noise **를 줄이기 위한** delta-sigma modulator **의 동작 원리에 대해 상세히 설명하시오.**

DCO 의 control code 를 fref 기준으로 update 하면 output
frequency 가 너무 느리게 변한다. 따라서 DSM 을 통해
update 를 더 자주할 수 있도록 만들어준다.
이 때 두 sample 의 quantization error 를 구한 후,
그것을 다음 sample 에서 빼주어서 일반적인 ADC 보다
quantization noise 를 줄일 수 있다.

+5

d. Spread-Spectrum Clock Generator 를 만들 때 PLL 의 bandwidth 는 얼마가 되어야 하나? 그 값을 크게 하기 위한 방법은?

VCO 측면에서 PLL은 High pass Filter 이므로

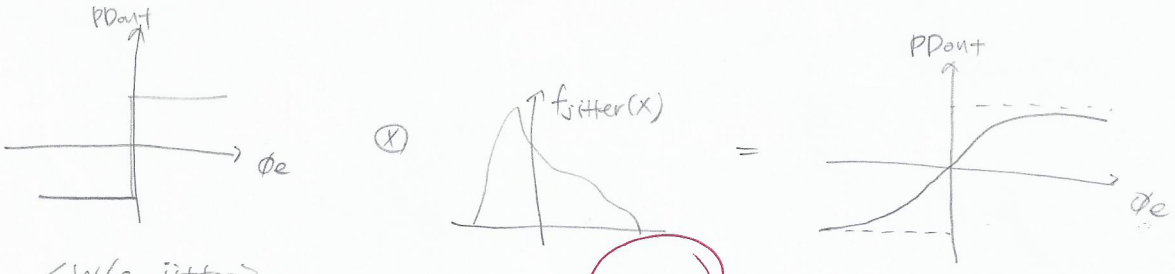
PLL의 BW는 modulation frequency 보다 충분히 작아야한다.

PLL의 BW를 크게 하려면 2 point modulation을 통해

$\Delta\phi$를 보정하는 방법을 사용하면 된다. +5

그리고 ref_clk을 SSCG 시킨다면 LPF 이므로 harmonic 성분을 제거하지 않도록 10. modulation frequency 보다 커야한다.

e. Jitter 가 있는 경우의 BBPD gain 을 구하는 방법에 대해 설명하시오.



<w/o jitter>

+5

jitter가 없는 PD gain 과 jitter의 함수를

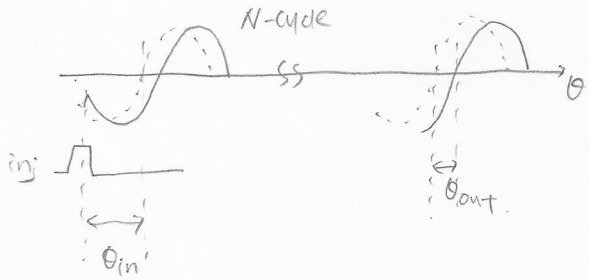
convolution 한다.

f. Phase-domain response in injection locking 을 설명하시오.

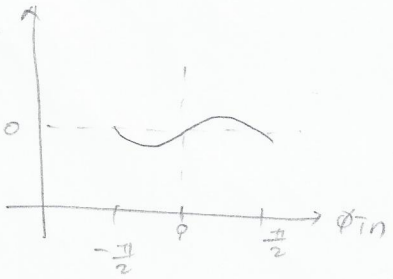
PDR = phase 변화에 대한 응답 ($\theta_{in} \rightarrow \theta_{out}$)

injection 시점에 따라 +5

위상특성이 달라 질 수 있다.



ex) ϕ_{out}



<End of Mid-term exam>