MEMS Process and Design
- release recipe -

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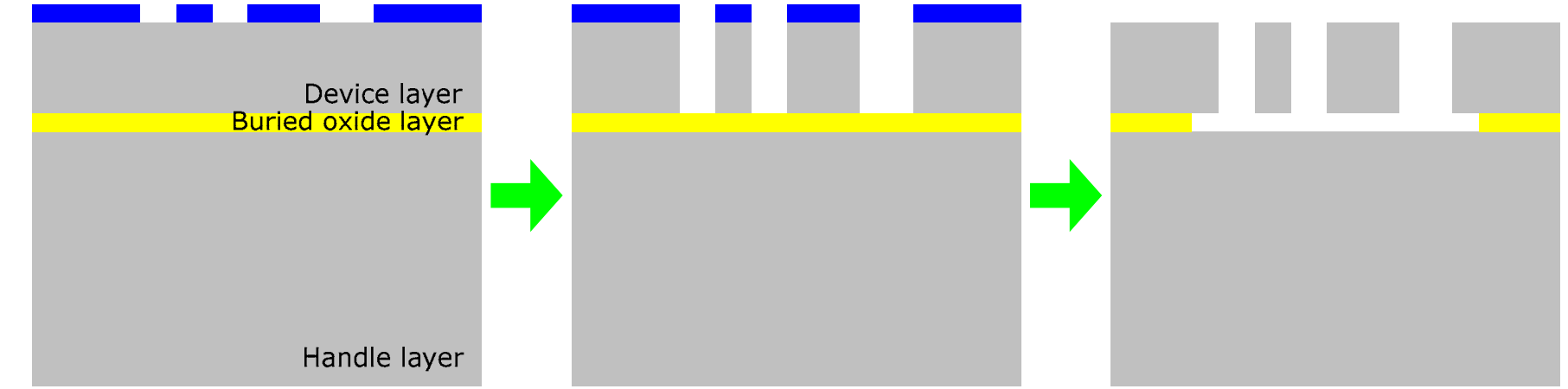
SOI Process

- Silicon On Insulator (SOI) Process
  - Vertical dimension of structures are defined by deep Si RIE
  - Structures are released by removal of buried oxide layer



Process Recipe

Seq.	Process	Condition
10	TEOS dep.	2 um deposition at P-5000 I
20	Photo	MA6 aligner
30	TEOS etch	2 um etch at P-5000 I (10% over etch)
40	PR strip	H_2SO_4 bath, Ashing
50	Deep Si etch	70 um ± 10 % etch (4 um X 20 um etch hole)
60	Dicing	
70	Release	Acetone (20 min) → Methanol (5 min) → Rinse (10 min) → HF (approximately 7 min) → Rinse (10 min) → Boling IPA (5 min) → Oven dry (5 min)

Further Work

- Release report: 2008. 5. 24
  - SEM image (individual work)
  - Report should be 4~5 pages of PPT
  - Should include,
    1) Thickness of spring
    2) Thickness of mass
    3) Footing phenomenon
    4) Etch lagging
    5) Midterm report of measurement results
    6) Etc

- Measurement : 2008. 5. 16 ~ 5. 31
- Final presentation & Final report due : 2008. 5. 31