Pushing the limits of lithography

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The phenomenal rate of increase in the integration density of silicon chips has been sustained in large part by advances in optical lithography — the process that patterns and guides the fabrication of the component semiconductor devices and circuitry. Although the introduction of shorter-wavelength light sources and resolution-enhancement techniques should help maintain the current rate of device miniaturization for several more years, a point will be reached where optical lithography can no longer attain the required feature sizes. Several alternative lithographic techniques under development have the capability to overcome these resolution limits but, at present, no obvious successor to optical lithography has emerged.

The integration density of devices on a silicon chip has been increasing steadily for over three decades, driven by a combination of market forces and technological innovation. The rate of increase is approximately 50% per year in the case of dynamic random-access memories (DRAMs) and 35% per year for microprocessors. And the resulting improvements in chip performance have gone hand in hand with increases in chip yield and reduction in the cost per chip. Underlying these developments are advances in lithography — the technology by which the fine-scale patterns required for the fabrication and integration of the component devices are generated.

Lithographic requirements differ from chip to chip. The fabrication of DRAM chips has traditionally required the most advanced lithographic techniques, and the half-pitch (essentially the separation between neighbouring memory 'cells' on the chip) remains an important practical constraint in the fabrication of DRAMs. But more recently, the significant commercial pressure for increased performance and expansion of market size has resulted in the development of microprocessors, high-end logic large-scale integrated (LSI) circuits, and 'system-on-a-chip' LSI circuits that each use smaller-scale patterning than the contemporary generation of DRAMs. This is exemplified by the minimum gate length of the component transistors of microprocessors, which ultimately determines the speed with which these chips can process information. For example, the current generation of commercial microprocessors has operational speeds in excess of 500 MHz, whereas 33 MHz was the norm barely 10 years ago.

The past three decades have seen the critical length-scales of the component devices decrease by a remarkable amount, from 15 μm in the case of the first integrated circuit, to the 180 nm routinely obtained today. Yet the means by which these circuits have been patterned has, at least in a qualitative sense, remained the same: optical lithography. Can this phenomenal rate of increase in integration density be sustained indefinitely? The answer is clearly negative, in the sense that the size of the constituent atoms imposes a fundamental limit on the minimum length scale that can be ultimately attained. But even if the current rate of miniaturization continues apace, this fundamental limit remains many years off: the challenges faced by the microelectronics industry are more immediate.

The purpose of this review is therefore essentially twofold. First, through an overview of the fundamentals of optical lithography, we will show how minimum attainable device dimensions are intimately (but not exclusively) related to the wavelength of light used, and we describe several techniques under investigation for further enhancing the resolution of this workhorse of the microelectronics industry. However, as the options available to industry are not all optical, we will also discuss the various non-optical lithographic techniques that are being explored. Figure 1 illustrates how the lithographic options vary as the critical device dimension decreases, and provides estimates of the timescales on which decisions may need to be made regarding which option(s) to adopt[1]. A shift by the microelectronics industry to any non-optical lithographic technique will require the introduction of a new infrastructure of tools, materials and processing technologies, the research and development costs of which will be enormous.

Projection optical lithography

The key elements of a practical lithographic system are essentially the same for all technologies, optical and non-optical. They include the following. (1) A set of 'masks' containing the patterns of components to be fabricated in and/or on the semiconductor, the tools for making the masks, and the metrology for ensuring precise dimensions and pattern overlay. (2) An energy source (for example, a light source) for transferring the pattern from a mask to the semiconductor. (3) A medium — known as a 'photoresist' or 'resist' — for recording the pattern on the semiconductor following exposure to the source, and which allows subsequent processing of material in and/or on the underlying semiconductor. (4) Procedures for reliable detection of pattern defects, which clearly become more challenging as the critical dimensions decrease. The lithographic process — especially projection optical lithography — is closely related to the developing process in print photography, where the photographic negative has the role of the mask, and the photographic emulsion on the print is the resist.

Resolution limits

The resolution limit in conventional projection optical lithography is determined largely by the well-known Rayleigh's equation. The resolution (minimum resolvable feature) R and the corresponding depth of focus (DOF) are given by the following[2]:

$$R = k_1 \cdot \lambda / \mathrm{NA}$$

$$\mathrm{DOF} = k_2 \cdot \lambda / \mathrm{NA}^2$$

Here λ is the exposure wavelength, NA is the numerical

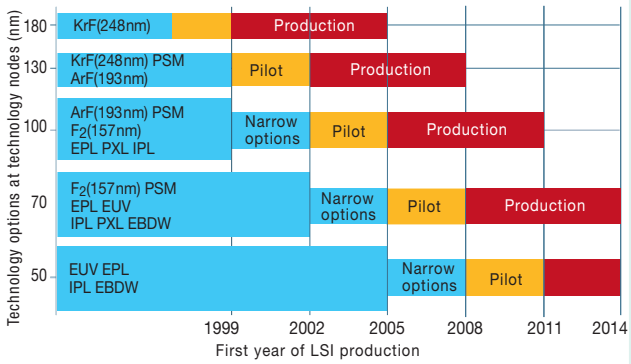

Figure 1 Technological trends in lithography. Shown are the various technologies under investigation for the development of pilot and production lines of LSI circuitry. These include: KrF (248 nm), KrF excimer laser lithography with wavelength 248 nm; ArF (193 nm), ArF excimer laser lithography with wavelength 193 nm; F_2 (157 nm), F_2 excimer laser lithography with a wavelength of 157 nm; PSM, phase-shifting mask applied to KrF, ArF and F_2; EPL, electron-projection lithography; PXL, proximity X-ray lithography; IPL, ion-projection lithography; EBDW, electron-beam direct writing.

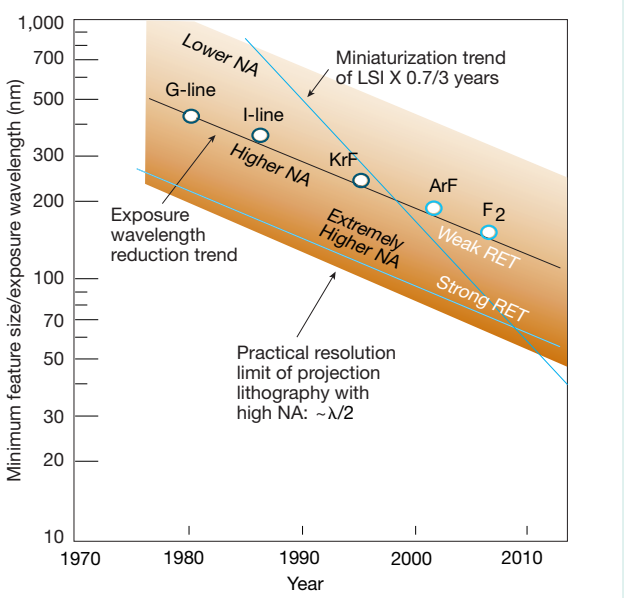

Figure 2 Comparison of trends in the wavelength of exposure light and the minimum feature size of LSI devices. The miniaturization trend is steeper than the rate at which exposure wavelengths have been reduced, illustrating the increasing practical importance of high-numerical-aperture (high-NA) systems and strong resolution-enhancement techniques (RETs). G-line and I-line refer to earlier exposure wavelengths.

aperture of the optical system, and k_1 and k_2 are constants that depend on the specific resist material, process technology and image-formation technique used. Figure 2 shows the evolution of projection optical lithography. It compares the trend of minimum feature size with that of the wavelength of the exposure light. When the projection system was first introduced, the required minimum feature size was relatively large compared to the wavelength of the exposure light. The numerical aperture of the lens system used was also rather small. However, as the rate of device miniaturization has proceeded faster than the rate of reduction of the exposure wavelength, projection systems with higher resolving capabilities are now required.

To obtain higher resolutions, shorter wavelength light and lens systems with larger numerical apertures can be used. In general, the minimum feature size that can be obtained is almost the same as (or slightly smaller than) the wavelength of light used for the exposure, for which one needs a relatively large numerical aperture (typically $\geqslant 0.5$). In such high-NA lens systems, the depth of focus becomes very small, and so the exposure process becomes sensitive to slight variations in the thickness and absolute position of the resist layer[3]. (The smaller the depth of focus, the more rapidly a focused beam diverges on moving away from the focal point.) With the recent introduction of a 'chemical mechanical polishing' technology, the topographic variations of semiconductor surfaces have been reduced, making it possible to use extremely large NA systems; however, the margin for error becomes minute under such high-NA exposure conditions.

Resolution enhancement

To improve the resolution of an optical lithography system without introducing other impractical constraints (on, for example, wafer smoothness), several resolution-enhancement strategies have been proposed[4–6]. Figure 3 shows a schematic view of a typical projection optical-exposure system. Such a system consists of several subsystems, and resolution-enhancement ideas can be applied at various points. These ideas generally amount to manipulating — or 'engineering' — the wavefront of the light used, and may take the form of modified illumination at the light source, phase shifting of the wavefront in the mask plane, and/or filtering with an aperture (pupil) at the projection lens. Some basic ideas of resolution enhancement are illustrated in Fig. 4, which compares image formation in the conventional system with phase shifting and modified illumination.

Consider the case when the image on the mask is a simple grating. In the conventional system (Fig. 4a), several diffracted light rays are generated by the grating. Zeroth-order light proceeds straight through the system, and several rays of higher order are generated with diffraction angles of θ (first order), 2θ (second order), 3θ (third order) and so on, with $\theta \approx \lambda/a$ for small θ (where a is the grating periodicity). Near the resolution limit, only the zeroth-order and first-order rays pass through the lens pupil: the transmission of at least two rays is required in order to reconstruct an image of the grating from their subsequent recombination.

Now consider the case in Fig. 4b, where the phase of the light passing through the grating mask is modified to have a periodicity twice that of the grating itself. (Phase shifting also requires a higher degree of coherency in the source light compared to the conventional case.) The transmitted wavefront is in turn modified such that the zeroth-order light is cancelled out and the diffraction angle of the first-order rays halved to 0.5θ. As a result, the spatial frequency of the patterns that can be imaged is doubled (or, put another way, the resolvable grating periodicity is halved). Although both the opaque pattern and the phase modifications on a real mask will be considerably more complex than a simple grating, this example nevertheless serves to illustrate the substantial improvement in resolution that can be achieved by this approach. Figure 5 shows resist patterns formed using KrF (248 nm) light and a phase-shift mask: structures having half the wavelength of the exposure light are clearly visible.

Finally we consider oblique (or off-axis) illumination, as shown in Fig. 4c. Zeroth-order light no longer passes through the centre of the pupil, but at an angle to the vertical. The first-order rays again emerge at angles of $\pm\theta$ with respect to the zeroth-order ray. And at the resolution limit, one of these passes through the side of the lens pupil opposite to that of the zeroth-order ray, whereas the other diffracted ray is blocked. The result is therefore geometrically equivalent to the phase-shifted case, and again leads to a doubling of the spatial frequency of the images that can be resolved.

At present, the most advanced mass-produced LSI circuits have a critical dimension of 180 nm. This is achieved by using partially coherent light from a KrF excimer laser with a wavelength of 248 nm, in combination with some resolution-enhancement techniques such as off-axis illumination, phase-shift mask, and optical proximity correction as well as advanced resist systems. To further reduce the

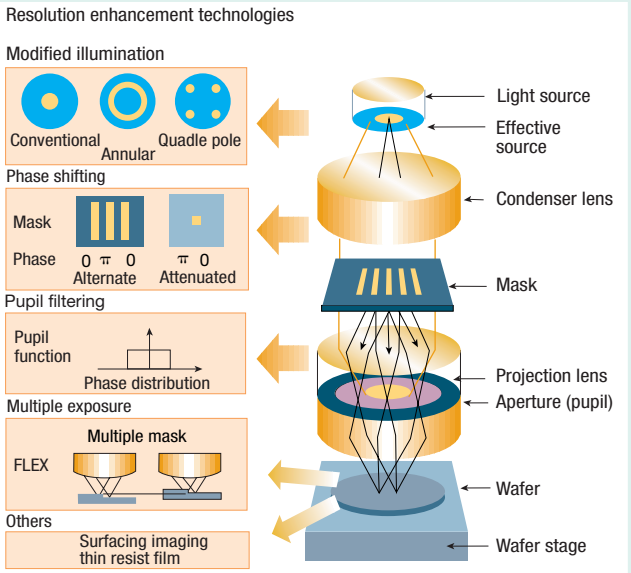

Figure 3 Schematic view of a typical exposure optical system. Resolution-enhancement techniques may be applied at various points in the optical path, as illustrated to the left of the figure.

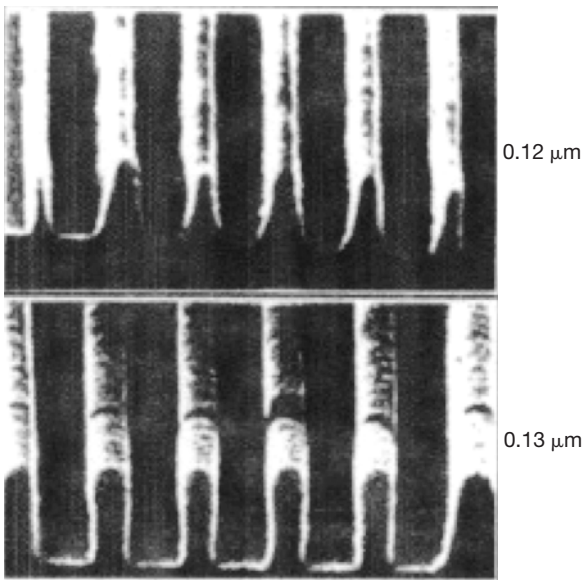

Figure 5 An example of resolution enhancement using phase-shifting technology. The exposure system uses a KrF excimer laser ($\lambda = 0.248$ μm; NA = 0.55; $\sigma = 0.3$). Structures having half the wavelength of the exposure light are clearly visible.

critical dimension, wavelength reduction is being actively pursued using ArF and F_2 excimer lasers (wavelengths of 193 nm and 157 nm, respectively). The combination of shorter-wavelength light and resolution-enhancement techniques should ensure optical lithography's position as the most practical technology for LSI fabrication for at least the next 5 years.

Electron-beam lithography

Electron-beam lithography — whereby a beam of electrons rather than photons is used as the exposure source — has extremely high-resolution capabilities combined with a large depth of focus. To date, it has been used mainly in the production of masks and reticules for optical lithography. But it has also been used in the fabrication of very fine scale devices for fundamental and device-verification studies, and in the small-scale production of the specialized very high frequency devices. However, in the context of mass-produced LSI circuitry, the largest problem of electron-beam lithography is the low throughput capability of the system. Although using a finely focused electron beam makes it possible to delineate extraordinarily fine patterns, writing of chip-scale patterns with a single electron beam is a slow process. And as the complexity and finesse of mask patterns has increased, even the use of electron-beam lithography for mask writing has become prohibitively slow.

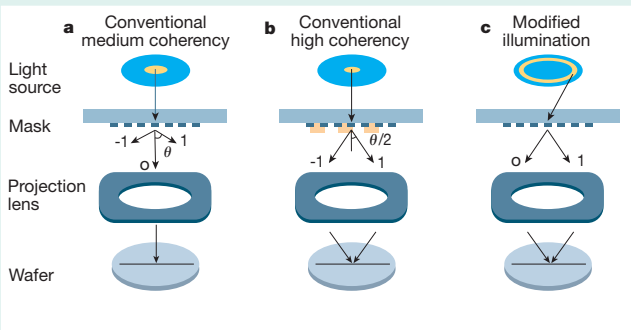

Figure 4 Grating pattern image formation using resolution enhancement. **a**, Conventional projection optics; **b**, with a phase-shifting mask; **c**, with oblique (annular) illumination.

There has accordingly been considerable interest in developing techniques to expand the throughput of electron-beam lithography, and these have generally involved finding ways to enlarge and shape the electron beam. For example, the ability to vary the size and (rectangular) shape of the electron beam during the writing process means that the writing time is not overly sensitive to the minimum feature size: coarser features can be written with a larger beam during a single pass. But to further reduce the writing time, several areas of the pattern need to be exposed in parallel.

The cell-projection system is one such approach that makes use of parallel exposure[7]. In a conventional variable-shaped beam system, the maximum size of the electron beam is sufficient to encompass a mask containing the pattern of several memory cells (which have a repetitive structure). This can therefore be projected on the semiconductor wafer in a single exposure. Figure 6 shows a resist pattern produced by this approach: the periodically arrayed patterns at the top are produced by exposure using a cell-projection aperture, whereas the random wiring patterns at the bottom were written using a variable-shaped beam. But even with this system, throughput remains a critical issue.

A more promising approach to improve throughput is to use a projection optical system that is geometrically equivalent to that used in optical lithography: the image of an arbitrary LSI circuit is projected from a mask. Most notable of the recent attempts to use mask projection are SCALPEL (scattering angular-limited projection electron-beam lithography, developed by Bell Laboratories)[8] and PREVAIL (projection reduction exposure with variable-axis immersion lenses, developed by IBM)[9].

A conceptually related technique is that of ion-projection lithography (IPL), in which the electron beam is replaced by an ion beam. In principle, the much higher mass of ions should result in imaging capabilities that are less prone to distortions due to back-scattering from the substrates. But high-resolution ion-beam systems remain in a primitive state of development compared to that of electron-beam systems.

Proximity X-ray lithography

Proximity lithography is essentially a form of 'shadow printing' — a mask is held in close proximity to the semiconductor surface, and the image is simply produced on exposure by the shadow of the mask on

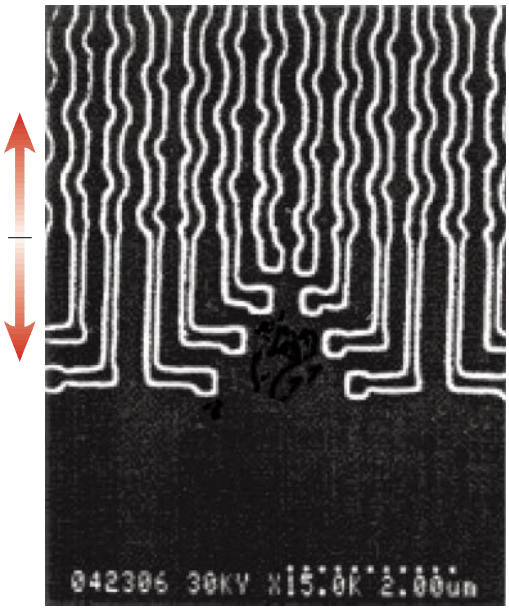

Figure 6 Resist patterns delineated by the cell-projection system. Above the indicated line are periodic patterns (memory cell patterns) exposed using cell-projection apertures; below the line are non-periodic patterns individually exposed using a variable-shaped beam (peripheral circuits patterns).

the surface. Proximity techniques were used in the early days of optical lithography, but have long since been superseded by projection techniques: the former are more susceptible to resolution-limiting diffraction effects. Resolution is less of an issue with proximity printing using X-rays, as the wavelengths used are so much smaller (~1 nm). In the exposure system for proximity X-ray lithography, X-rays are first collimated using a silicon carbide mirror, and are then passed through a transparent window of beryllium into a chamber containing the mask and wafer. The mask is prepared on a membrane of silicon carbide or diamond, and a layer of tantalum (patterned by direct-write electron-beam lithography) serves to absorb the X-rays and so generate the shadow on the semiconductor wafer.

Figure 7 shows a series of typical patterns produced in the resist layer following X-ray exposure and subsequent development[10]. The patterns shown were formed on stepped substrates, and exhibited critical dimensions as small as 150 nm with a distribution of less than 10 nm (3σ). The final image of 100-nm node patterns demonstrates the promise of proximity X-ray lithography as a candidate for the next-generation lithographic process in LSI production. But to realize this promise, several key issues remain, such as the requirement for tight control over the mask–substrate separation (~15 nm) and high initial investment in equipment and infrastructures such as mask supply.

Extreme ultraviolet lithography

Extreme ultraviolet (EUV) lithography is a strong candidate for achieving critical dimensions of 70 nm and below[11,12]. This approach uses the same principle of conventional optical-projection lithography and also obeys Rayleigh's equation shown earlier. But now the exposure wavelength is in the range 11–13 nm, which introduces its own problems.

First, as the absorption of light in this short-wavelength regime is very strong, lens-based refractive optics cannot be used in this lithographic system: an all-reflective optic system must therefore be used. A second difficulty relates to the mirrors themselves. A conventional mirror surface cannot be used at these wavelengths, so one must resort to multilayer structures that rely on interference effects to achieve reflectivity. And even then, the resulting reflectivities are rather low, typically around 60–70% at 13 nm. Accordingly, the number of mirror surfaces in the system needs to be kept as low as possible — six or fewer — to avoid significant reductions in the light intensity level.

In the case of multilayer mirror optics, the requirement of fewer optical elements means that aspherical mirrors must be introduced to achieve such capabilities. Such aspherical mirrors need to be extremely precise, with figure errors and surface roughness less than 0.1–0.2 nm. As such, an extremely high precision metrology system needs to be developed if this approach to lithography is to become viable.

The source of EUV light is another problematic issue[14]. At present, the best candidate is a laser-produced plasma of xenon gas. But the energy conversion ratio of laser light (from a YAG laser) to EUV light is so small that lasers of enormous power are required to achieve practical EUV exposure intensities. Different strategies, such as the use of electrical discharge lamps, are therefore being explored for providing practical light sources for EUV lithography[15].

Figure 8 shows a pattern produced by an experimental EUV exposure system: 70-nm patterns are clearly delineated[13]. The insertion time for EUV lithography is thought to be 2007–2008 (see Fig. 1), leaving several years to address the practical requirements of this technology.

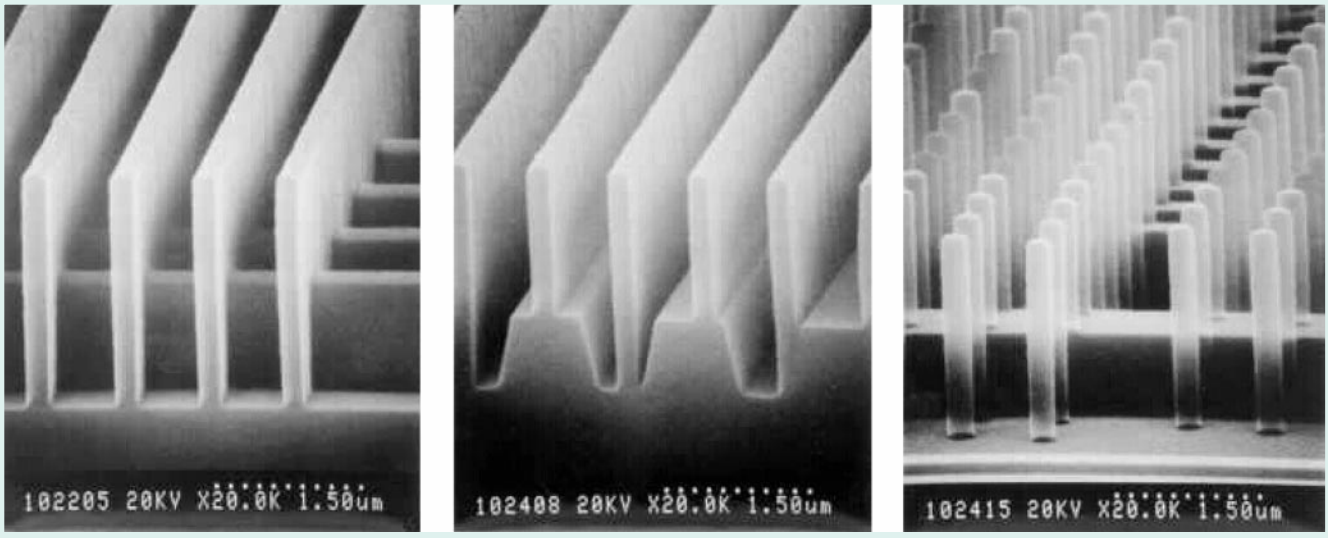

Figure 7 Resist patterns produced on different substrates using proximity X-ray lithography (PXL). (Courtesy of NTT-AT.)

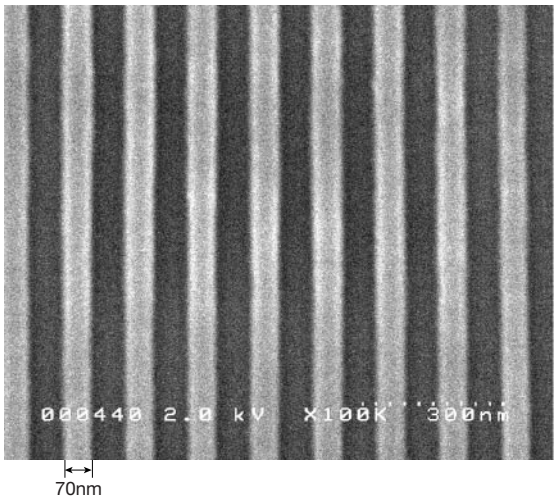

Figure 8 Seventy-nanometre line and space patterns delineated by an EUV microlithography system (NA = 0.15).

Other lithographies

Several other approaches have been proposed (and indeed demonstrated) for delineating patterns below 100 nm. These include nano-imprint lithography, near-field optical lithography, and direct patterning on a nanometre scale with scanning-probe microscopes. Although such approaches are useful for producing individual nano-structures for the investigation of nanometre-scale devices, the throughput is likely to always remain impracticably low for commercial application.

The 'little' picture

Optical lithography is a fundamental process in the manufacture of highly integrated microelectronic circuitry. But with the relentless commercial drive for ever smaller, faster and cheaper components, the existing technologies are rapidly being pushed to their limits. However, optical lithography has far from reached the end of the road, and will continue to be used for some years, adopting light sources of smaller wavelengths (such as ArF and F_2 excimer lasers) and optical techniques for further enhancing resolution. Indeed, despite many years of investigation (involving the investment of hundreds of millions of dollars) into alternative lithographic techniques, no obvious replacement for optical approaches has been developed.

But the microelectronics industry is not complacent, and possible next-generation lithographic technologies using non-optical sources are still being actively explored. Whether the future of lithography lies ultimately with X-rays, electron beams or extreme ultraviolet light is far from clear at present, as critical issues remain to be solved with all alternative approaches. And as enormous costs will be incurred in developing any one technology to a stage where it becomes commercially viable, global collaboration in the microelectronics industry will be key. □

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