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Correspondence and requests for materials should be addressed to I.M. (e-mail: mirebea@llb.saclay.cea.fr).

Epitaxial core–shell and core–multishell nanowire heterostructures

Lincoln J. Lauhon*†, Mark S. Gudiksen*†, Deli Wang* & Charles M. Lieber*‡

** Department of Chemistry and Chemical Biology; and ‡ Division of Engineering and Applied Sciences, Harvard University, Cambridge, Massachusetts 02138, USA*
† These authors contributed equally to this work

Semiconductor heterostructures with modulated composition and/or doping enable passivation of interfaces and the generation of devices with diverse functions[1]. In this regard, the control of interfaces in nanoscale building blocks with high surface area will be increasingly important in the assembly of electronic and photonic devices[2–10]. Core–shell heterostructures formed by the growth of crystalline overlayers on nanocrystals offer enhanced emission efficiency[7], important for various applications[8–10]. Axial heterostructures have also been formed by a one-dimensional modulation of nanowire composition[11–13] and doping[11]. However, modulation of the radial composition and doping in nanowire structures has received much less attention than planar[1] and nanocrystal[7] systems. Here we synthesize silicon and germanium core–shell and multishell nanowire heterostructures using a chemical vapour deposition method applicable to a variety of nanoscale materials[14]. Our investigations of the growth of boron-doped silicon shells on intrinsic silicon and silicon–silicon oxide core–shell nanowires indicate that homoepitaxy can be achieved at relatively low temperatures on clean silicon. We also demonstrate the possibility of heteroepitaxial growth of crystalline germanium–silicon and silicon–germanium core–shell structures, in which band-offsets drive hole injection into either germanium core or shell regions. Our synthesis of core–multishell structures, including a high-performance coaxially gated field-effect transistor, indicates the general potential of radial heterostructure growth for the development of nanowire-based devices.

Our approach to the synthesis of core–shell nanowire structures is based upon control of radial versus axial growth (Fig. 1). We have previously developed a general method for synthesis of semiconductor nanowires using nanocluster catalysts to direct axial growth by a vapour–liquid–solid growth process (Fig. 1a)[15,16]. Axial growth is achieved when reactant activation and addition occurs at the catalyst site and not on the nanowire surface (Fig. 1b). Correspondingly, it is possible to drive conformal shell growth by altering conditions to favour homogeneous vapour-phase deposition on the nanowire surface (Fig. 1c). Subsequent introduction of different reactants and/or dopants produces multiple shell structures of nearly arbitrary composition, although epitaxial growth of these shells requires consideration of lattice structures. This approach to core–shell nanowire heterostructures is elaborated below for the technologically important silicon (Si) and germanium (Ge) systems[17].

Homoepitaxial Si–Si core–shell nanowires were grown by chemical vapour deposition (CVD) using silane as the silicon reactant (Fig. 2)[18]. Intrinsic silicon (i-Si) nanowire cores were prepared by gold-nanocluster directed axial growth, which yields single-crystal structures with diameters controlled by the nanocluster diameter, and then boron-doped (p-type) silicon (p-Si) shells were grown by homogeneous CVD, where the shell thickness was directly proportional to the growth time. Radial shell growth can be 'turned-on' by the addition of diborane, which serves both to lower the decomposition temperature of silane[19] and acts as a p-type dopant. Transmission electron microscopy (TEM) images of the i-Si/p-Si product obtained from constant temperature growth shows a uniform core–shell structure consisting of a crystalline Si core and amorphous Si shell (Fig. 2a), where the core diameter, 19 nm, is consistent with the 20-nm nanocluster used in the initial axial growth step. TEM images show reproducible crystalline faceting at the core–shell interface (Fig. 2b). This faceting suggests that the nanowire surfaces are sufficiently clean following axial growth to nucleate epitaxial shell growth.

To understand and control Si on Si homoepitaxy in core–shell nanowire structures we carried out several distinct experiments. First, i-Si/p-Si core–shell nanowires prepared as above were annealed *in situ* at 600 °C. TEM images recorded on the annealed samples exhibited no diffraction contrast between the core and shell (Fig. 2c), and lattice-resolved images and electron diffraction data further show that the shell crystallizes to yield a single-crystal structure (Fig. 2d). Second, the importance of the initial nucleation for achieving epitaxy in the shell was probed using *in situ* oxidation of the silicon core (see Methods), which produces a thin amorphous silicon oxide layer at the surface of the core, before silicon-shell growth. Significantly, TEM images of i-Si/SiO_x/p-Si core–shell–shell structures show a smooth and abrupt interface between the crystalline core and amorphous shell (Fig. 2e, f). The low roughness of the interface is comparable to that observed in nanowires after only axial growth, and contrasts sharply with the faceted interface of the low-temperature homoepitaxy (Fig. 2b). These results show that the thin oxide layer completely disrupts homoepitaxy; further annealing and TEM studies show that oxidation inhibits crystallization of

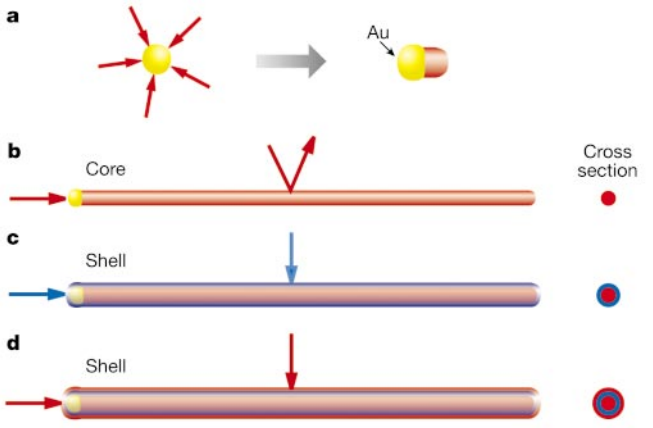

Figure 1 Synthesis of core–shell nanowires by chemical vapour deposition. **a**, Gaseous reactants (red) catalytically decompose on the surface of a gold nanocluster leading to nucleation and directed nanowire growth. **b**, One-dimensional growth is maintained as reactant decomposition on the gold catalyst is strongly preferred. **c**, Synthetic conditions are altered to induce homogeneous reactant decomposition on the nanowire surface, leading to a thin, uniform shell (blue). **d**, Multiple shells are grown by repeated modulation of reactants.

the shell under annealing conditions that lead to complete crystallization in samples without the oxide layer.

We have used three-terminal measurements to characterize the electrical transport properties of the three distinct types of i-Si/p-Si core–shell structures, thereby defining the impact of the observed structural differences (Fig. 2g). First, the i-Si/SiO_x/p-Si nanowires (Fig. 2f), which have an amorphous p-Si shell, show relatively high resistivities, about $10^3\,\Omega\,cm$, and low hole mobilities, about $0.001\,cm^2\,V^{-1}\,s^{-1}$. These resistivity and mobility values are comparable to those of heavily doped amorphous silicon deposited by plasma-enhanced CVD[20], and suggest that conduction is dominated by the amorphous p-Si shell. In contrast, the i-Si/p-Si structures, which have partly or fully crystalline p-Si shells, exhibit much lower resistivities, about $(0.5–5) \times 10^{-3}\,\Omega\,cm$. The similarity in these values is consistent with our observation of crystalline faceting (Fig. 2b), and suggests that a continuous epitaxial layer of p-Si, which dominates transport, exists prior to complete crystallization by annealing. In addition, the hole mobility of the crystalline p-Si shell nanowires, $25\,cm^2\,V^{-1}\,s^{-1}$, is comparable to that of single-crystal silicon at similar high doping levels (see Supplementary Materials)[21].

Radial heteroepitaxy of Si on Ge was pursued to explore the potential of our approach to core–shell structures in materials of rapidly increasing scientific and technological importance[17]. For example, the energy band offsets in Si–Ge heterostructures produce internal fields that drive charge-carrier redistribution[22], which can enable high-mobility devices. Single-crystal Ge nanowires were defined through gold nanocluster directed axial growth, and then boron-doped p-Si shells were grown by homogeneous CVD (see Methods). Bright-field TEM images (Fig. 3a) reveal a core–shell structure that is consistent with Ge-core (dark) and Si-shell (light) structure, and we confirmed this assignment by elemental mapping (Fig. 3b, c), which shows a localized Ge core and Si shell. High-resolution TEM images of i-Ge/p-Si core–shell nanowires in which the p-Si shell was deposited at low temperature without annealing show a crystalline Ge core and predominantly amorphous Si shell (Fig. 3d). Analysis of cross-sectional elemental mapping data (Fig. 3e) shows that the Ge core is about 26 nm, the Si shell is about 15 nm, and the Ge–Si interface width is believed to be <1 nm on the basis of the electron beam width and modelling (see Methods).

Significantly, we find that the amorphous Si shell can be completely crystallized following *in situ* thermal annealing at 600 °C. Lattice-resolved TEM images of Ge–Si core–shell structures following this thermal treatment exhibit a uniform crystalline Si shell (Fig. 3f), and suggest that thin regions of epitaxially grown Si are present in the unannealed wires. Higher silicon-deposition temperatures might make the annealing step unnecessary by improving the surface mobility of adsorbed silicon. Elemental mapping (Fig. 3g) confirms that the contrast in high-resolution TEM images is consistent with an abrupt (<1 nm) Si–Ge interface. Although the present measurements cannot rule out some interface mixing, previous studies of planar growth under similar conditions found no evidence for Si–Ge interdiffusion[23]. Notably, preliminary elec-

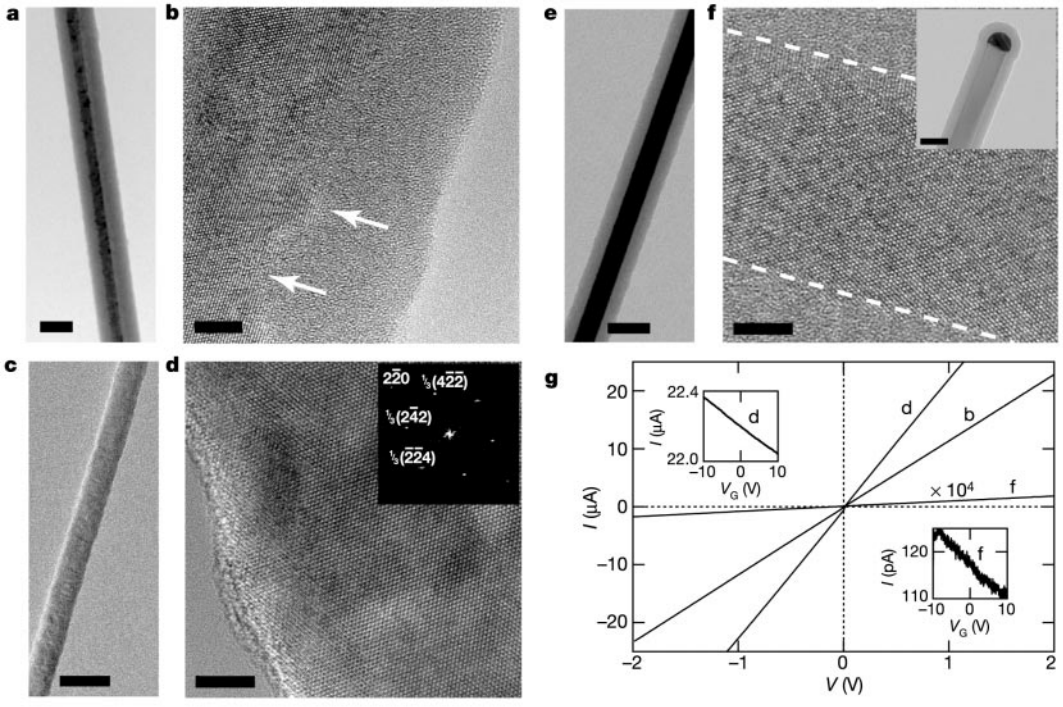

Figure 2 Si–Si homoepitaxial core–shell nanowires. **a**, **b**, Diffraction contrast and high-resolution TEM images, respectively, of an unannealed intrinsic silicon core and p-type silicon shell nanowire grown at 450 °C. Crystal facets in the high-resolution TEM image designated by arrows indicate initially epitaxial shell growth at low temperature. Scale bars are 50 nm and 5 nm, respectively. **c**, **d**, TEM images (analogous to **a** and **b**) of an i-Si/p-Si core–shell nanowire annealed at 600 °C for 30 min after core–shell growth at 450 °C. Inset, two-dimensional Fourier transforms of the image depicting the [111] zone axis of the single crystal nanowire. The $\frac{1}{3}\{422\}$ reflections, although forbidden in bulk silicon, arise as a result of the finite thickness of the nanowire[27]. **e**, **f**, TEM images of an i-Si/SiO_x/p-Si nanowire. The oxide layer is too thin (<1 nm) to discern in the high-resolution image, but the sharp interface (dashed line) between the crystalline core and amorphous overcoat clearly differs from the faceting seen in **b** and illustrates the disruption of epitaxy. Inset, TEM image of p-Si coating the nanowire and the Au nanocluster tip. Scale bar is 50 nm. **g**, Three-terminal current (I) versus voltage (V) measurements of the nanowires described in the preceding panels. A schematic of the measurement set-up is provided in the Supplementary Information. Curves b, d and f are labelled according to the representative TEM image (**b**, **d** and **f**) from the same sample of wires. Curve f has been multiplied by a factor of 10^4. Insets, current versus backgate voltage to determine field-effect mobilities (see Supplementary Information).

trical transport studies of the i-Ge/p-Si core–shell nanowires provide good evidence for internal field-driven carrier redistribution (see Supplementary Information), and we believe these systems are worth investigating further.

Synthetic control of Si–Ge core–multishell nanowire structures could be used to explore a variety of fundamental phenomena and new device concepts, although achieving this goal will require the ability to prepare an essentially arbitrary sequence of Si, Ge and alloy overlayers on both Si and Ge nanowire cores. To this end, we studied Ge deposition on Si nanowire cores. TEM images and composition mapping (Fig. 4a) show the Si–Ge core–shell structure with a sharp (<1 nm) interface, and demonstrate that the Ge shell is fully crystallized for low-temperature growth (Fig. 4b), presumably owing to the higher surface mobility of Ge adatoms. In addition, diffraction data are consistent with coherently strained epitaxial overgrowth (inset Fig. 4b); that is, a single diffraction peak is observed along the axial direction, which indicates compressively strained Ge and tensile-strained Si. Two peaks, which can be indexed to the Ge (5.657 Å) and Si (5.431 Å) lattice constants, are also observed in the radial direction and indicate relaxation normal to the interface. Preliminary transport studies of these structures (Supplementary Information) provide evidence for hole injection from the p-Si core to i-Ge shell as expected from valence band offsets[22]. Finally, we have also explored the growth of more complex multishell structures; composition mapping of a Si–Ge–Si core–double-shell structure (Fig. 4c) demonstrates the potential of extending our approach in this direction.

Lastly, we have used our approach to prepare new device structures, such as a coaxially gated nanowire field-effect transistor (FET) (Fig. 5). The coaxial geometry offers advantages for nano-FETs, such as a capacitance enhancement compared to standard planar gates used in nanowire[3] and nanotube[24] FETs, and might be best compared to double-gated structures being investigated for advanced planar devices[25]. The nanowire building blocks used to fabricate coaxial FETs consisted of a core–multishell structure: p-Si/i-Ge/SiO_x/p-Ge, where the active channel is the i-Ge shell. The source, drain and gate contacts were made by selective etching and metal deposition onto the inner i-Ge shell and outer p-Ge shell, respectively. Significantly, transport measurements made on these initial devices show very good performance characteristics (Fig. 5c) with transconductance values up to 1,500 nAV^{-1} for a 1-V source–drain bias. These data for unoptimized devices are comparable to recent results reported for intensively studied carbon-nanotube FETs. We are encouraged by this comparison because the values for the coaxial nanowire FET thus probably represent a lower limit to what may be achieved. For example, minimizing SiO_x trap states, which can compensate the applied gate voltage, reducing the gate dielectric thickness, and/or substituting high-K dielectrics should lead to improvements in transistor performance. We believe it is significant that all of these changes can be implemented during the initial synthesis stage, and thus integration of this advanced device structure is essentially no more difficult than for a single-component semiconducting nanowire or nanotube.

Thus we have shown that heterostructures in which composition and/or doping are modulated at the nanometre scale can be realized in core–shell nanowires. Much of our initial efforts have focused on demonstration of structural diversity in core–shell nanomaterials, and the promise of these new structures has already been demonstrated with the realization of a coaxial FET device. Future advances in nanowire semiconductor devices could be realized by increasing carrier mobilities. We believe that substantial increases could be achieved in modulation-doped core–shell structures in which, for example, a layer of i-Si separates the i-Ge core from a high-density dopant layer. Formation of a radial two-dimensional electron or

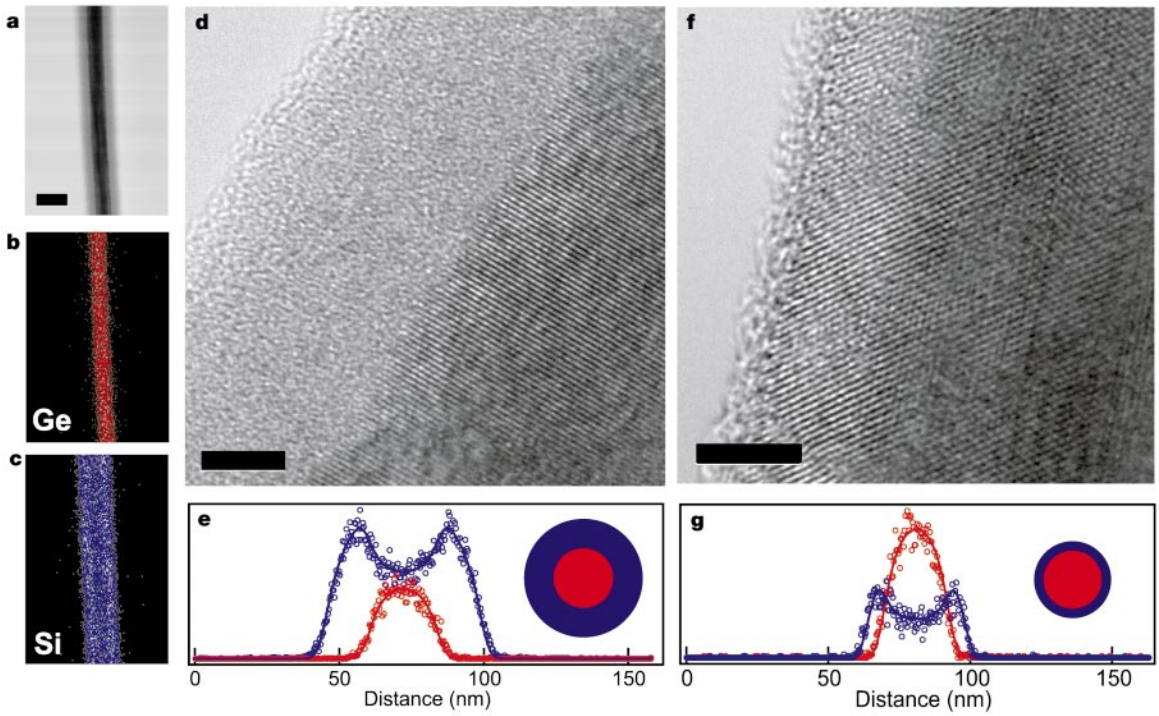

Figure 3 Ge–Si core–shell nanowires **a**, Bright-field image of an unannealed Ge–Si core–shell nanowire with an amorphous p-Si shell. Scale bar is 50 nm. **b**, **c**, Scanning TEM elemental maps of Ge (red) and Si (blue) concentrations, respectively, in the nanowire of **a**. **d**, High-resolution TEM image of a representative nanowire from the same synthesis as the wire in **a**–**c**. Scale bar is 5 nm. **e**, Elemental mapping cross-section showing the Ge (red circles) and Si (blue circles) concentrations. The solid lines show the theoretical cross-section for a 26-nm-diameter core, 15-nm-thick shell and <1 nm interface according to the model described in the Methods section. **f**, High-resolution TEM image of annealed Ge–Si core–shell nanowire exhibiting a crystalline p-Si shell. Scale bar is 5 nm. **g**, Elemental mapping cross-section gives a 5-nm shell thickness with a sharp interface consistent with the TEM image, suggesting that the Ge and Si do not interdiffuse substantially during the annealing process.

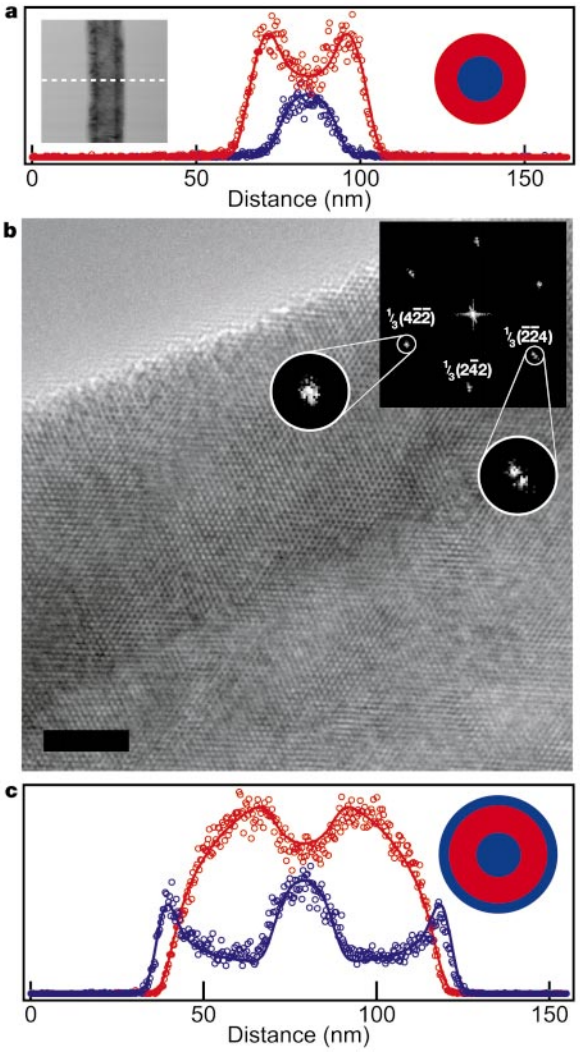

Figure 4 Si–Ge and Si–Ge–Si core–shell nanowires. **a**, Elemental mapping cross-section indicating a 21-nm-diameter Si core (blue circles), 10-nm Ge shell (red circles) and <1 nm interface. Inset, TEM image of the corresponding Si–Ge core–shell nanowire. The white dashed line indicates mapping cross-section. **b**, High-resolution TEM image of a representative crystalline nanowire core and shell from the same synthesis as the wire in **a**. Scale bar is 5 nm. Inset, two-dimensional Fourier transform of the real-space image showing the [111] zone axis. The split lattice reflections perpendicular to the interface can be indexed to the Ge and Si lattice constants (5.657 Å and 5.431 Å, respectively). **c**, Cross-sectional elemental mapping of a double-shell structure with an intrinsic silicon core (diameter, 20 nm), intrinsic germanium inner shell (thickness, 30 nm), and p-type silicon outer shell (4 nm); silicon is blue circles and germanium is red circles.

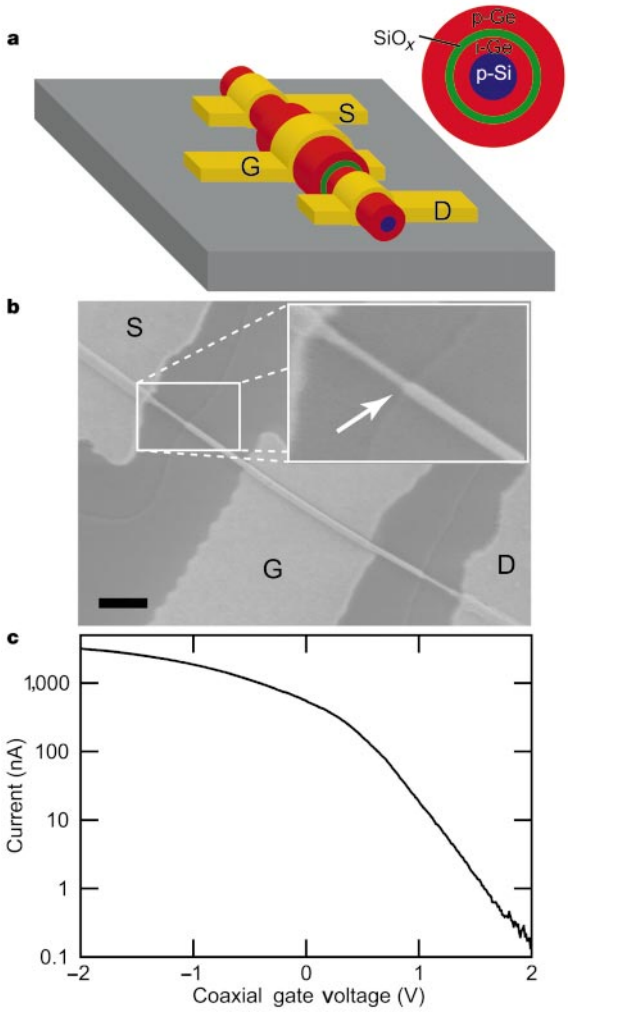

Figure 5 Coaxially-gated nanowire transistors. **a**, Device schematic showing transistor structure. The inset shows the cross-section of the as-grown nanowire, starting with a p-doped Si core (blue, 10 nm) with subsequent layers of i-Ge (red, 10 nm), SiO_x (green, 4 nm), and p-Ge (5 nm). The source (S) and drain (D) electrodes are contacted to the inner i-Ge core, while the gate electrode (G) is in contact with the outer p-Ge shell and electrically isolated from the core by the SiO_x layer. **b**, Scanning electron micrograph (SEM) of a coaxial transistor. Source and drain electrodes were deposited after etching the Ge (30% H_2O_2, 20 s) and SiO_x layers (buffered HF, 10 s) to expose the core layers. The etching of these outer layers is shown clearly in the inset and is indicated by the arrow. The gate electrodes were defined in a second step without any etching before contact deposition. Scale bar is 500 nm. **c**, Gate response of the coaxial transistor at $V_{SD} = 1$ V, showing a maximum transconductance of 1,500 nA V^{-1}. Charge transfer from the p-Si core to the i-Ge shell produces a highly conductive and gateable channel.

hole gas of very high mobility would significantly improve the performance of existing nanowire-based devices and open up substantial new opportunities to study electron–electron interactions in this low-dimensional system. More generally, our CVD-based epitaxial shell-growth method implies that for any active core or shell region, be it metallic, semiconducting or insulating, the surrounding material can be chosen to provide chemical passivation, charge carrier confinement, or wave-guiding capability analogous to graded-index optical fibres. When combined with the ability to produce axial nanowire heterostructures[11], the techniques described herein provide unprecedented control of nanometre-scale composition in two independent dimensions and represent a significant advance in the complexity and functionality of building blocks for nanoscience and nanotechnology. □

Methods

Gold nanoclusters were deposited on oxidized silicon wafers and placed in a quartz tube furnace. Silicon nanowire cores were grown at 450 °C using silane (5 cm^3 at standard temperature and pressure, STP min^{-1}) at 5 torr, producing a one-dimensional (axial) growth rate of about 2 μm min^{-1}. p-type silicon shells were deposited using silane (1 cm^3 STP min^{-1}) and 100 p.p.m. diborane in helium (20 cm^3 STP min^{-1}) at 20 torr yielding a radial growth rate of about 10 nm min^{-1}, stoichiometric incorporation of boron would yield a bulk doping level of 2×10^{20} cm^{-3}, and is similar to the values obtained from transport measurements (see Supplementary Information). Ge nanowires were grown at 380 °C using 10% germane in argon (30 cm^3 STP min^{-1}) at 30 torr (axial growth rate, ~0.7 μm min^{-1}), while Ge shells were deposited at 5 cm^3 STP min^{-1} and 4 torr (radial growth rate, ~10 nm min^{-1}) by changing the position of the growth substrate within the furnace. The amount of reactant that has thermally decomposed typically increases as the gas flows through the furnace, and thus radial growth may be 'turned on' by moving the growth substrate downstream to favour uncatalysed surface growth. Oxidation of i-Si cores to interrupt epitaxy was accomplished by flowing oxygen (30 cm^3 STP min^{-1}) at 30 torr for 2 min. The oxide gate dielectric in the coaxially gated structures was grown at 450 °C using oxygen (2.5 cm^3 STP min^{-1}) and silane (0.25 cm^3 STP min^{-1}) at 1 torr for 2 min.

The substrate-bound nanowires were sonicated in ethanol and deposited on oxidized degenerately doped silicon wafers or copper grids for electrical transport and TEM measurements, respectively. Electron-beam lithography was employed to define contact regions with subsequent deposition of Ti/Au electrodes, as described previously[3]. Effective mobilities were calculated according to the method of ref. 26. Additional details are provided in the Supplementary Information. The integrity of the SiO_x gate dielectric in the coaxially gated nanowire transistors was confirmed by the low, <5 pA, gate to source–drain leakage currents. The continuity of the p-Ge outer shell was verified by two-terminal resistance measurements on the shell itself.

The high-resolution TEM images were collected on a Jeol 2010F microscope, and elemental imaging and cross-sectional mapping was conducted on a VG HB603 STEM. The elemental mapping data were modelled by calculating the cross-sectional thicknesses for concentric cylinders of different composition with abrupt interfaces, taking the electron beam profile into account by convoluting with a gaussian profile of 1.6 ± 0.5 nm full-width, consistent with the known value for the instrument.

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Correspondence and requests for materials should be addressed to C.M.L. (e-mail: cml@cmliris.harvard.edu).

The amount of carbon released from peat and forest fires in Indonesia during 1997

Susan E. Page*, Florian Siegert†‡, John O. Rieley§, Hans-Dieter V. Boehm‡, Adi Jaya‖ & Suwido Limin‖

** Department of Geography, University of Leicester, Leicester LE1 7RH, UK*
† Ludwigs-Maximilians-Universität München, Biology Department II, Luisenstrasse 14, D-80333 München, Germany, and Remote Sensing Solutions GmbH, Woerthstrasse 49, D-81667 München, Germany
‡ Kalteng Consultants, Kirchstockacher Weg, 81663 München, Germany
§ School of Geography, University of Nottingham, Nottingham NG7 2RD, UK
‖ Centre for International Co-operation in Management of Tropical Peatland, Faculty of Agriculture, University of Palangka Raya, Palangka Raya 73112, Indonesia

Tropical peatlands are one of the largest near-surface reserves of terrestrial organic carbon, and hence their stability has important implications for climate change[1–3]. In their natural state, lowland tropical peatlands support a luxuriant growth of peat swamp forest overlying peat deposits up to 20 metres thick[4,5]. Persistent environmental change—in particular, drainage and forest clearing—threatens their stability[2], and makes them susceptible to fire[6]. This was demonstrated by the occurrence of widespread fires throughout the forested peatlands of Indonesia[7–10] during the 1997 El Niño event. Here, using satellite images of a 2.5 million hectare study area in Central Kalimantan, Borneo, from before and after the 1997 fires, we calculate that 32% (0.79 Mha) of the area had burned, of which peatland accounted for 91.5% (0.73 Mha). Using ground measurements of the burn depth of peat, we estimate that 0.19–0.23 gigatonnes (Gt) of carbon were released to the atmosphere through peat combustion, with a further 0.05 Gt released from burning of the overlying vegetation. Extrapolating these estimates to Indonesia as a whole, we estimate that between 0.81 and 2.57 Gt of carbon were released to the atmosphere in 1997 as a result of burning peat and vegetation in Indonesia. This is equivalent to 13–40% of the mean annual global carbon emissions from fossil fuels, and contributed greatly to the largest annual increase in atmospheric CO_2 concentration detected since records began in 1957 (ref. 1).

In Indonesia, peatland fires are mostly anthropogenic, started by local (indigenous) and immigrant farmers as part of small-scale land clearance activities, and also, on a much larger scale, by private companies and government agencies as the principal tool for clearing forest, before establishing crops[9,11,12]. During the abnormally long, El Niño dry season of 1997, many of these 'managed' fires spread out of control, consuming not only the surface vegetation but also the underlying peat and tree roots, contributing to the dense haze that blanketed a large part of Southeast Asia and causing both severe deterioration in air quality and health problems[9,11].

In order to investigate the role of peatland in the release of carbon during the 1997 fires in Indonesia, we focused on 2.5 million hectares of landscape in Central Kalimantan within a single Landsat TM (thematic mapper) image. We determined land cover types and the total area of peatland. The latter includes natural and semi-natural vegetation (peat swamp forest, PSF) and land converted to various other types of use (such as the ill-fated Mega Rice Project (MRP) that was promoted by the Indonesian government from 1995 to 1999 (Fig. 1a)). By combining peat thickness, pre-fire land cover and burnt area data we were able to estimate the amount of carbon released from peatland during the fires. Our objectives were to: (1) provide accurate information on the location and extent of