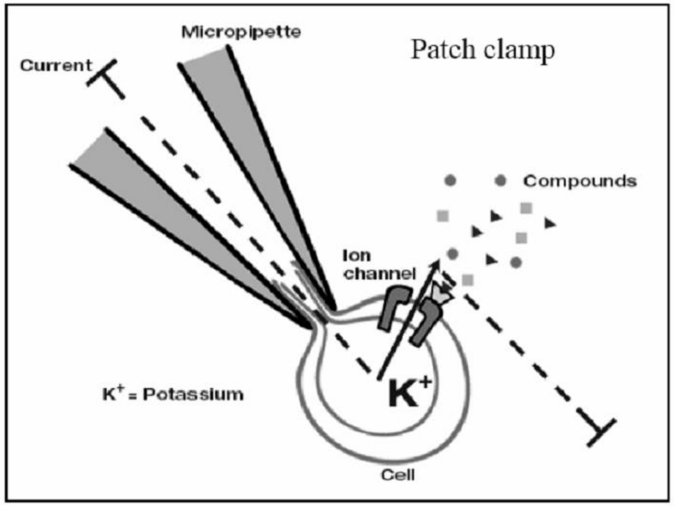
Patch Clamp Chip

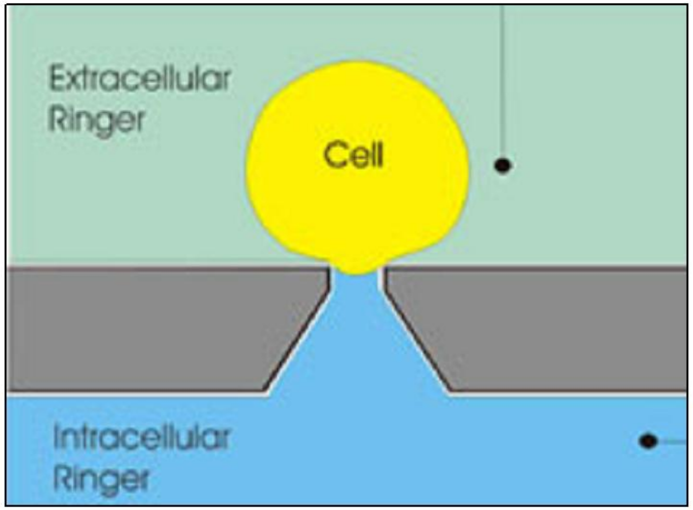
Patch clamp chip 이란?

Patch clamping

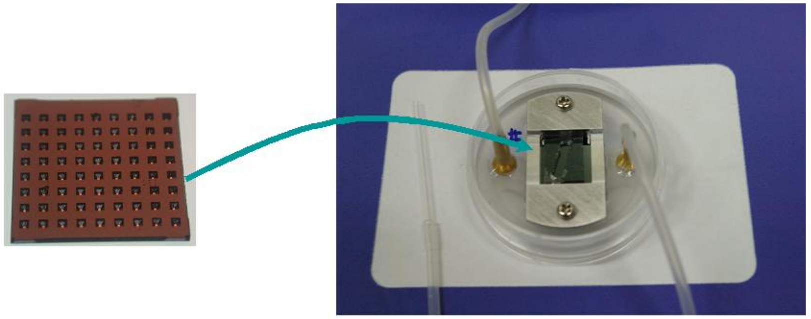
Pipette Method



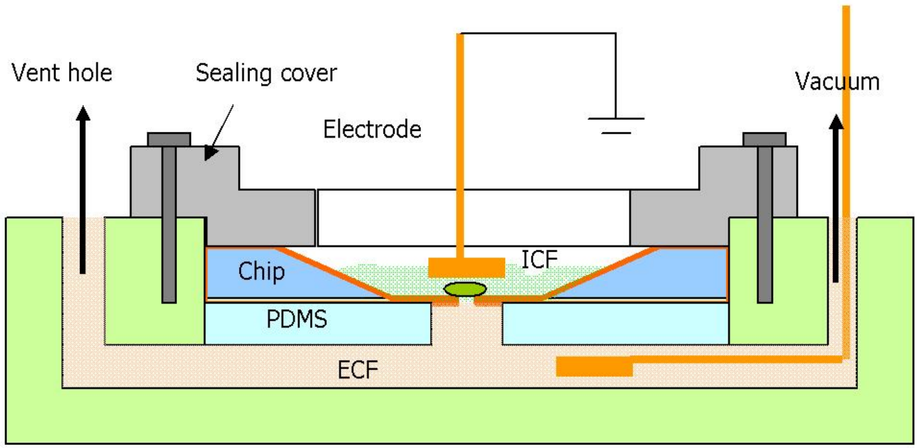
On-chip Patch clamp

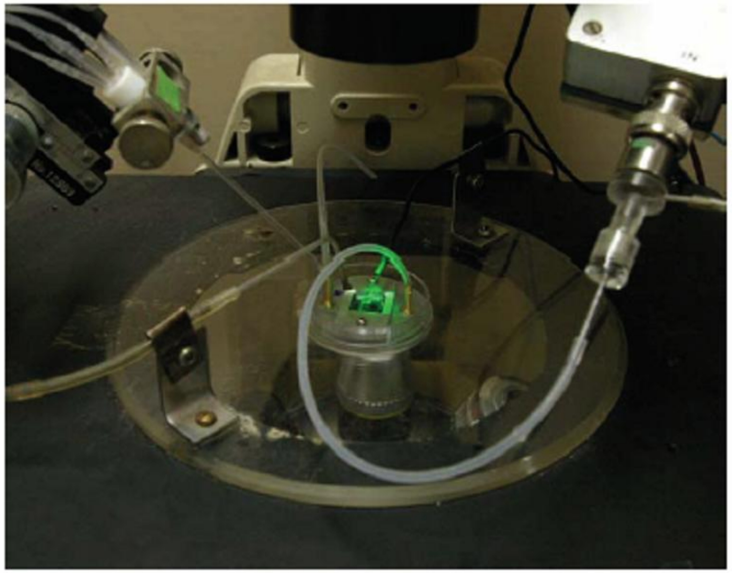


Experiment Setup



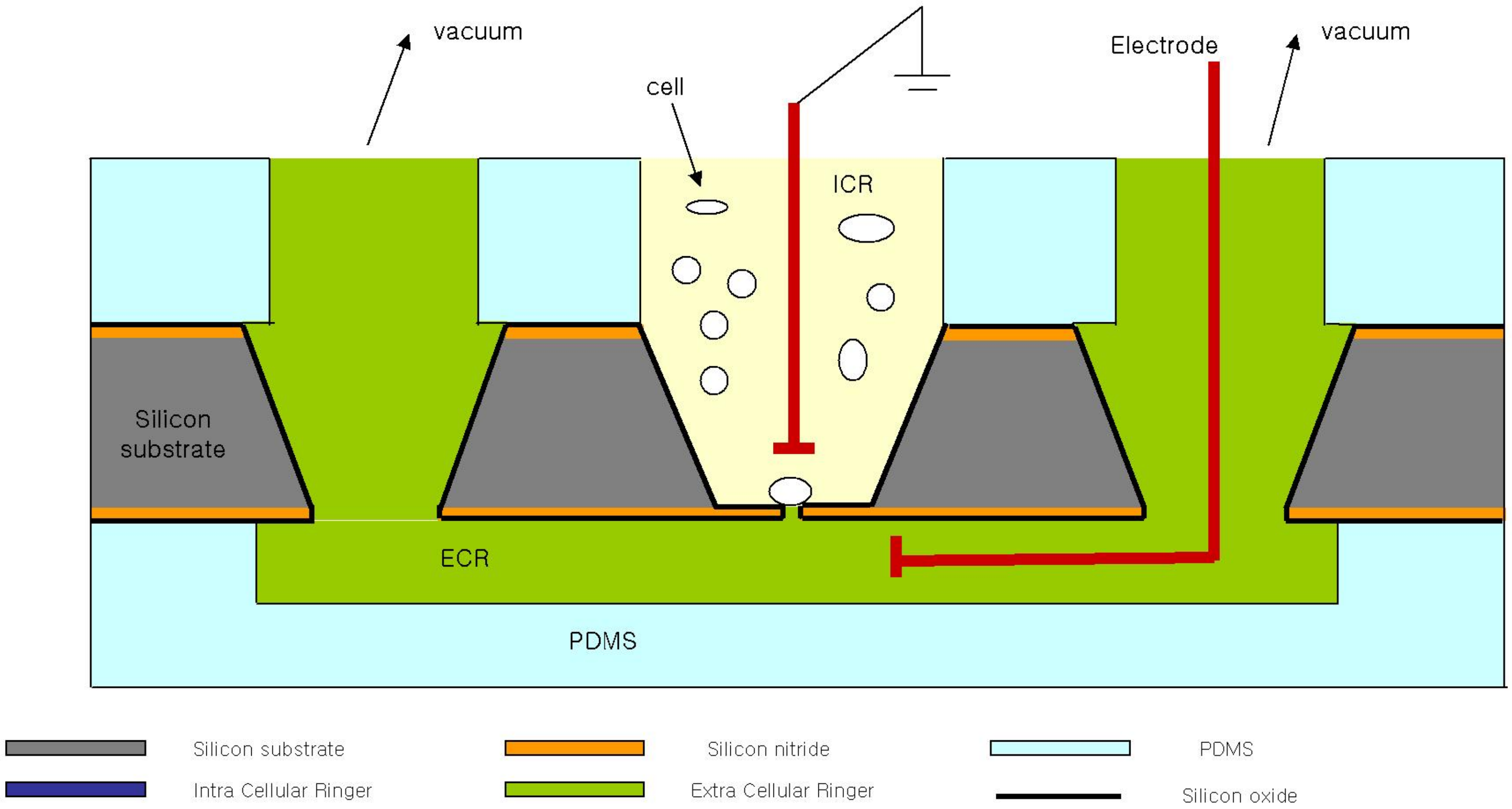
Jig for vacuum suction





Setup with Patch clamping system

Design new Device



Fabrication

Bulk Micromachining

- The purpose of bulk micromachining
  - Selectively remove significant amounts of silicon from a substrate
  - Broadly applied in the fabrication of micromachined sensors, actuators, and structures

- Fabrication method: dry/wet etching
  - Undercut structures that are required to physically move
  - Form membranes on one side of a wafer
  - Make a variety of trenches, holes, or other structures

Bulk Micromachining

- Isotropic wet etching
- <u>Anisotropic wet etching</u>
- Xenon Difluoride Etching (XeF2)

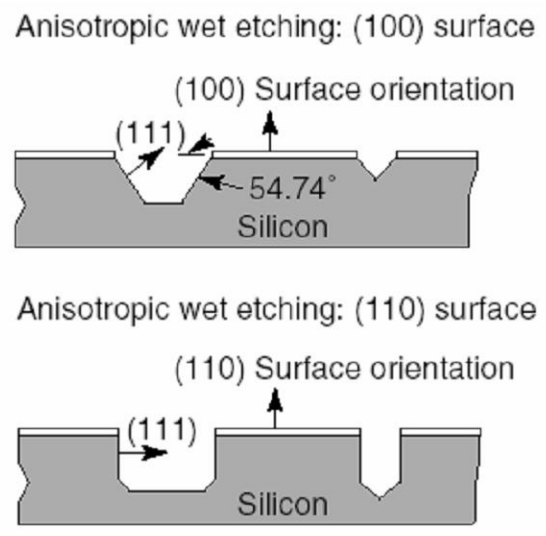
  –Isotropic dry etching
- <u>Plasma/Reactive Ion Etching (RIE)</u>

  –Anisotropic dry etching
- <u>Deep Reactive Ion Etching (Deep RIE)</u>

Bulk Micromachining Methods (1)

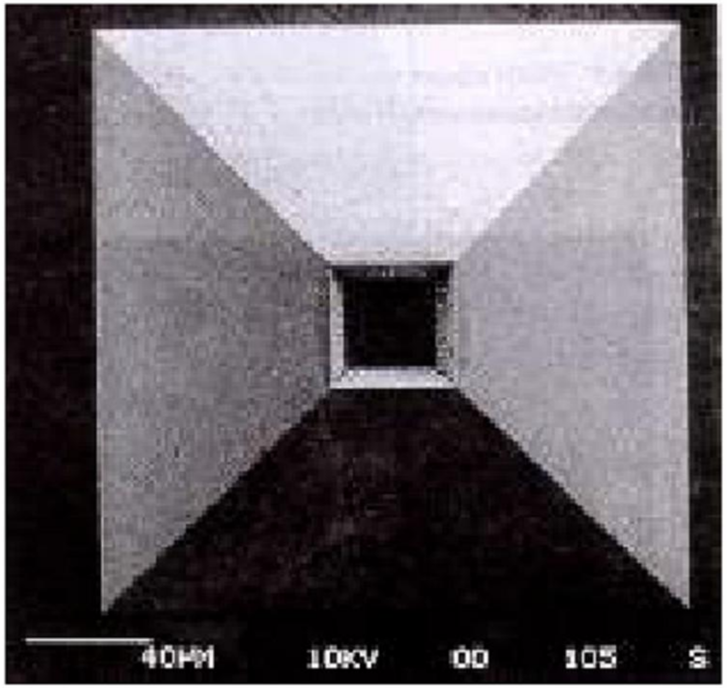
- Anisotropic wet etching

- Anisotropic etchants etch much faster in on direction than in another
  → exposing the slowest etching crystal planes over time
  → (111) planes have the slowest etch rate

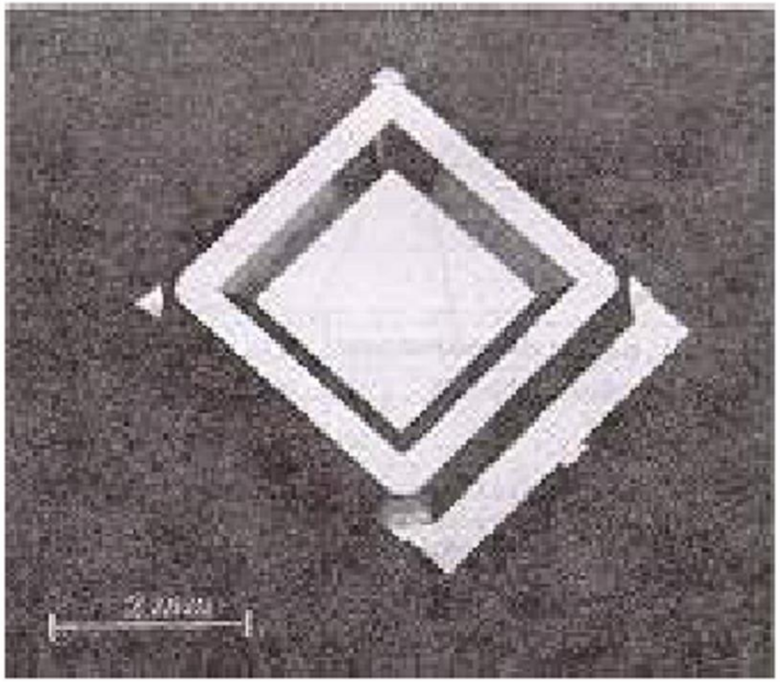


- Several solutions:
  - Alkalic OH (KOH, NaOH)
  - Tetramethylammonium hydroxide (THAH, $(CH_3)_4NOH$)
  - Ethylenediamine pyrocatechol (EDP, $NH_2(CH_2)_2NH_2+C_6H_4(OH)_2$)
- Etching at concave corners on (100), stop at (111) intersections. Convex corners are under cut

(100) Si Wet Etch



Nozzle

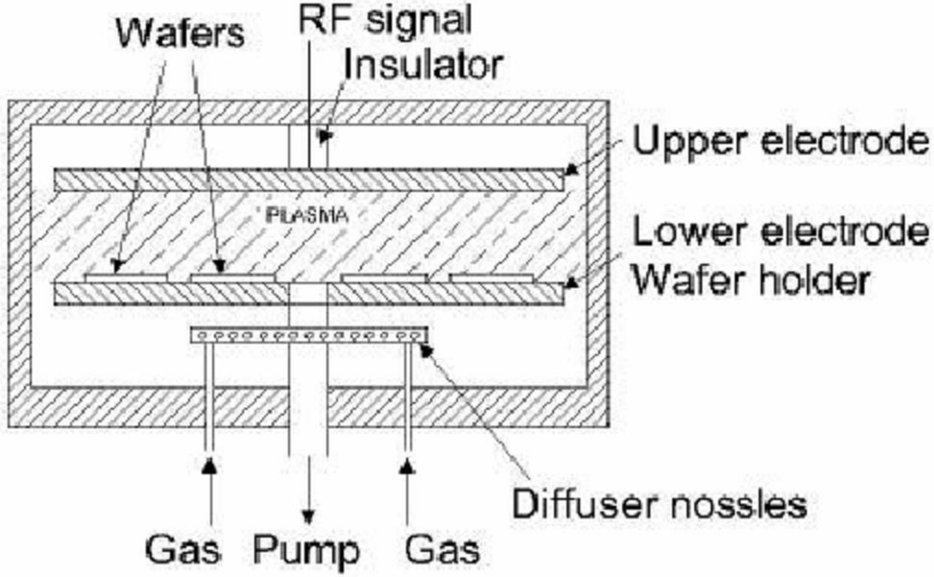


Diaphragm

Bulk Micromachining Methods (2) – Anisotropic Dry Etching

- Plasma/Reactive Ion Etching (RIE)

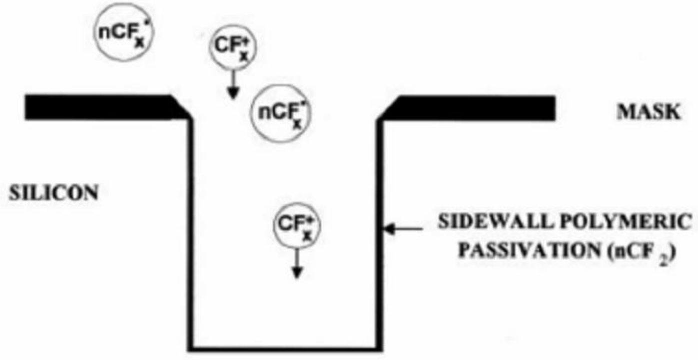
- anisotropic dry etch process
- Process in which chemical etching is accompanied by ion bombardment
- Combination of physical and chemical etching



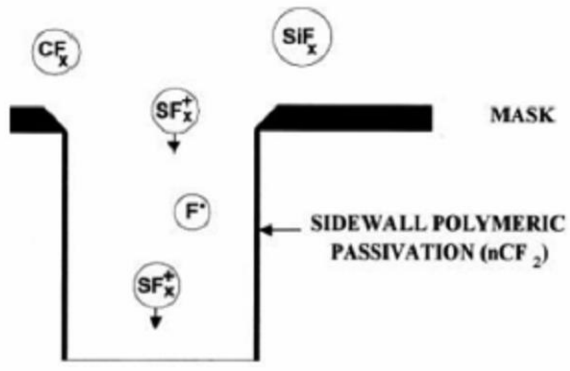
Typical parallel-plate reactive ion etching system

Bulk Micromachining Methods (3)

- Deep Reactive Ion Etching (Deep RIE)
  - Uses high density plasma to alternatively etch silicon and deposit etch resistant polymer on sidewall
    - Unconstrained geometry 90^{O} side walls
    - High aspect ratio 1:30
    - Easily masked (PR, SiO_2)
  - Bosch process: sidewall passivaiton → etch → sidewall passivaiton → etch …



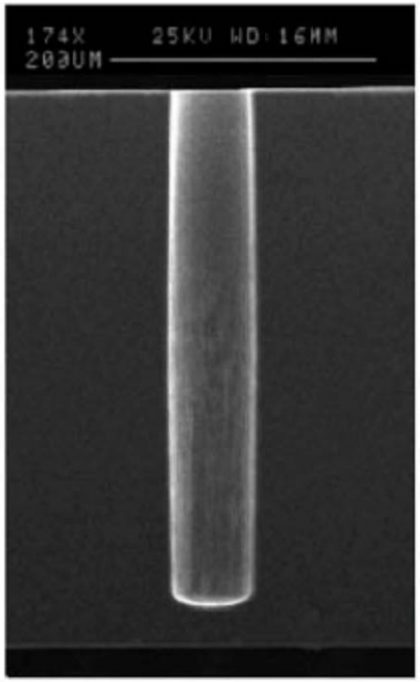
ASE process deposition step



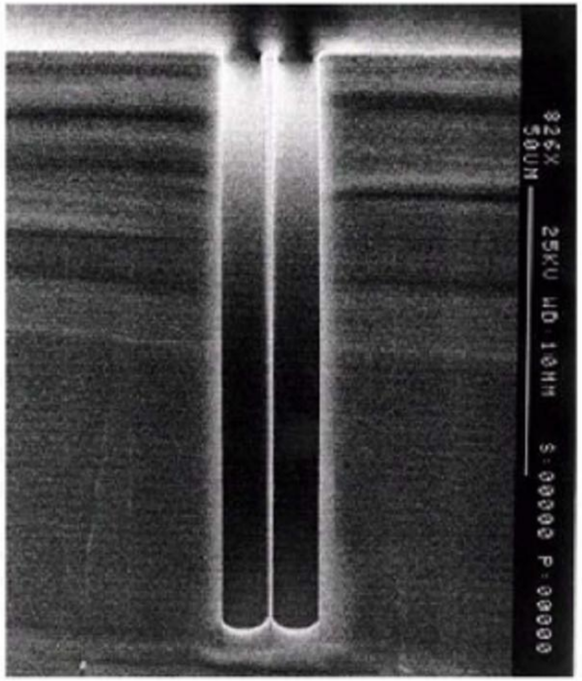
ASE process etch step

Deep RIE Fabrication example (1)

- Fabrication example (deep trench)



350㎛-depth

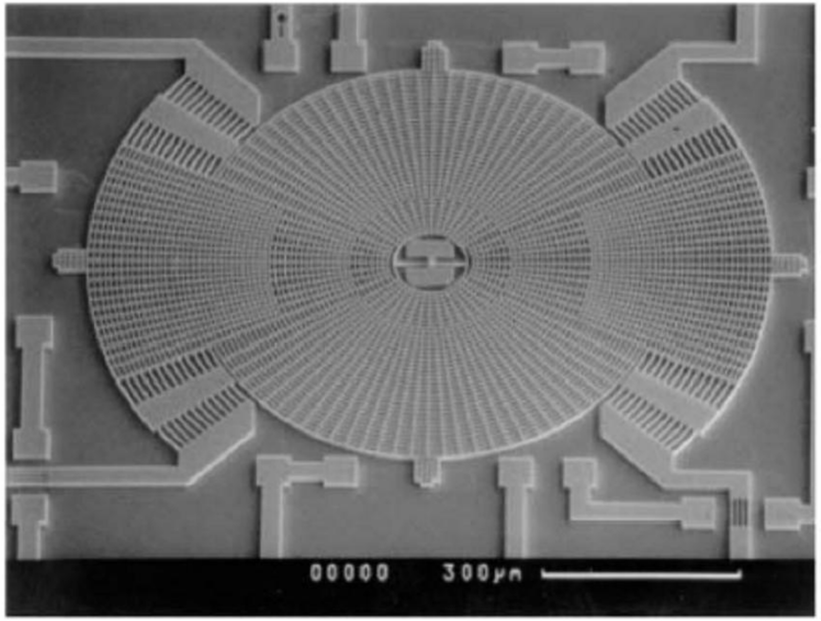


100㎛-depth

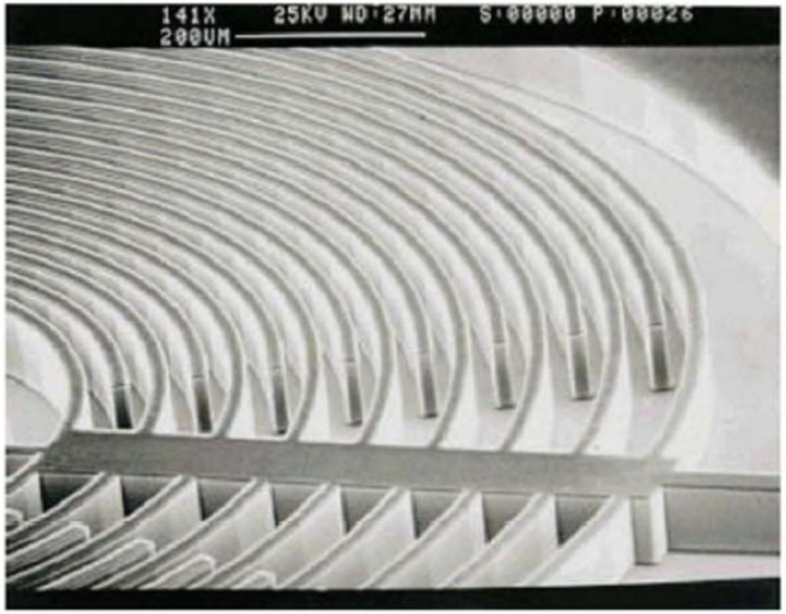
80㎛-depth, 4.5㎛ space width, 2㎛ line width

Deep RIE Fabrication example (2)

- Fabrication example (IMU device)



Gyroscope



Accelerometer (170㎛-depth)

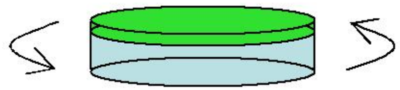
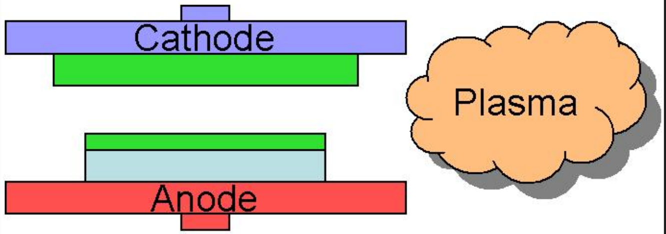
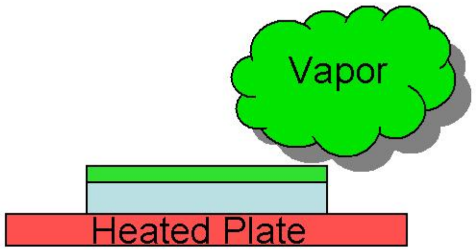
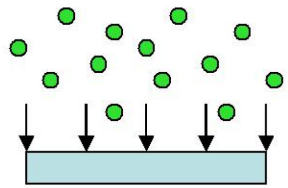
Surface Micromachining

- What is surface micromachining ?
  - Surface micromachining is characterized by the fabrication of micromechanical structures from deposited thin films
  - Originally employed for integrated circuits
  - Used films: low-pressure chemical-vapor-deposition polycrystalline silicon, silicon nitride, silicon dioxide
- In the surface micromachining
  - Dry etching defines the surface features in the x, y plane, and wet etching released them from the plane by under cutting
  - Shapes in x, y plane are unrestricted by the crystallography of the substrate

Thin Film Deposition (1)

- Deposition
  - The transformation of vapors into solids, frequently used to grow solid thin film and powder materials
- Physical Vapor Deposition (PVD)
  - Direct impingement of particles on the hot substrate surface
  - Electron-beam Evaporation, Sputtering
- Chemical Vapor Deposition (CVD)
  - Convective heat and mass transfer as well as diffusion with chemical reactions at the substrate surfaces
  - More complex process than PVD
  - More effective in terms of the rate of growth and the quality of deposition
  - LP/AP CVD, Thermal/PE/Ph/LC CVD

Thin Film Deposition (2)

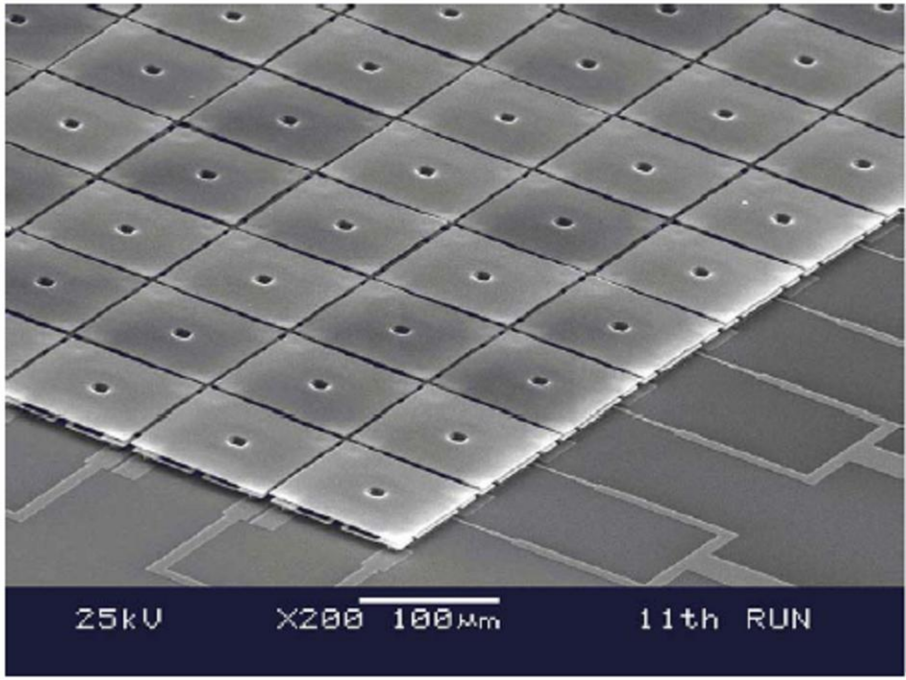
Type	Materials	Physics
Spin-on	Organic	
Sputtering	Metals	
Chemical Vapor Deposition	Silicon Compounds	
Doping	Conductors	

Considerations

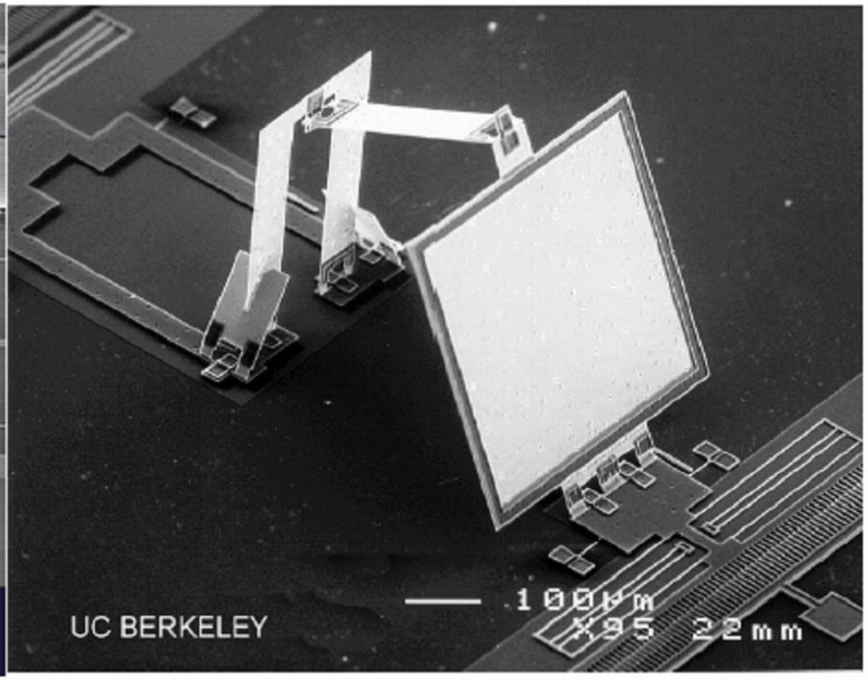
- Thickness
- Time
- Uniformity
- Cost
- Damage
- Contamination
- Adhesion
- Material Choice

Surface micromachined devices

- Optical system



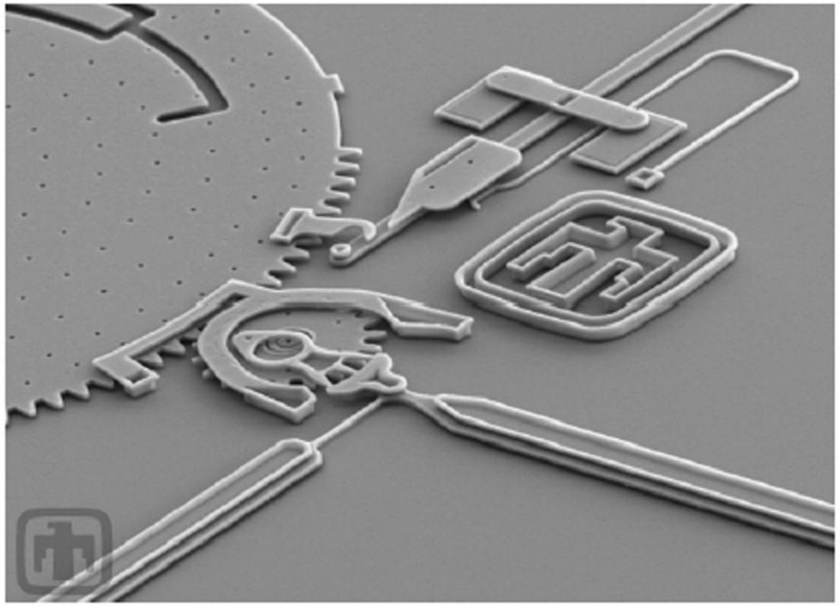
Surface micromachined micromirror
(MiSA SNU)



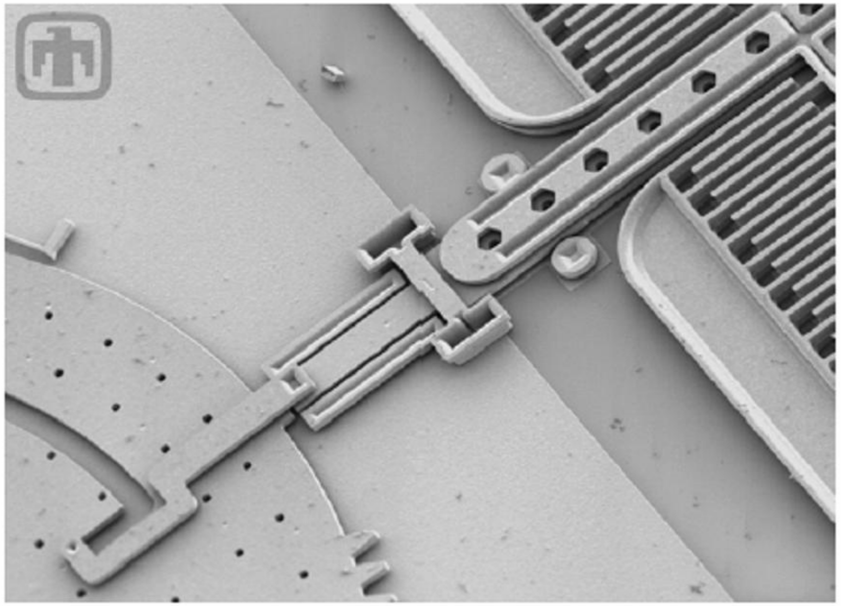
Actuated micromirror
for external cavity semiconductor lasers
(UC Berkeley)

Surface micromachined devices

- Microlock system



Microlock latch mechanism

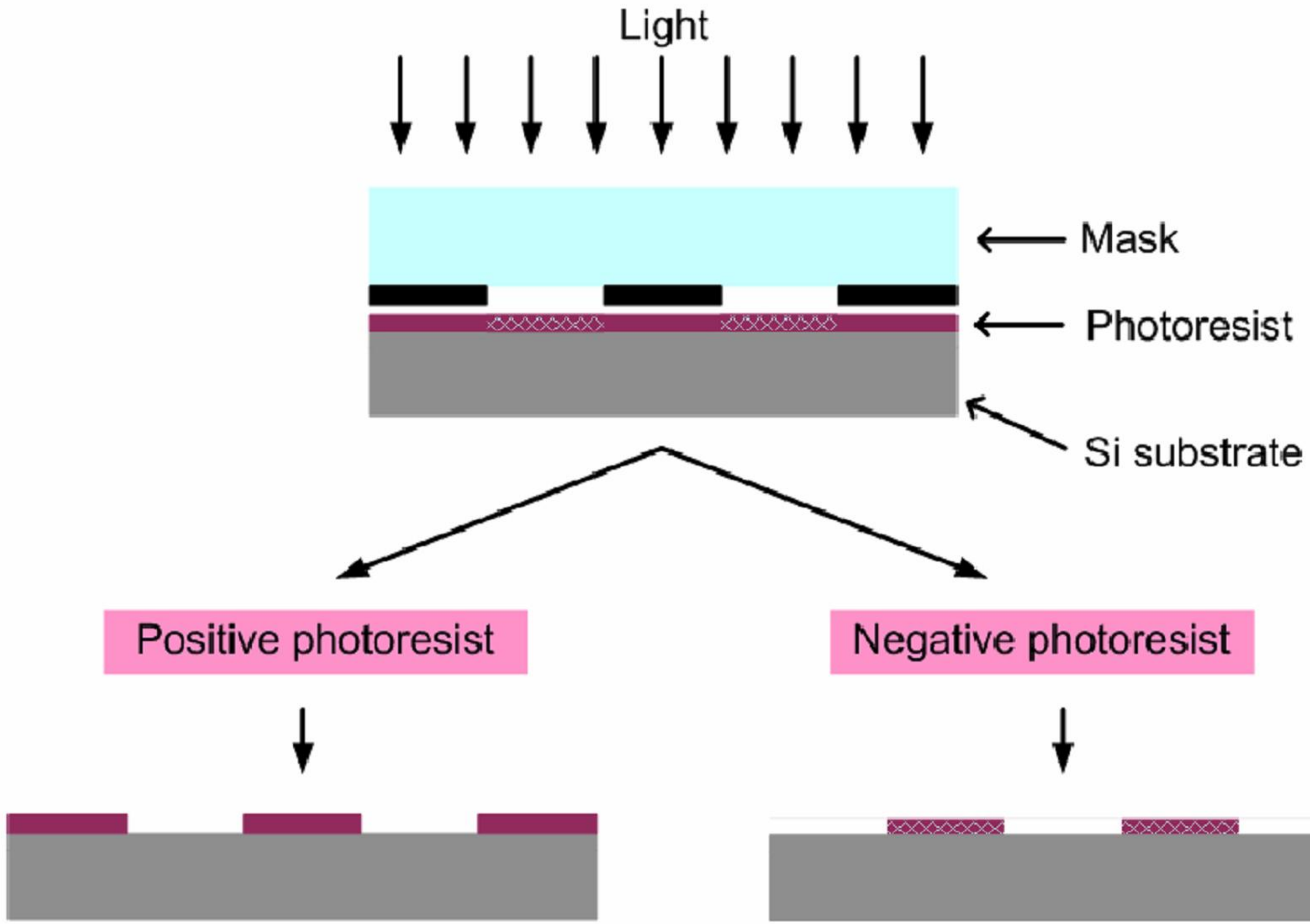


Micromechanical lock pin actuator

(Sandia National Laboratories)

Photo Lithography

Procedure



Light
Mask
Photoresist
Si substrate
Positive photoresist
Negative photoresist

Lithography process (1)

- Basic step of photolithography

Clean wafers

(Solvent removal, hydrous oxide removal, removal of residual organic, ionic contamination..)

↓

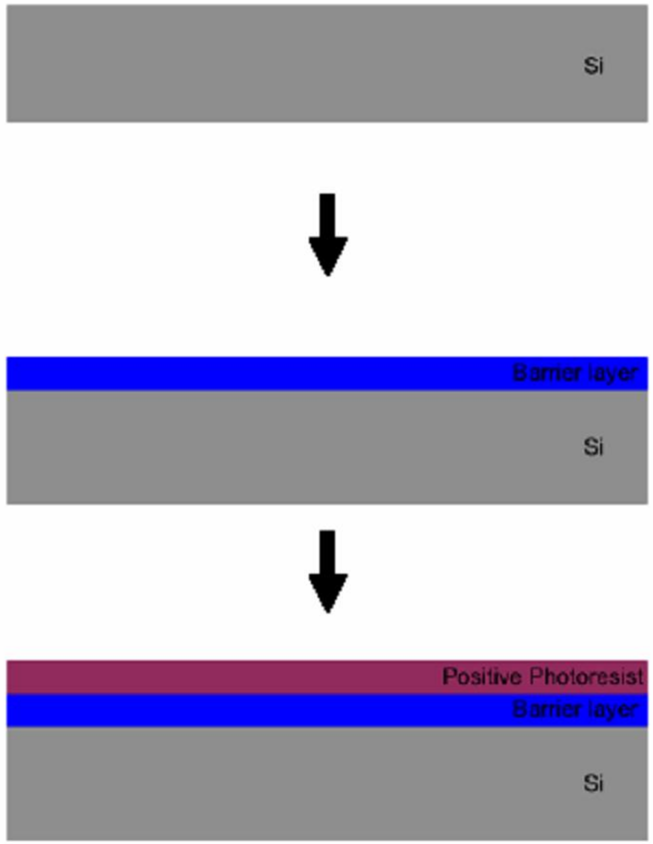
Deposit barrier layer

(SiO_2, Si_3N_4, metal..)

↓

Coat with photoresist

- HMDS (enhance adhesion to Si) coating
- Photoresist coating



Lithography process (2)

Soft bake

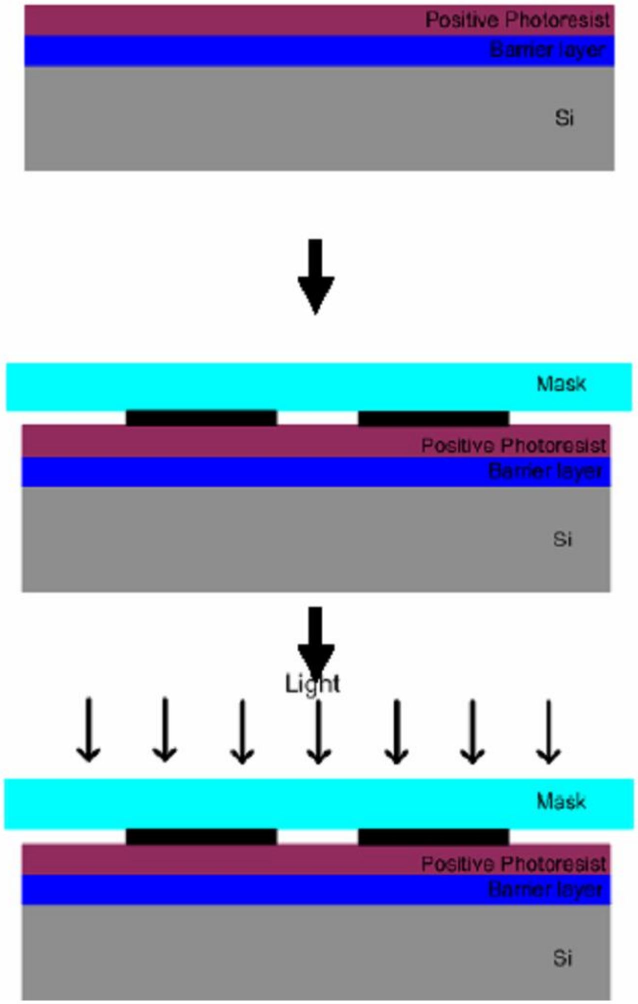
- Improve adhesion
- Remove solvent from PR
- 5-30 min in the oven at 60-100 ℃

Align masks

- Each mask must be aligned to the previous pattern on the wafer

Expose pattern

- Expose through mask with high-intensity UV light



Lithography process (3)

Develop photoresist

- develop the PR pattern on substrate

↓

Hard bake

- harden the PR
- improve adhesion to substrate
- 20-30 min in the oven at 120-180 ℃

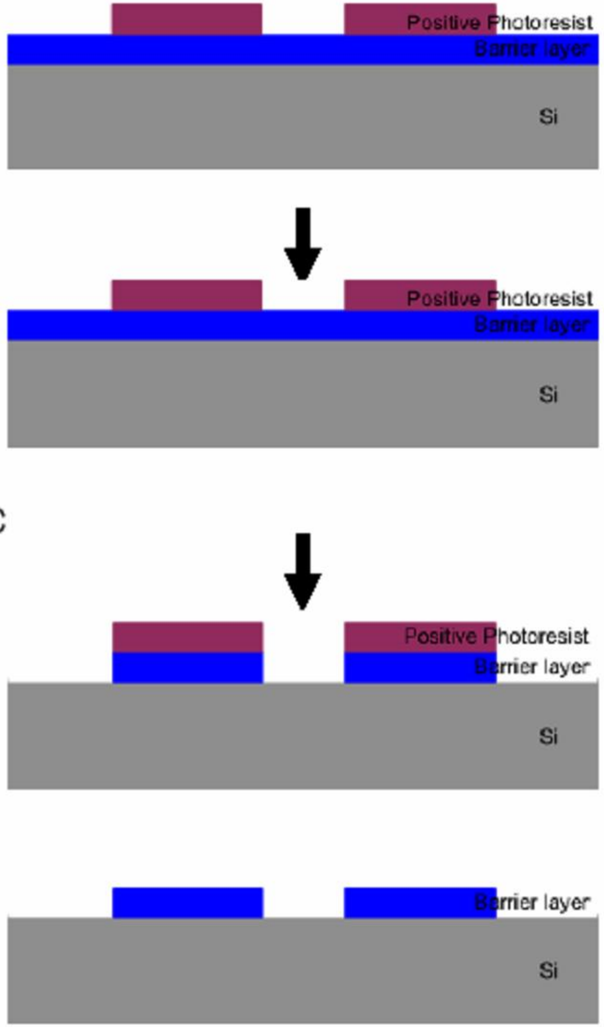
↓

Etch windows in barrier layer

- wet / dry etch

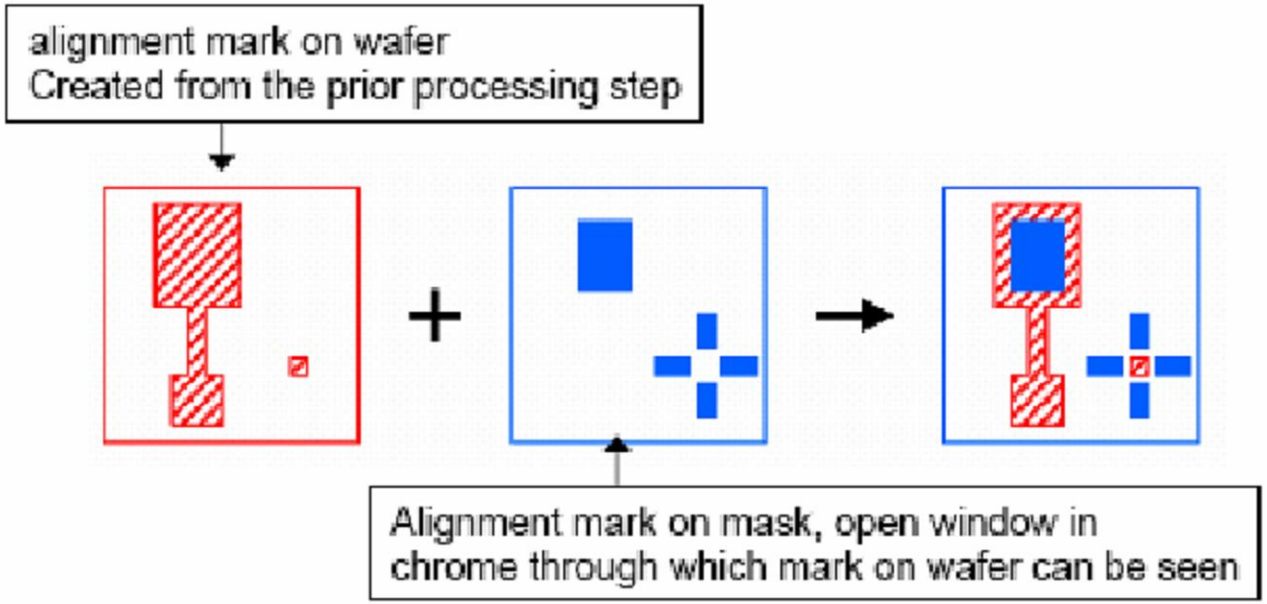
↓

Remove photoresist

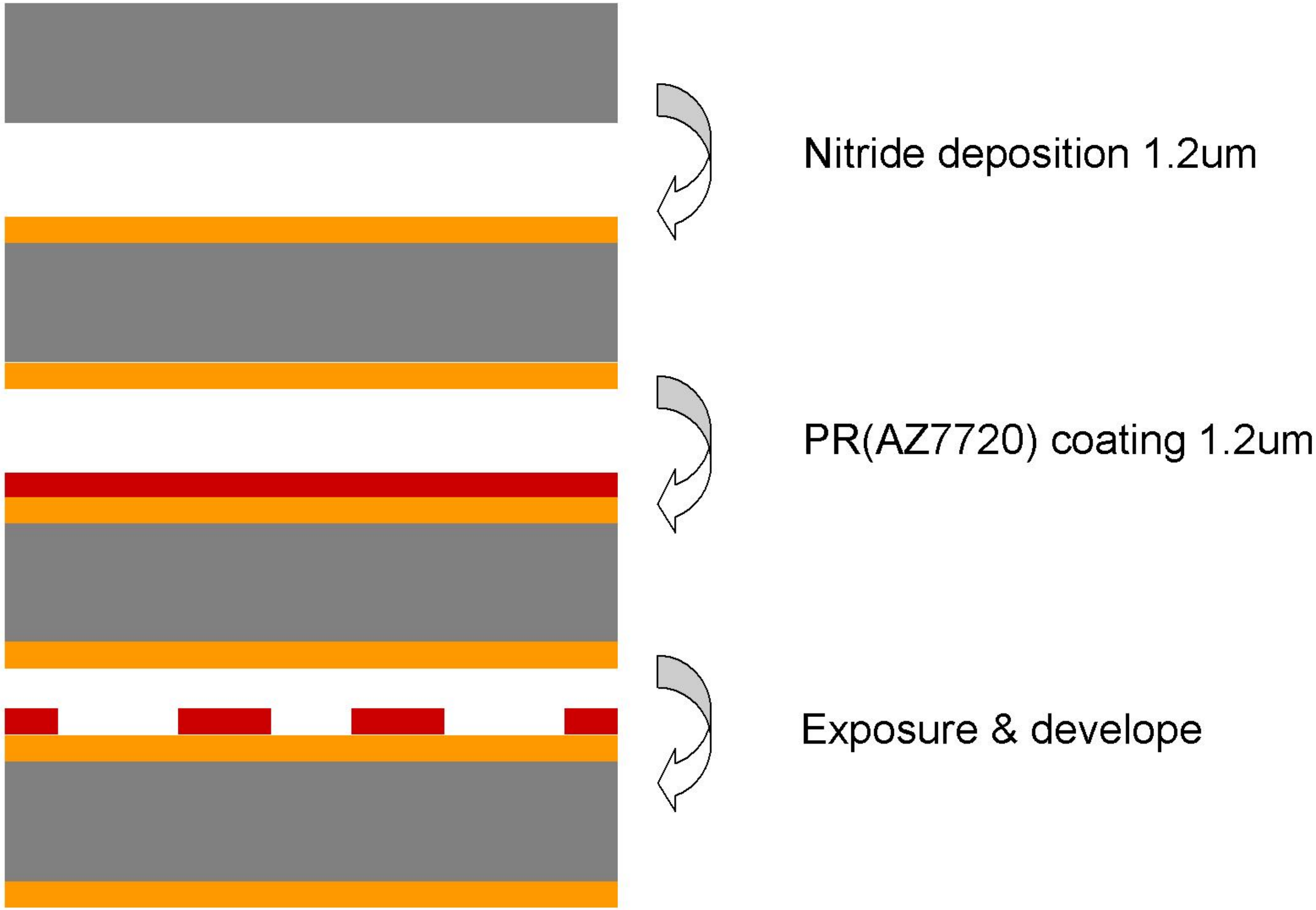


Mask to wafer alignment

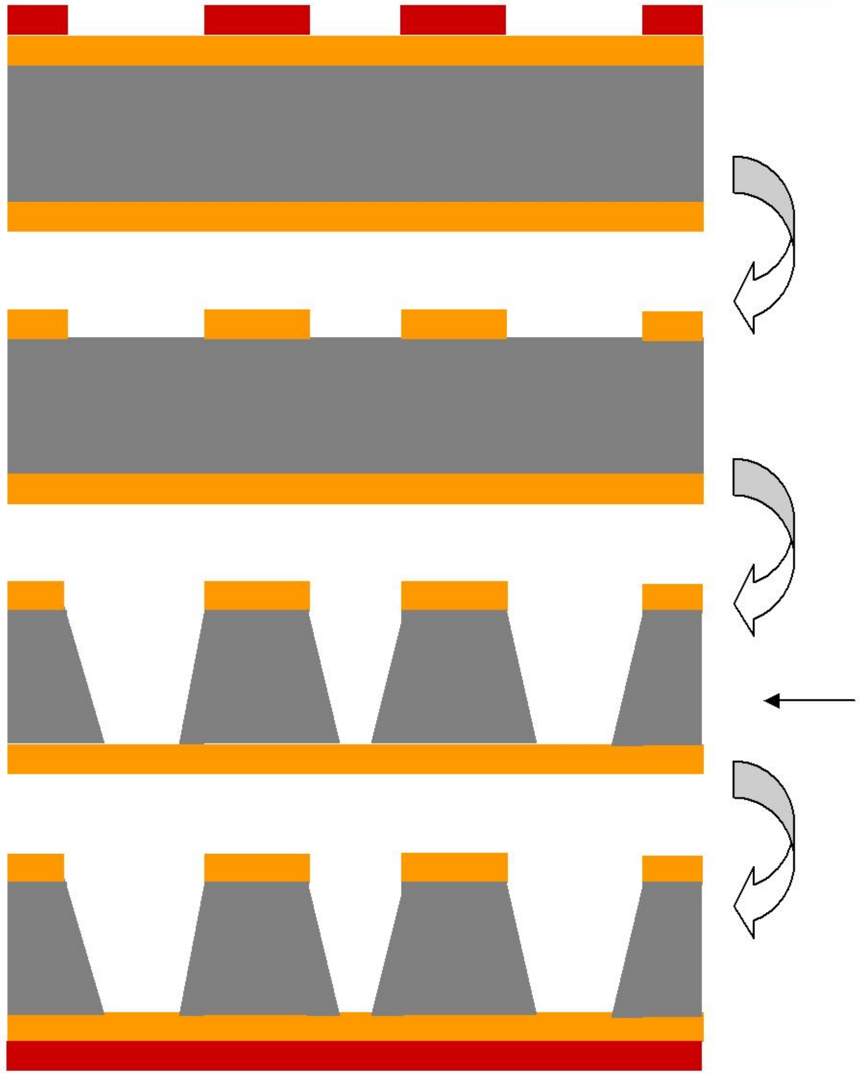
- Alignment: Each mask following the first must be carefully aligned to the previous pattern on the wafer
- 3 degrees of freedom between mask and wafer: (x,y,q)
- Use alignment marks on mask to register patterns prior to expose



Device Fabrication (1)



Device Fabrication (2)



RIE process (nitride layer etching)

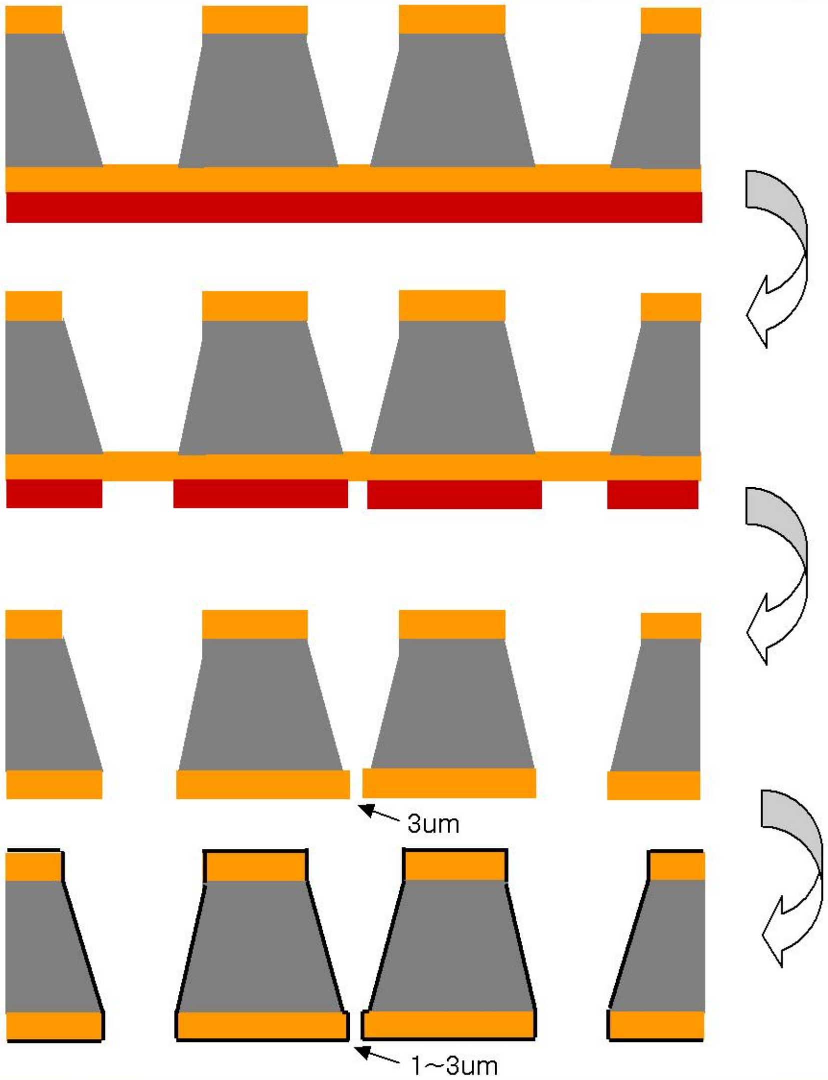
& Ashing

Wet etching (KOH)

Backside complete

PR(AZ7720) coating 1.2um

Device Fabrication (3)



Exposure & develop

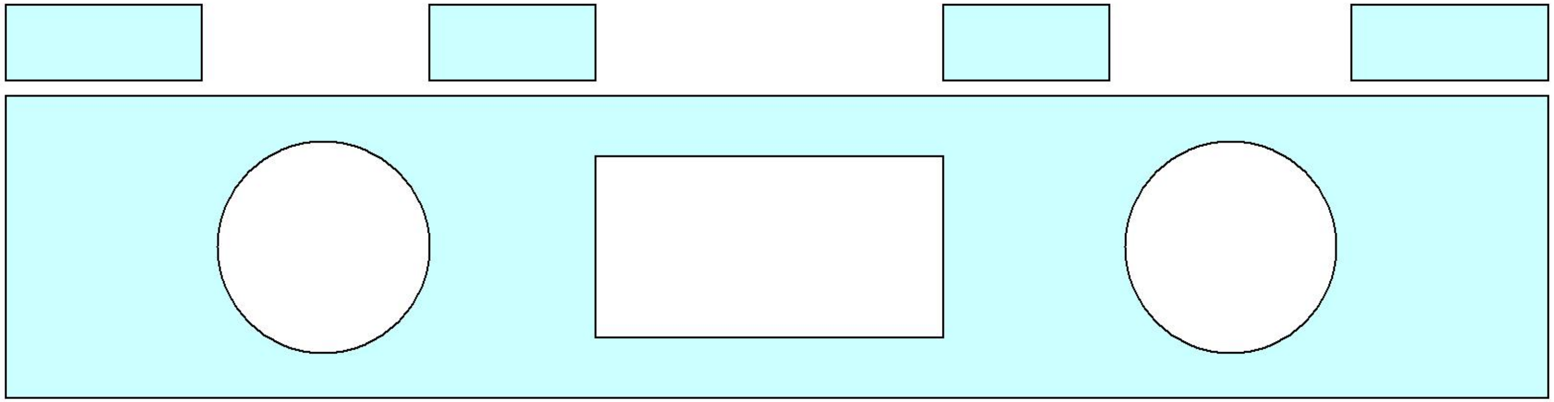
Deep RIE (Nitride etching)
& Ashing

Oxidation (hole size reducing)

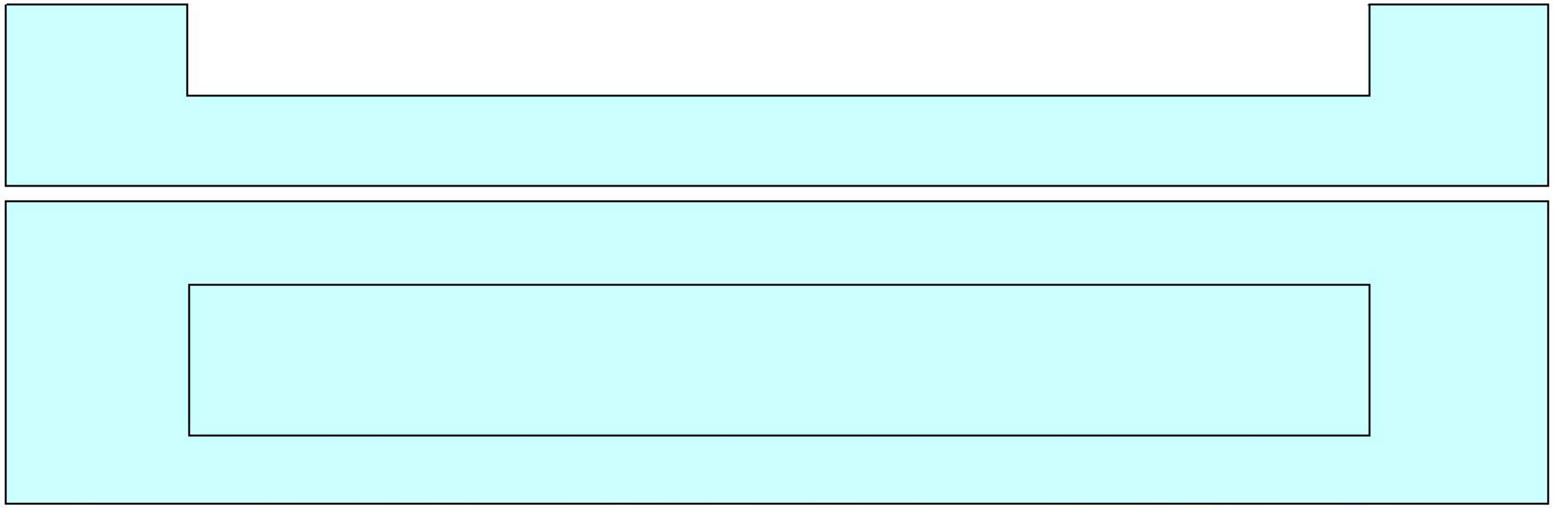
5000A

Device Fabrication (4)

Upper PDMS



Bottom PDMS



Device Fabrication (5)

Assemble all parts (plasma bonding)