

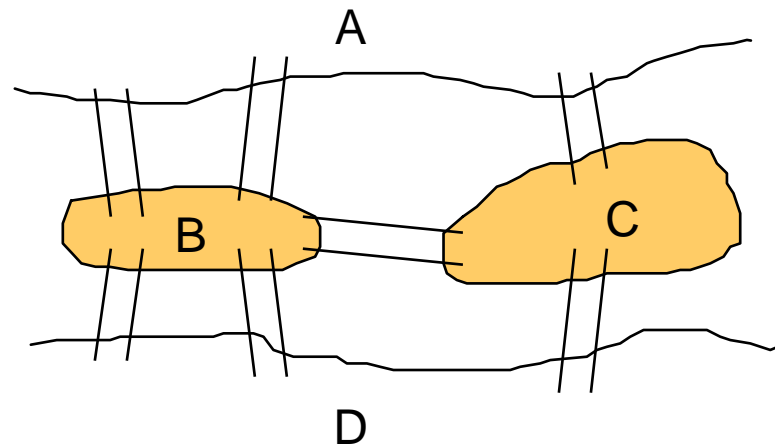
Introduction

(4541.554 Introduction to Computer-Aided Design)

School of EECS
Seoul National University

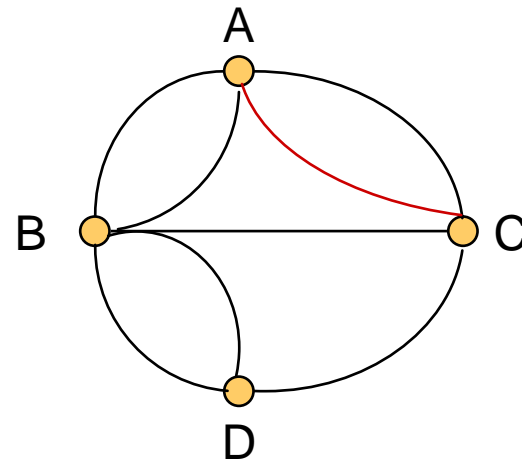
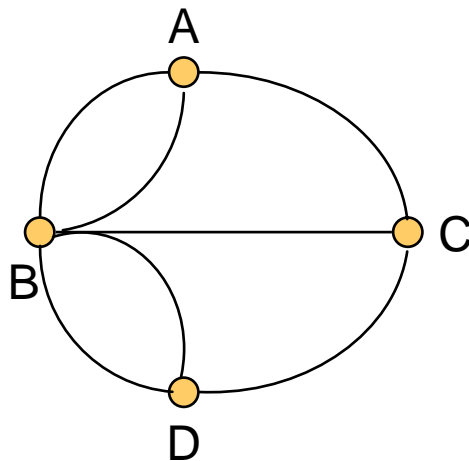
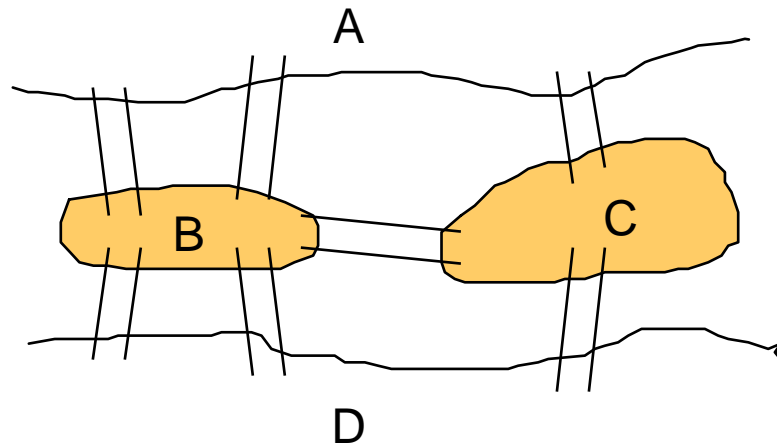
Warming Up

- **Königsberg Bridge Problem**
 - Königsberg (Kaliningrad) bridges
 - Walk across each bridge exactly once



- **Euler Trail**

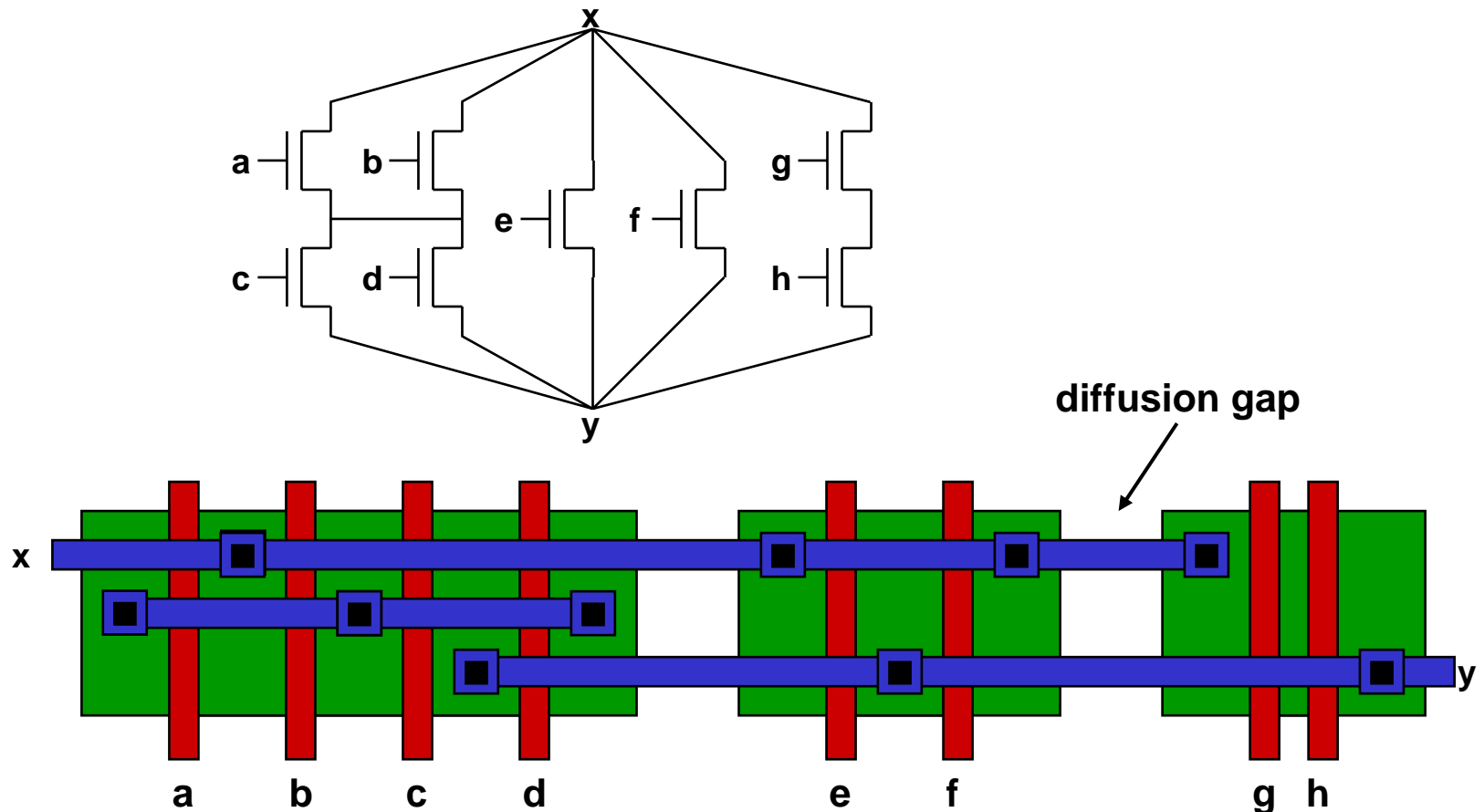
- **Model it as a graph**
- **Euler trail: a trail that traverses all edges exactly once**
- **No more than 2 vertices must have odd degree**



- **Functional Cell Design**

- **Layout**

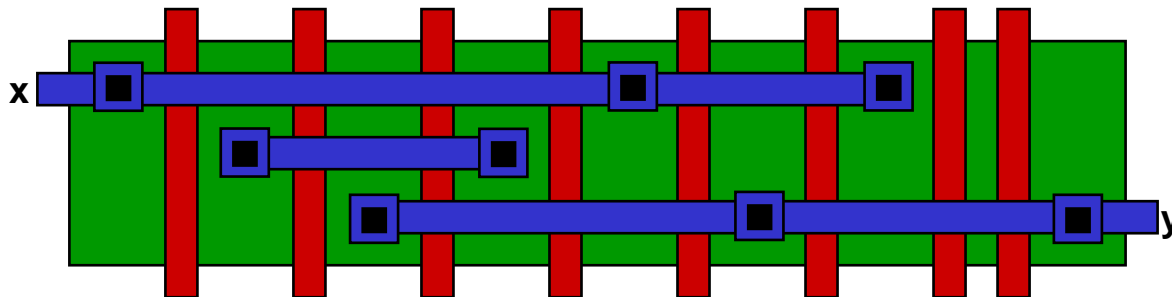
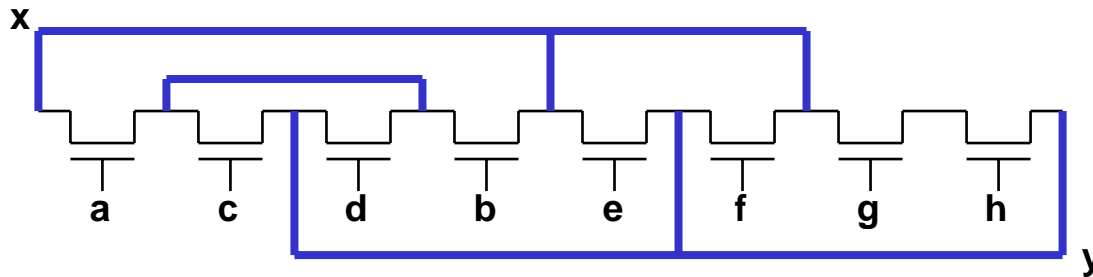
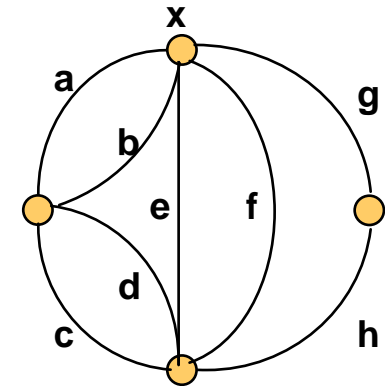
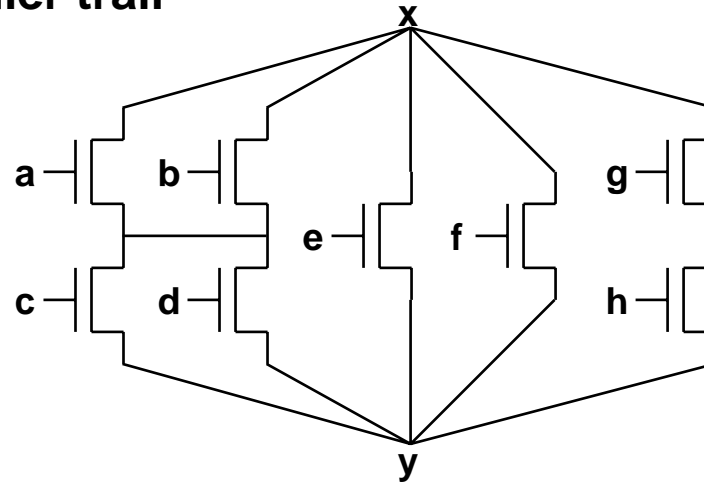
- **Layers: diffusion, metal, poly**
 - **Linear array of transistors**
 - **Avoid diffusion gaps to minimize area**



- **Functional Cell Design**

- How to minimize the number of diffusion gaps?

- Find an Euler trail

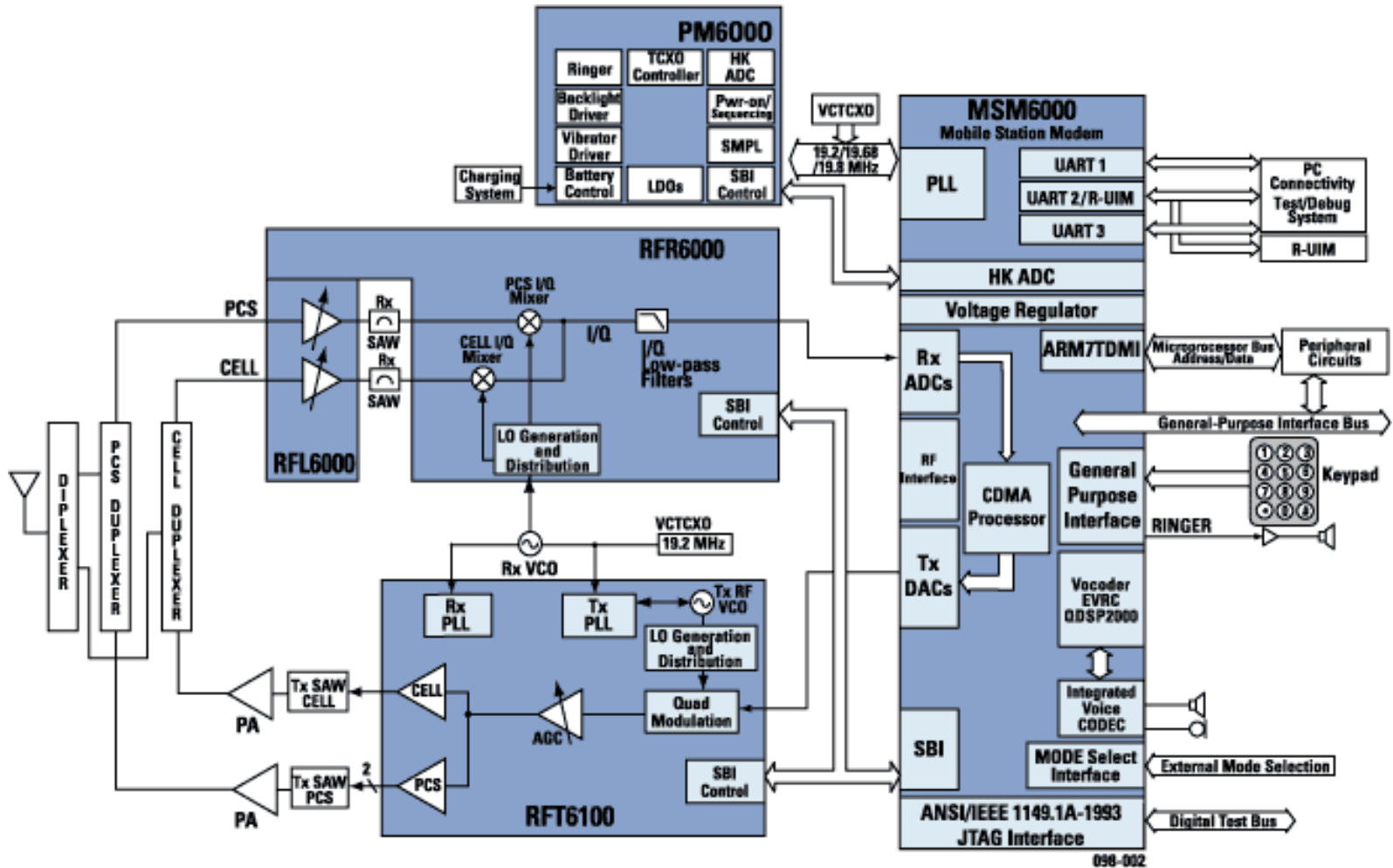


Electronic Systems Design

- **Embedded systems**



- 3G Mobile Communication (CDMA2000)

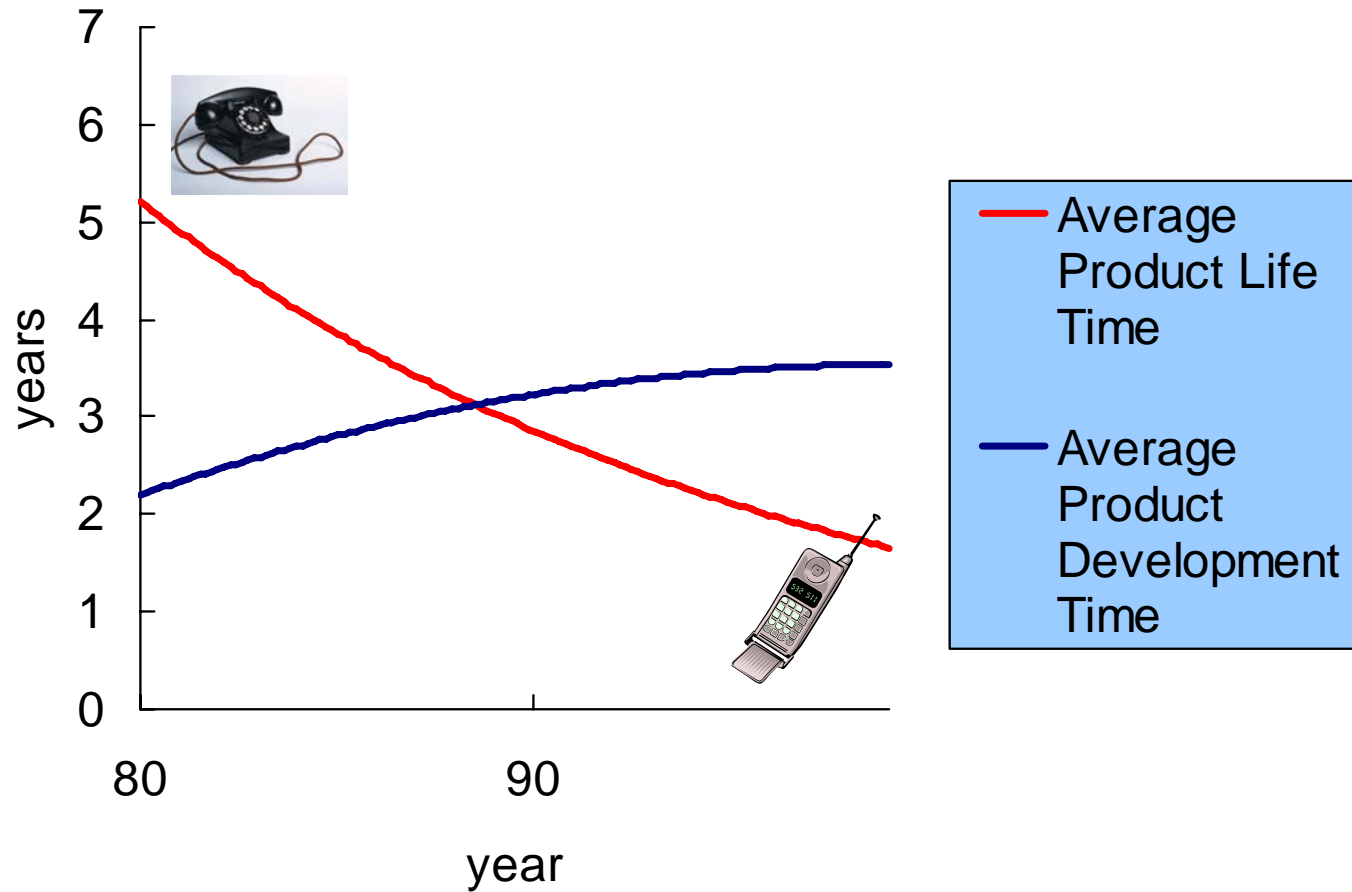


Major Factors to be Considered

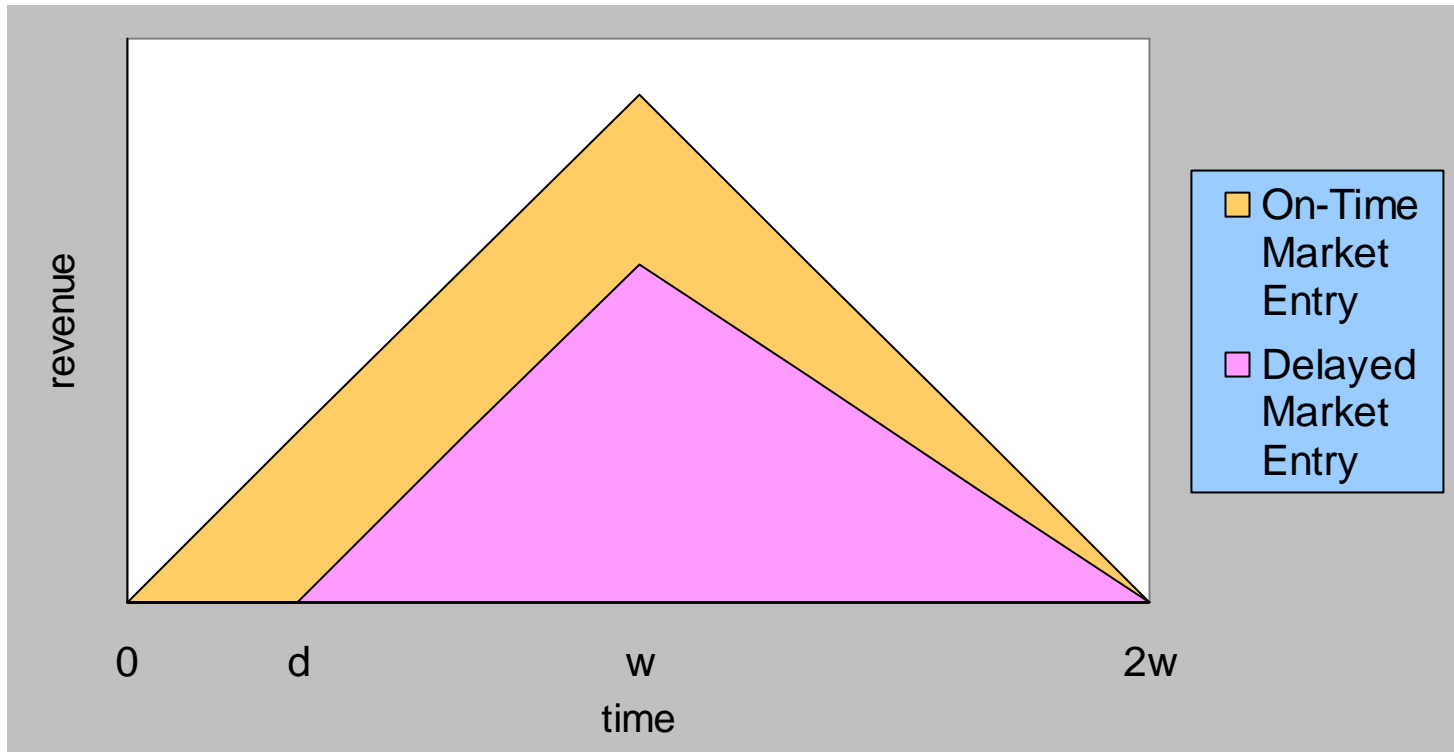
- **Time-to-market**
- **Technology**
- **Performance**
- **Power consumption**
- **Reliability**
- **Testability**
- **Availability of CAD tools, libraries, IP's**
- **Cost, chip area**
- **...**

Time-to-Market

- Product life time vs. development time



- Revenue and time-to-market

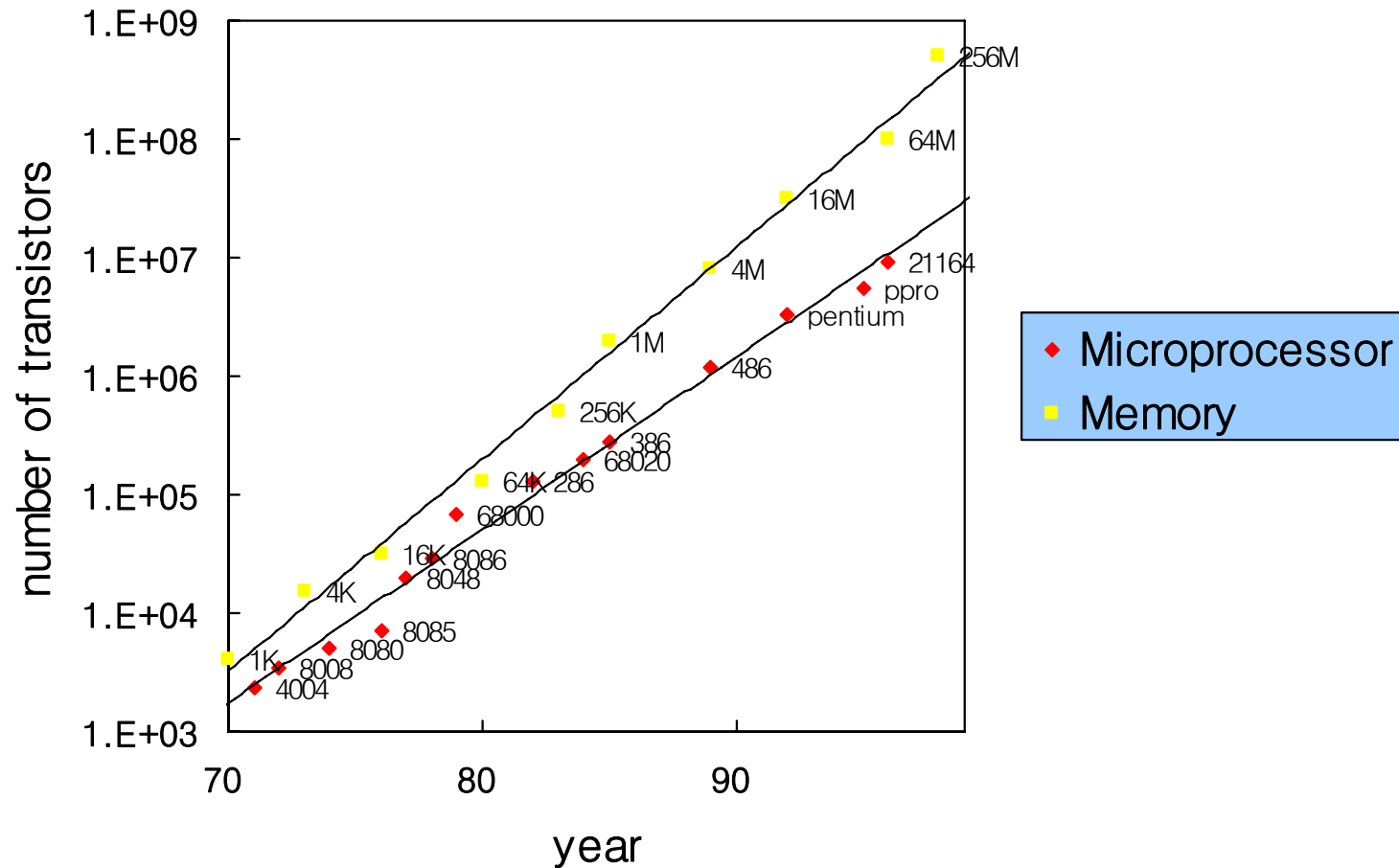


$$\text{Lost Revenue} = \text{Total Expected Revenue} \times \frac{d(3w - d)}{2w^2}$$

w = 1 year, d = 4 months → 40.5% lost

Technology

- Memory capacity quadrupled every three years



- **Problems with deep sub-micron design**

- **Thin wire**

- Large interconnect delay
- delay \propto (wire length)²
- Al --> Cu

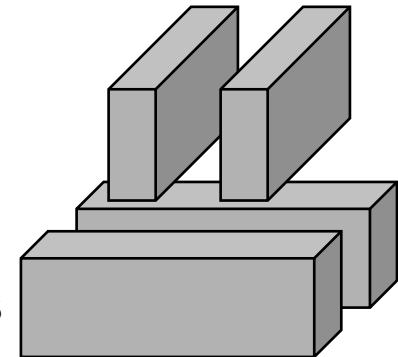
- **H > W**

- Delay due to larger edge capacitance
- Cross-talk with neighboring wires
- Permutation of signal wires
- Interleaving with power and ground wires

- **Clock distribution**

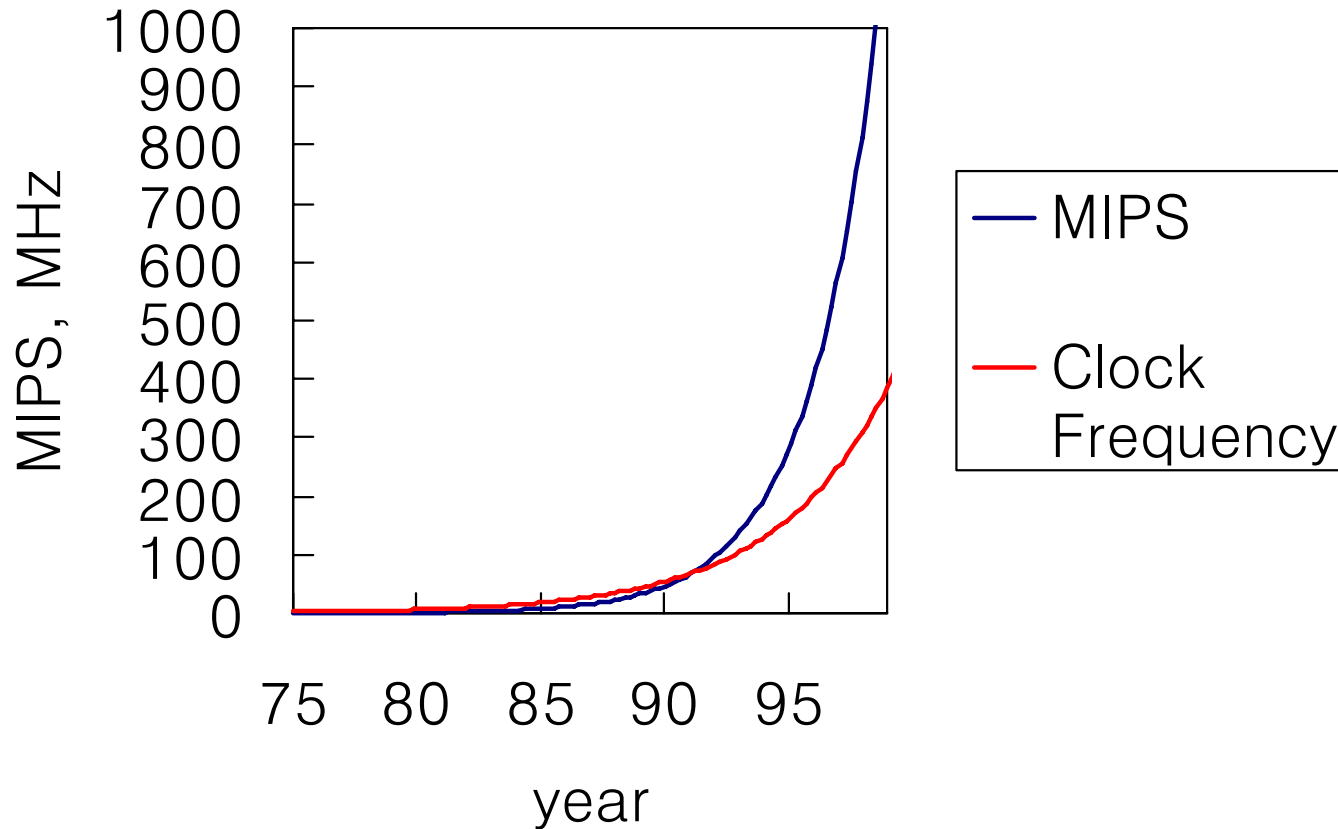
- **Heat dissipation**

- ...



Performance

- **Microprocessor performance and clock frequency**



Power Consumption

- **Why low power?**
 - High performance and integrity of VLSI circuits
 - Popularity of portable devices
- **Power consumption in CMOS circuits**
 - Dynamic power dissipation (dominant)
 - Short-circuit power dissipation
 - Leakage power dissipation
- **Dynamic power dissipation**

$$P_{dynamic} = \alpha \cdot C_{phy} \cdot V_{dd}^2 \cdot f_{clk}$$

where

α : switching activity

C_{phy} : physical capacitance

V_{dd} : supply voltage

f_{clk} : clock frequency

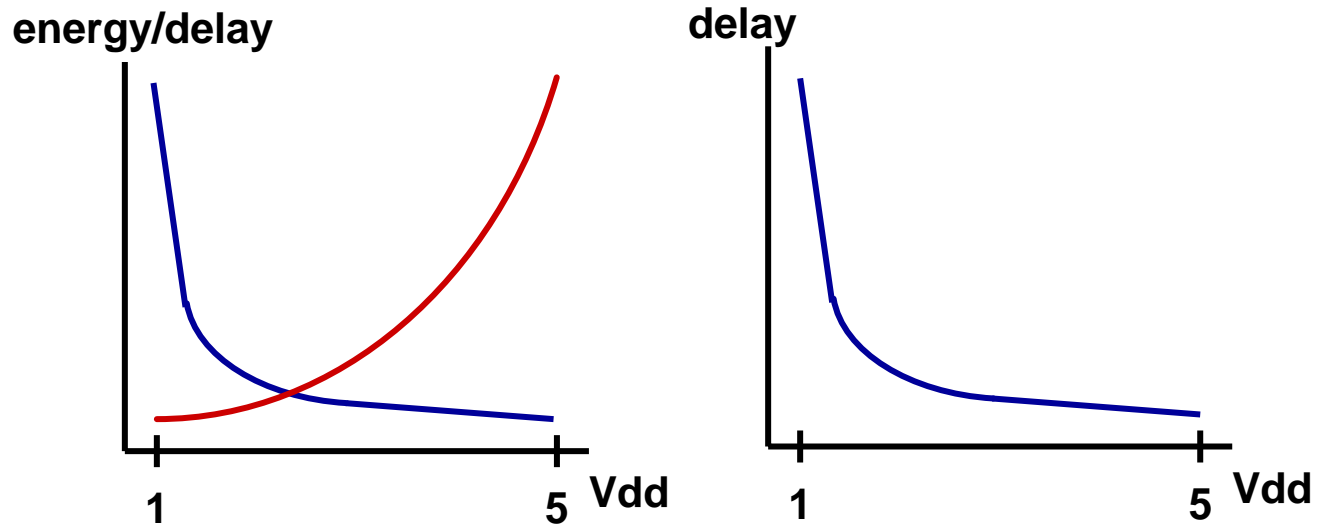
- **Supply voltage reduction**

- Quadratic effect of voltage scaling on power

$$P_{dynamic} = \alpha \cdot C_{phy} \cdot V_{dd}^2 \cdot f_{clk}$$

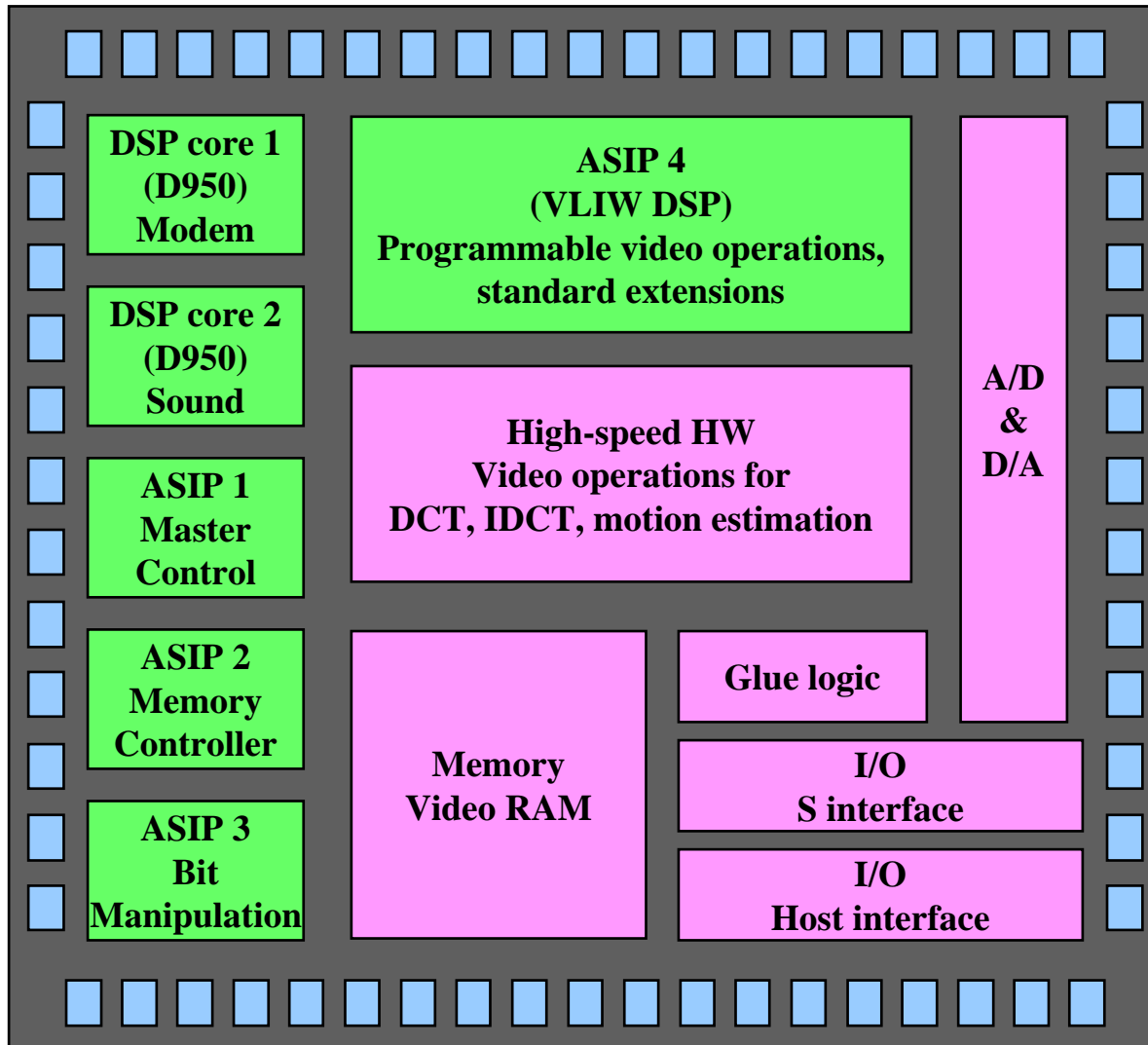
5V --> 3.3V => 60% power reduction

- Supply voltage reduction => increased latency



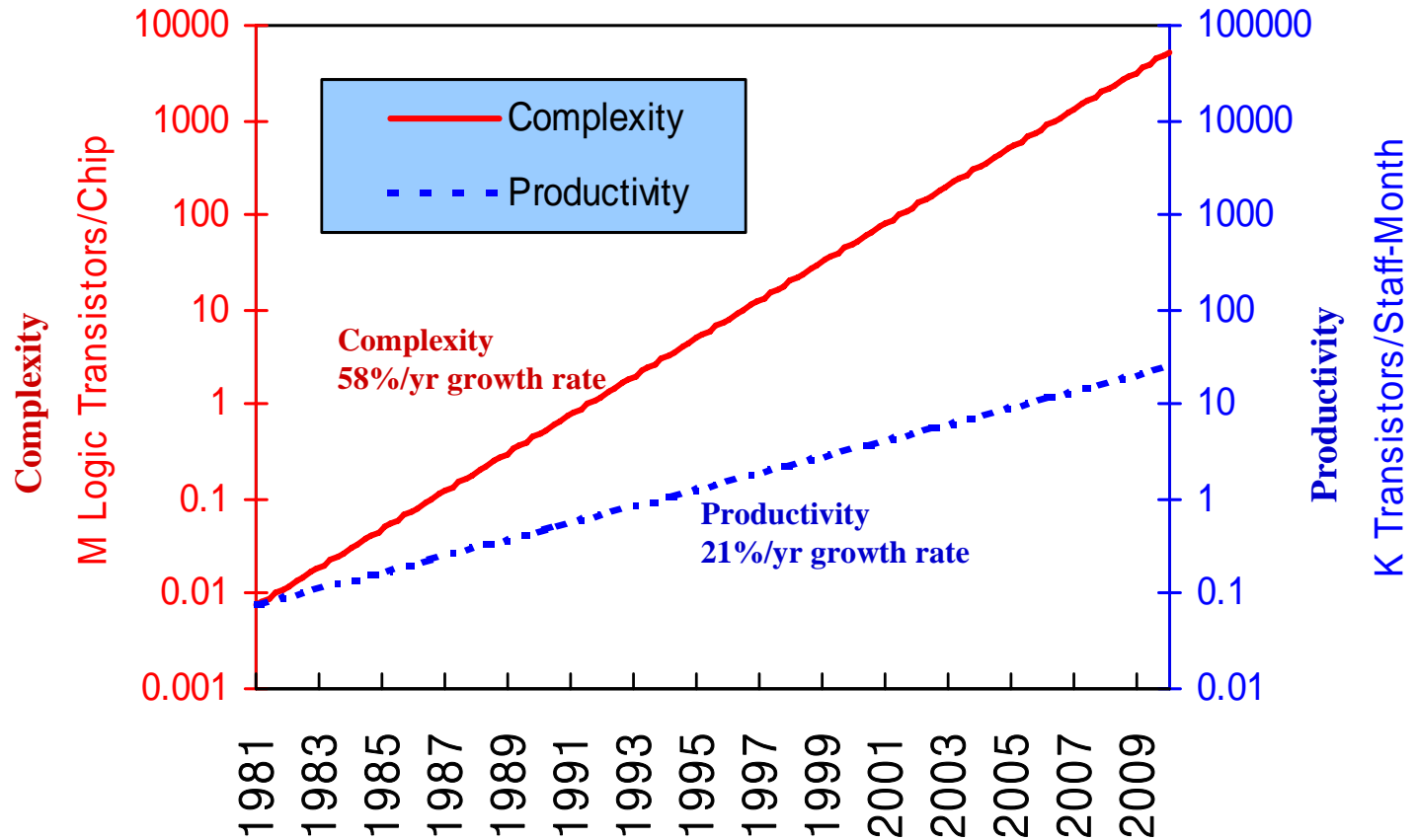
System-On-Chip

- **Example**

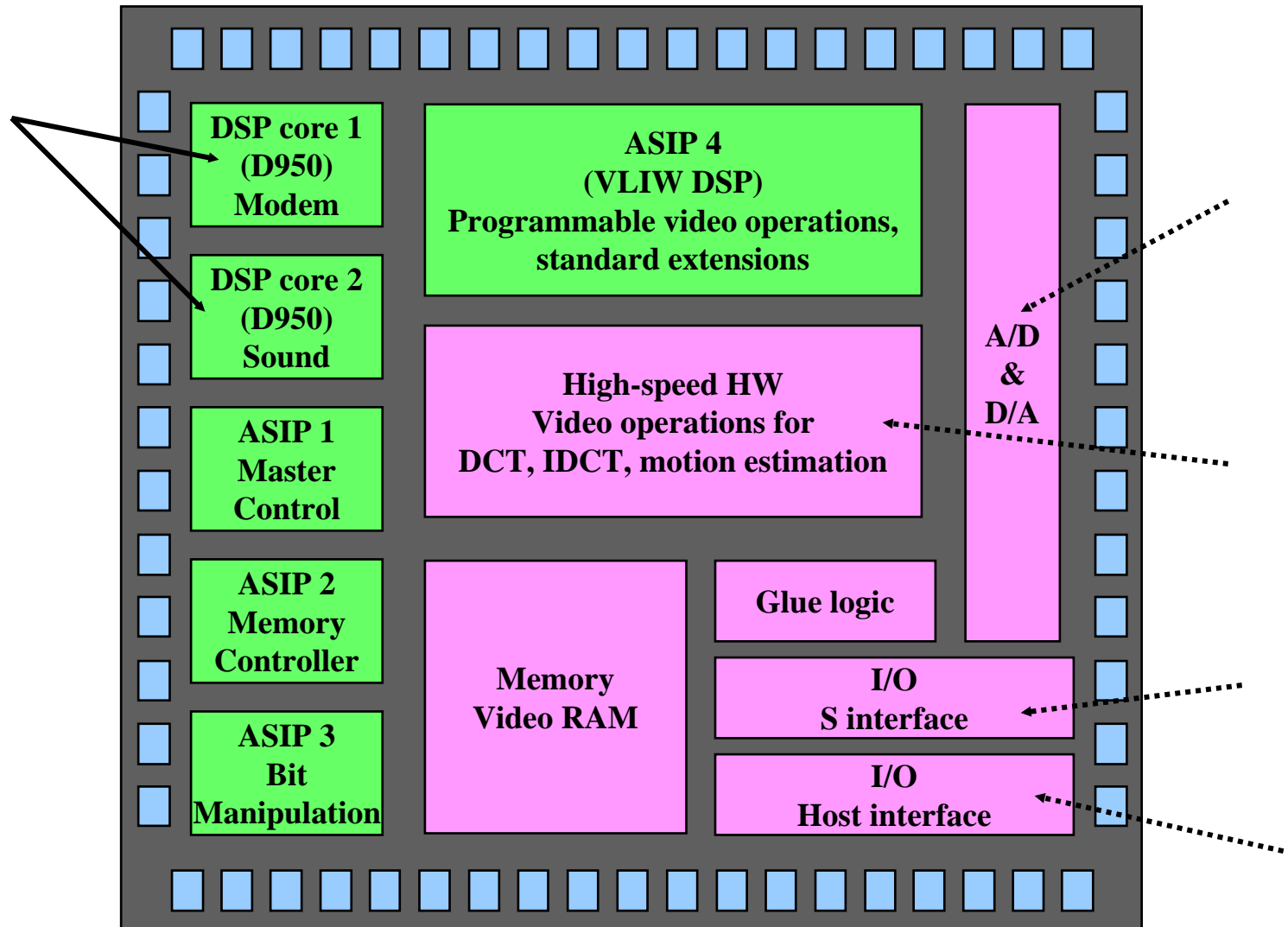


**Single chip
videophone
(H.263)**

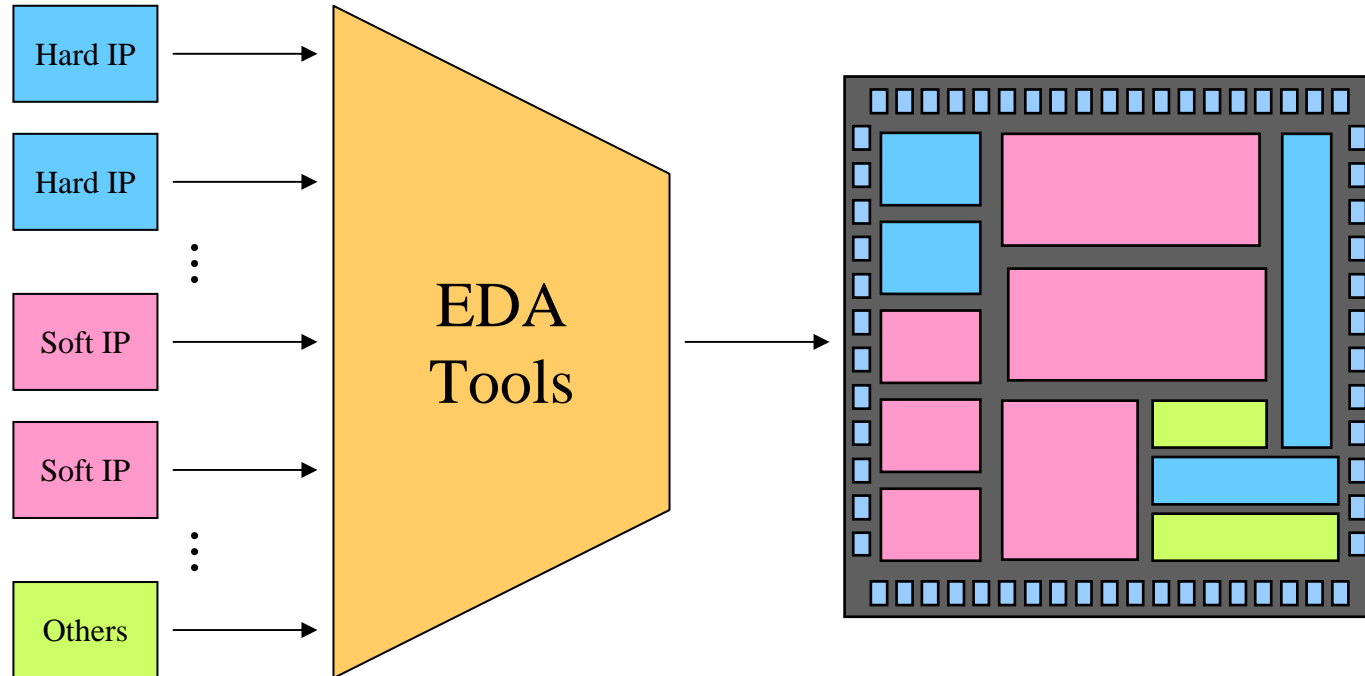
- **IP/Platform-Based Design**
 - Complexity vs. productivity



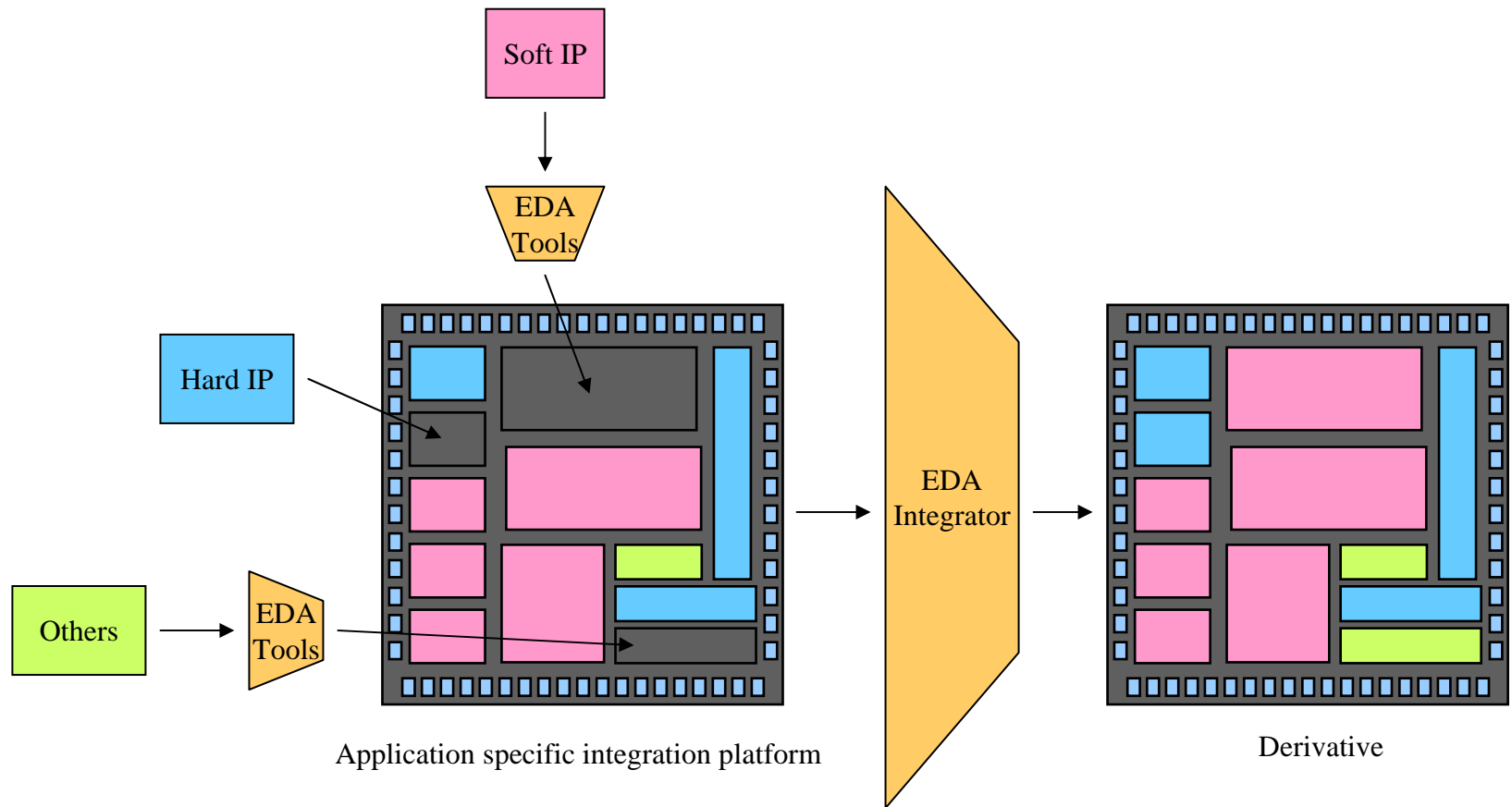
– Reuse of IPs



- IP-based design



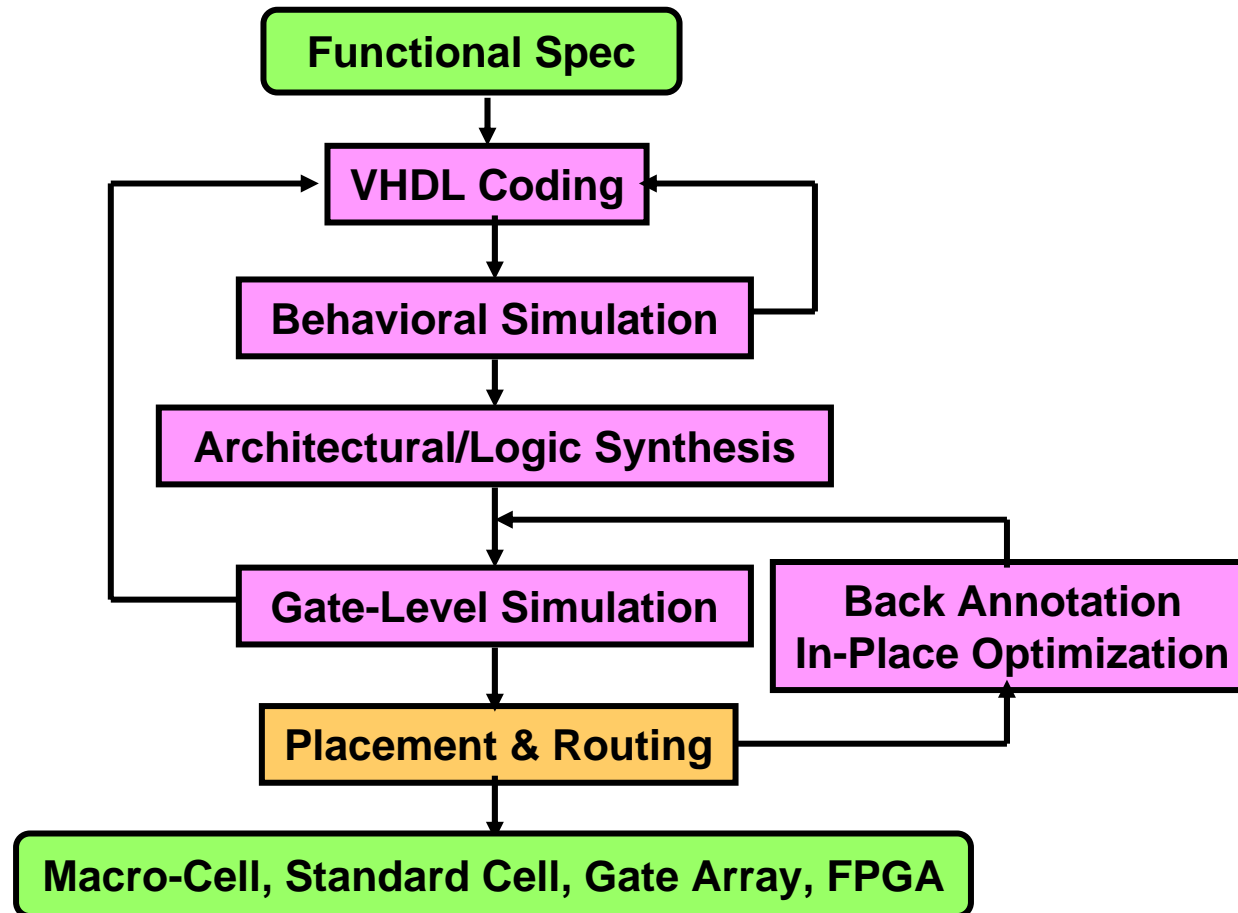
– Platform-based design



Hardware Design

- **Initial design moves toward more abstract levels as the complexity increases**
 - Top-down design with libraries
 - Synthesis tools are used
 - Layout design: layout editor
 - Symbolic layout: layout compactor
 - Gate-level design: technology mapping, P&R
 - RT-level design: Logic synthesis tool
 - Behavioral-level design: Architecture synthesis tool
- **Behavioral-level/RTL design using HDL**
 - VHDL, Verilog, ...
 - Validation by simulation
 - Refine using synthesis tools
 - Gate-level simulation
 - Placement, routing
 - Circuit/delay extraction, back-annotation
 - Simulation, LVS
 - Emulation, prototyping

- Design flow example

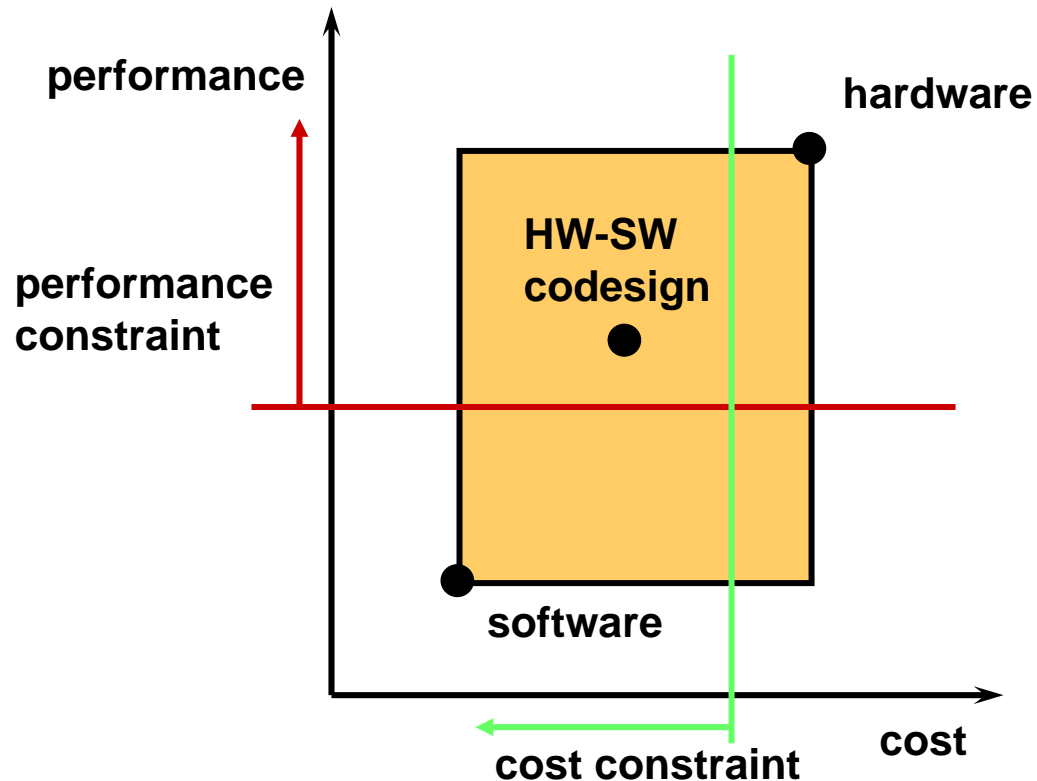


Software Design

- **Paradigm shift toward software**
 - Microprocessor performance rapidly increases
 - Flexibility, upgradability
 - Low cost
- **Microprocessor, microcontroller, DSP, ASIP**
- **Code optimization in embedded systems**
 - Minimization of memory size
 - Maximization of performance
 - Minimization of power consumption
- **Estimation of the execution time**
 - Worst case performance (hard real-time)
 - Probabilistic performance (soft real-time)
 - Average case performance (no real-time)

Hardware-Software Co-Design

- **Benefits of co-design**
 - **Balancing**
 - Performance of customized HW units
 - Programmability of low cost SW components



– Reduction of design time

