Memory

Read-Only Memories

- **Mask ROM**
  - **Programmed permanently during manufacturing process**
- **Programmable ROM**
  - **PROM**
    - **programmed by fusing or anti-fusing process**
    - **the process is irreversible**
  - **Erasable PROM**
    - **UV EPROM**
    - **EEPROM**

Random Access Memories

- **Transistor efficient methods for implementing storage elements**
- **Small RAM: 256 words by 4-bit**
- **Large RAM: 1 billion words by 1-bit**
- **Static RAMs and Dynamic RAMs**

Static RAMs

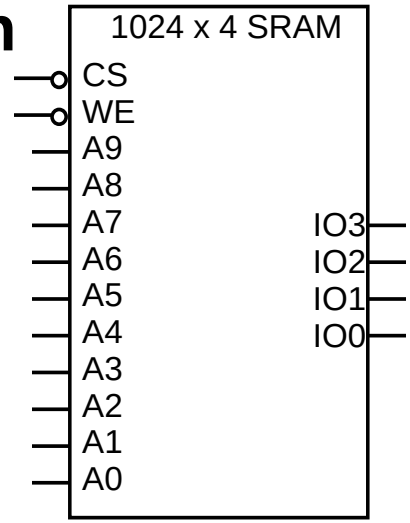
- **We will discuss a 1024 x 4 organization**

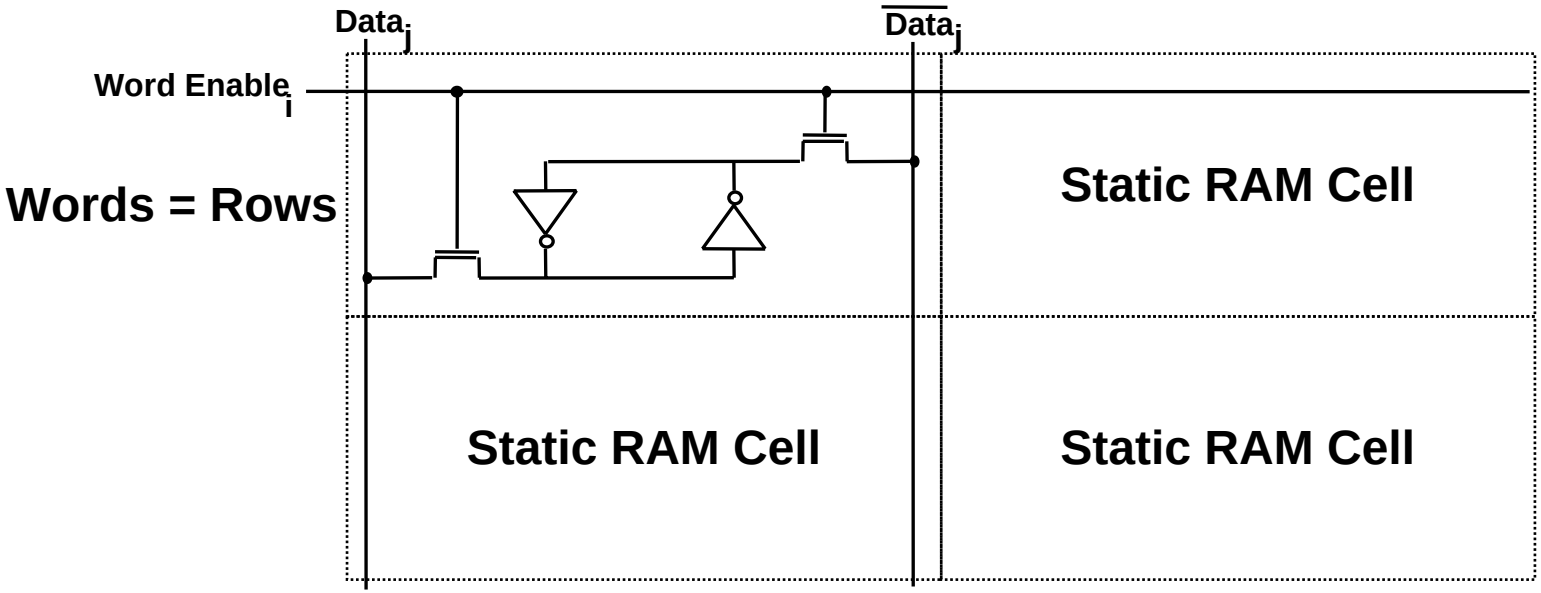
  Chip Select Line (active lo)

  Write Enable Line (active lo)

  10 Address Lines

  4 Bidirectional Data Lines

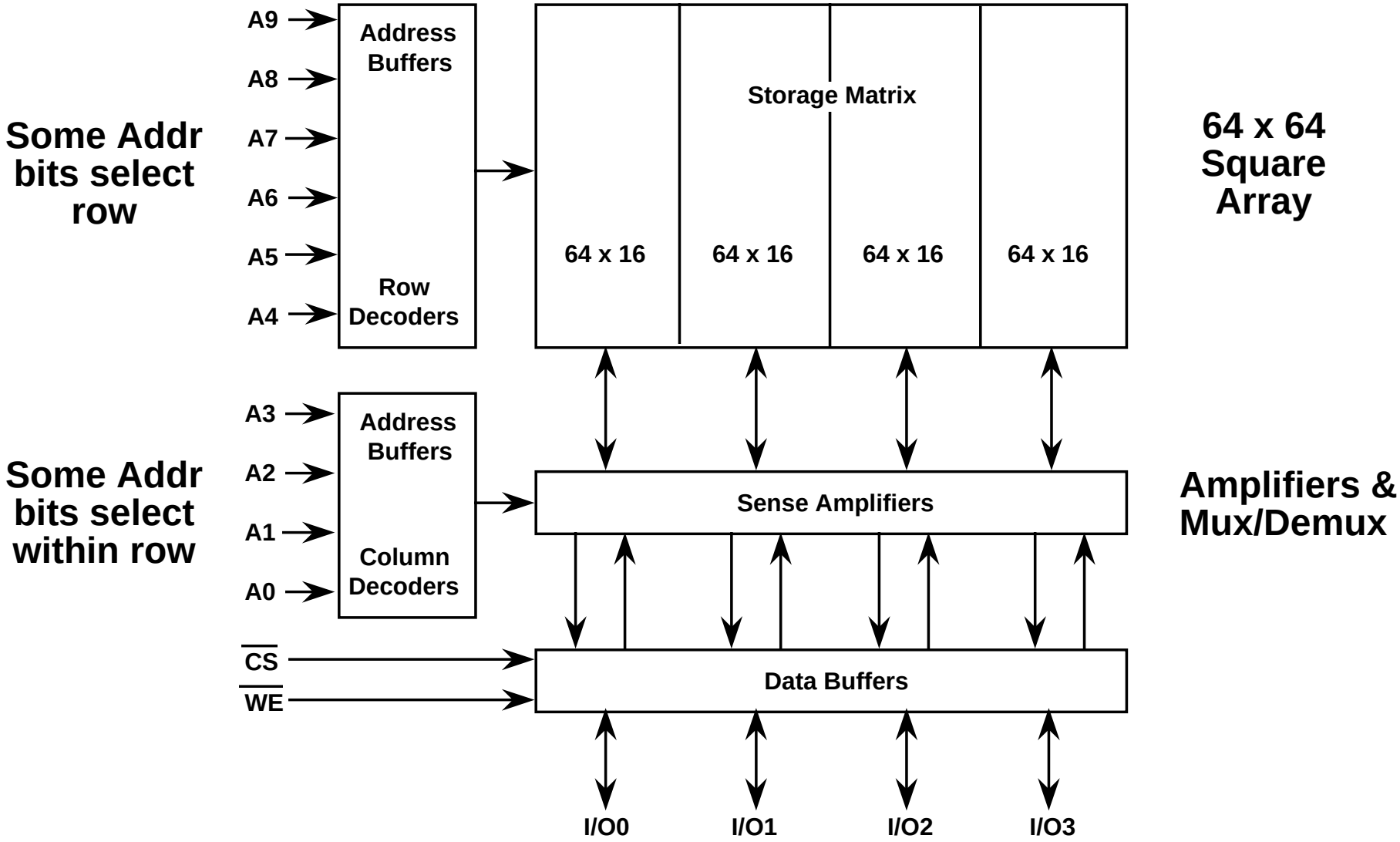




Columns = Bits (Double Rail Encoded)

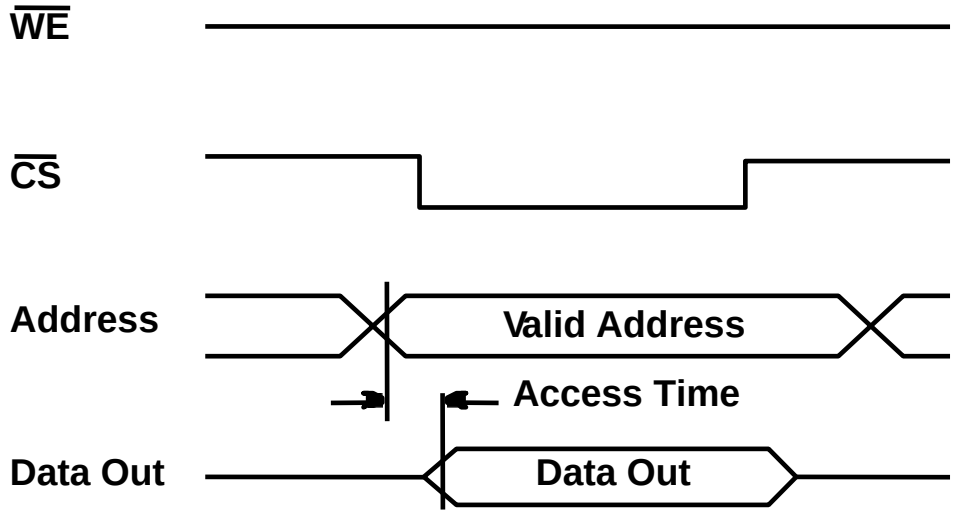
RAM Organization

Long thin layouts are not the best organization for a RAM

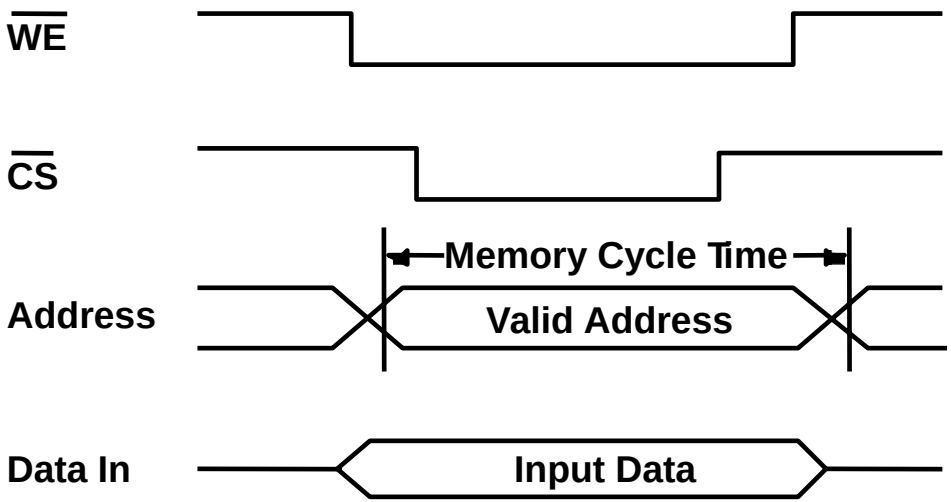


RAM Timing

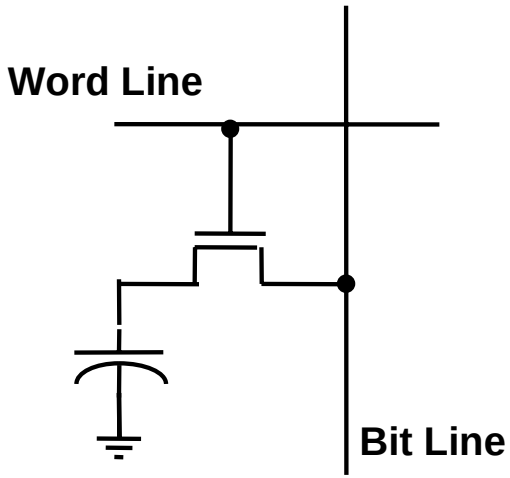
Simplified Read Timing



Simplified Write Timing



Dynamic RAMs



1 Transistor (+ capacitor) memory element

Read: Assert Word Line, Sense Bit Line

Write: Drive Bit Line, Assert Word Line

Need for Refresh Cycles: storage decay in ms

Destructive Read-Out

Internal circuits read word and write back

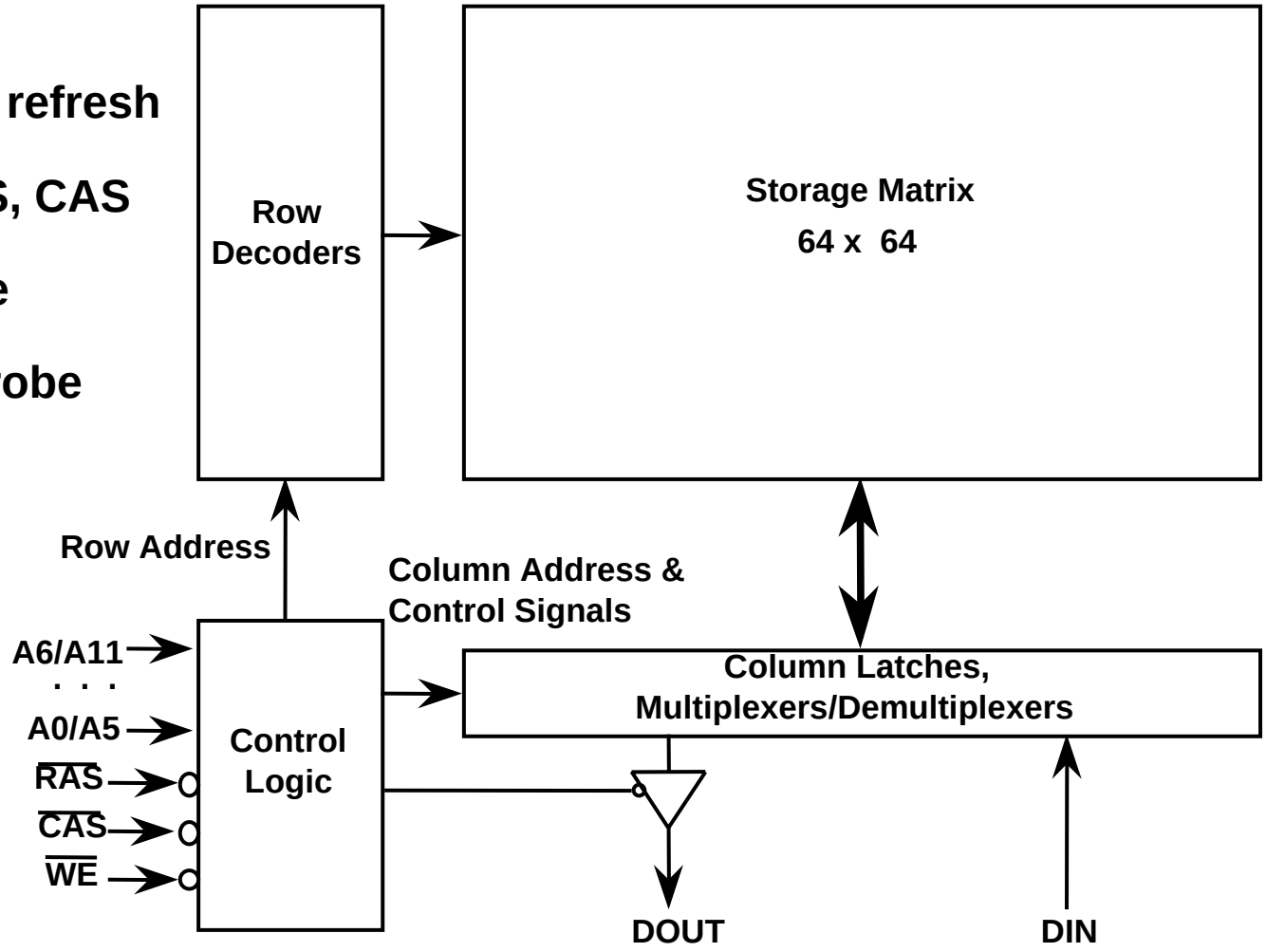
DRAM Organization

Long rows to simplify refresh

Two new signals: RAS, CAS

- **Row Address Strobe**
- **Column Address Strobe**

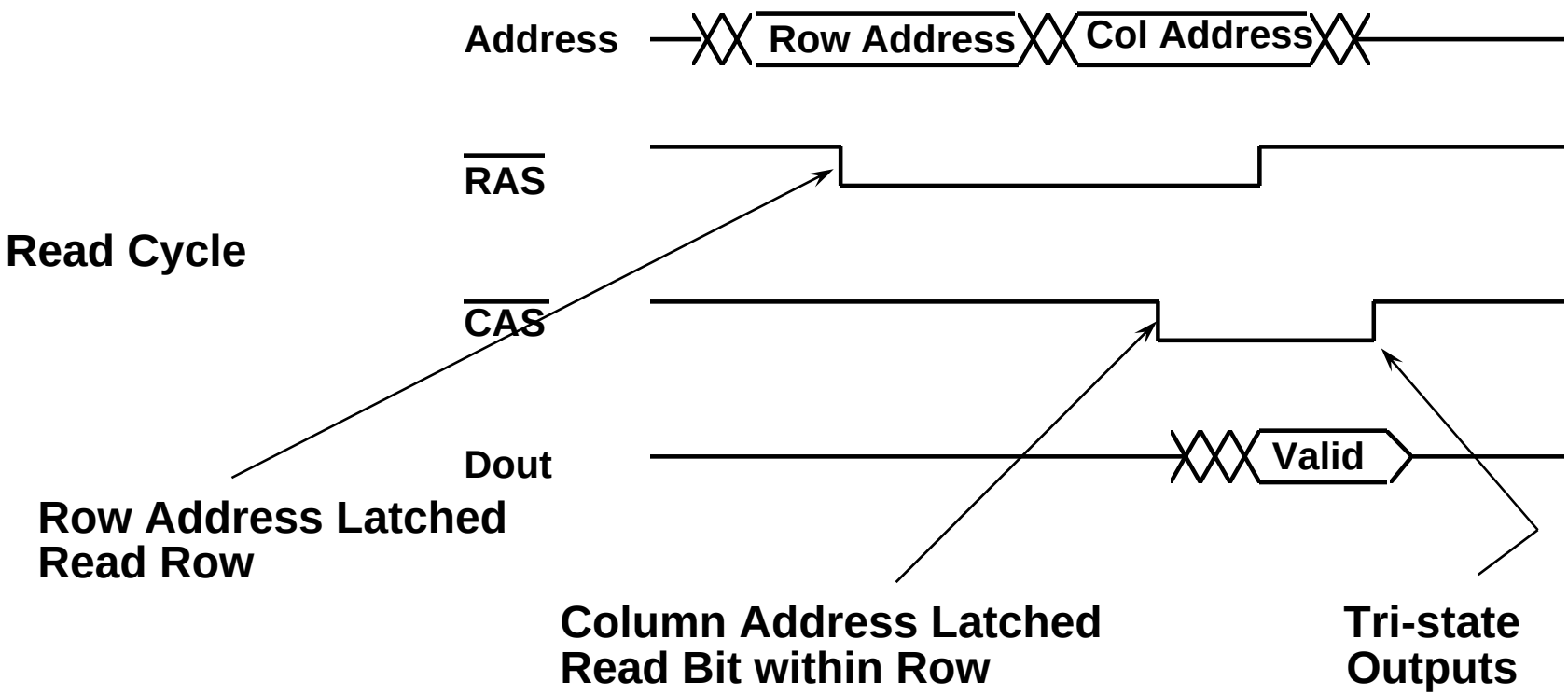
Replace Chip Select



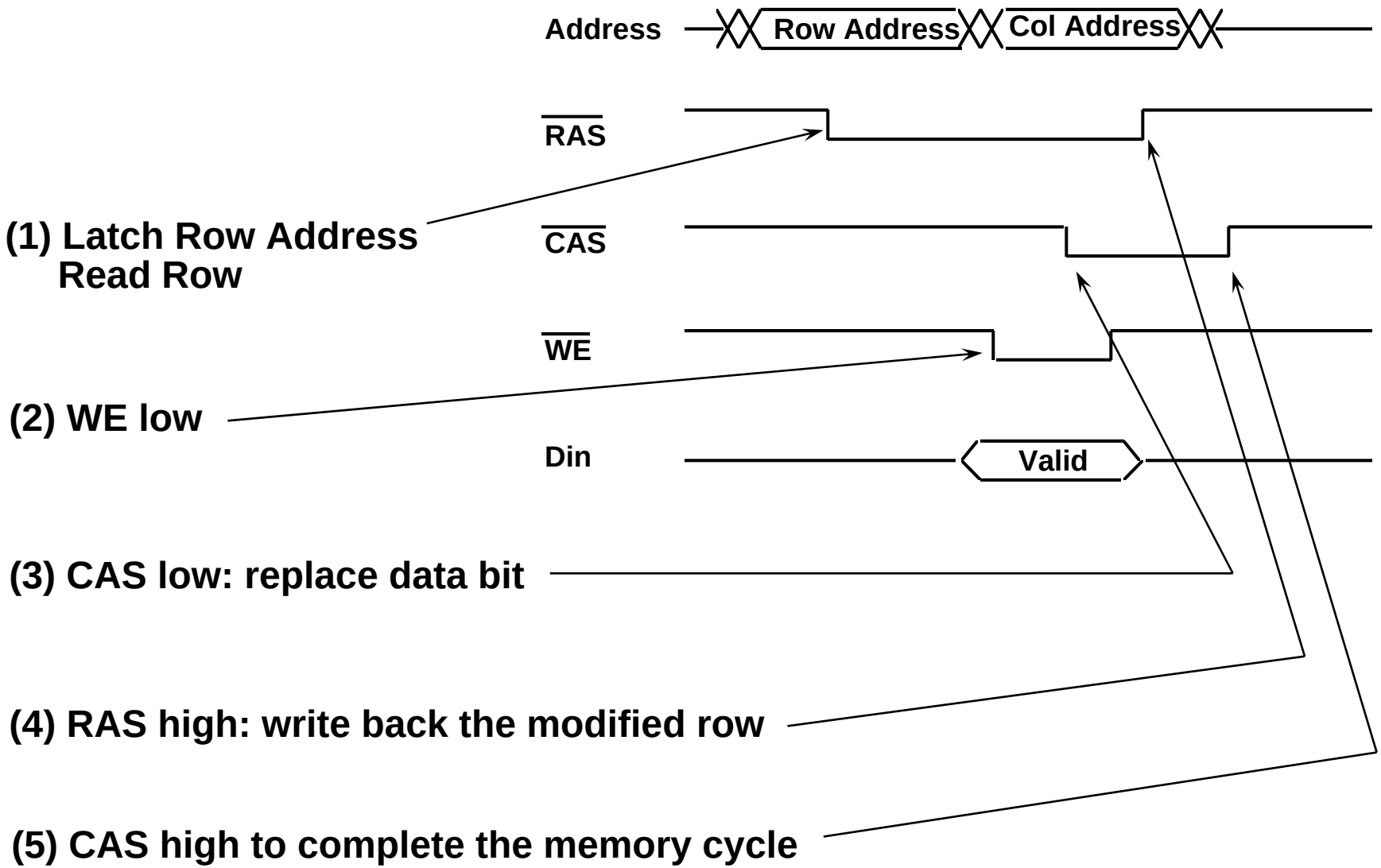
RAS, CAS Addressing

Even to read 1 bit, an entire 64-bit row is read!

Separate addressing into two cycles: Row Address, Column Address
Saves on package pins, speeds RAM access for sequential bits!



Write Cycle Timing



RAM Refresh

Refresh Frequency:

4096 word RAM -- refresh each word once every 4 ms
=> This is one refresh cycle every 976 ns

Assume 120ns memory access cycle
=> 1 in 8 DRAM accesses!

But RAM is really organized into 64 rows
=> This is one refresh cycle every 62.5 μs(1 in 500 DRAM accesses)

Large capacity DRAMs have 256 rows, refresh once every 16 μs

RAS-only Refresh (RAS cycling, no CAS cycling)

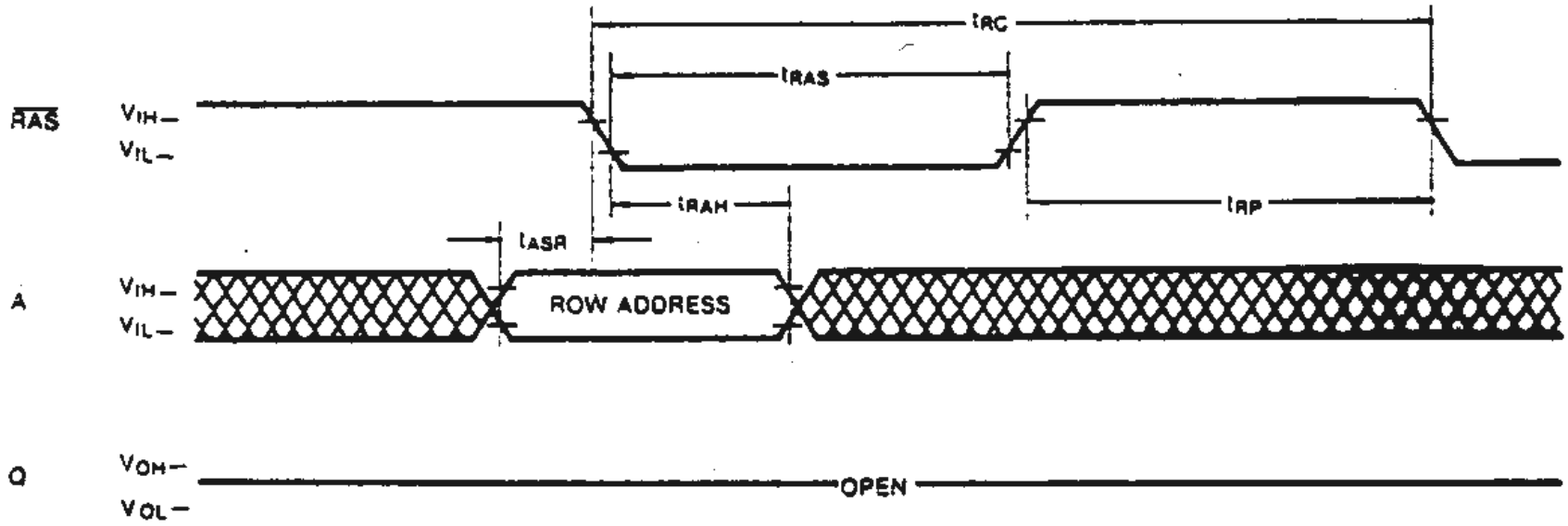
External controller remembers last refreshed row

Some memory chips maintain refresh row pointer

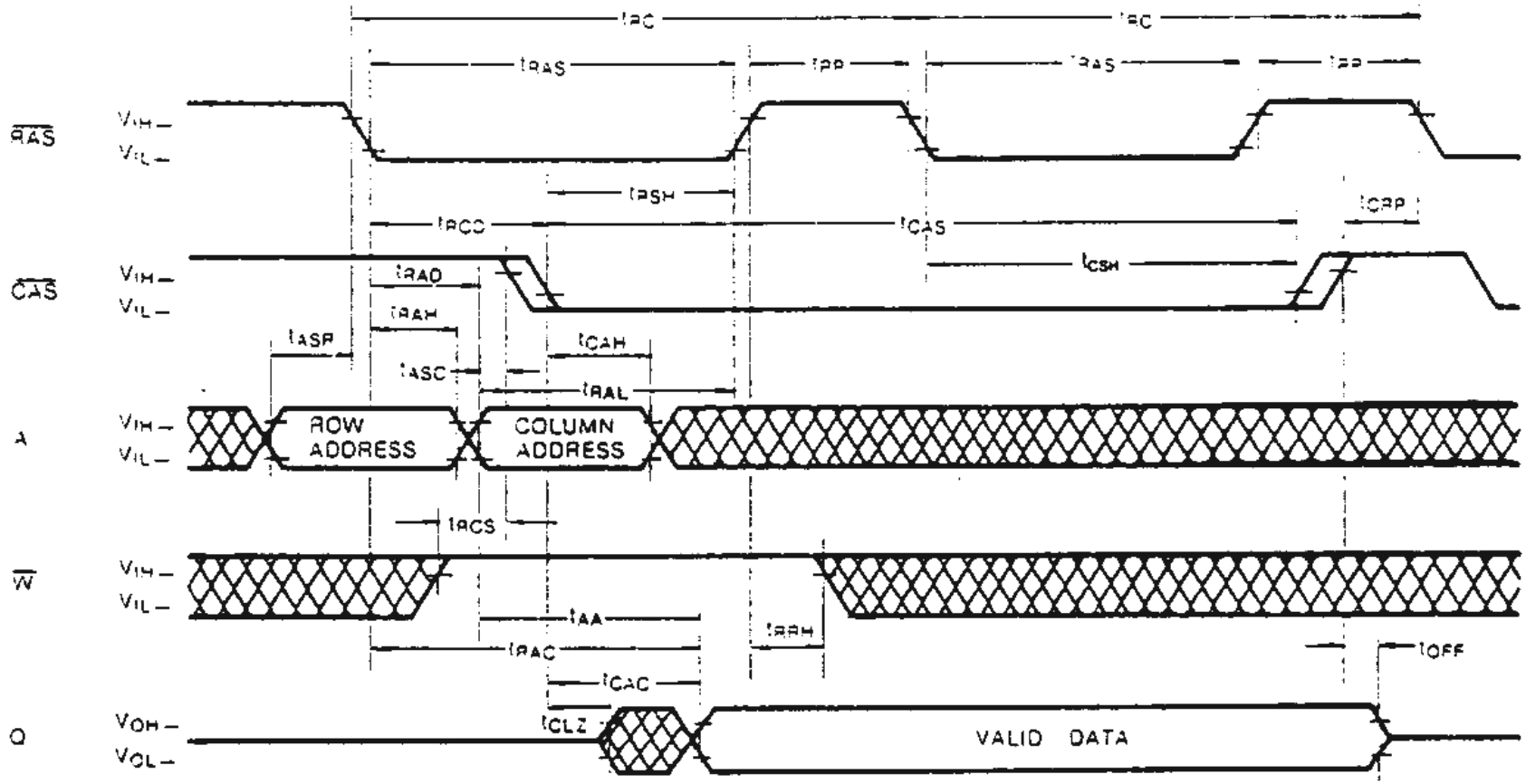
CAS before RAS refresh: if CAS goes low before RAS, then refresh

$\overline{RAS}$-ONLY REFRESH CYCLE

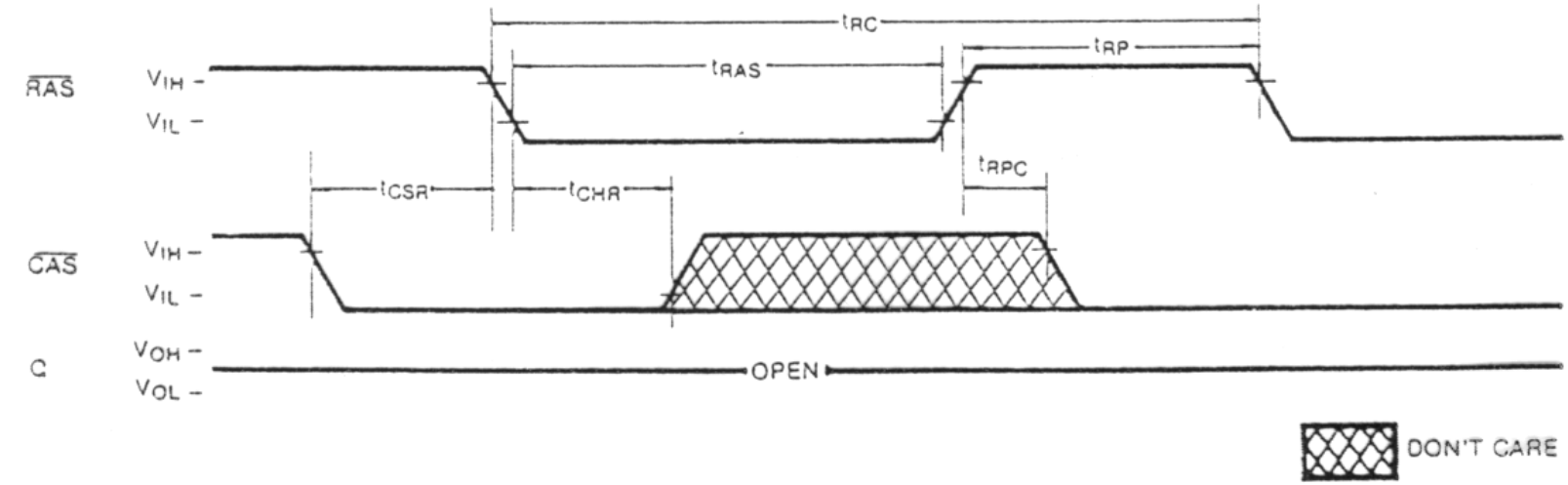
Note: $\overline{CAS}$ = V_{IH}, $\overline{W}$, D, A_9 = Don't Care



HIDDEN REFRESH CYCLE



$\overline{\text{CAS}}$-BEFORE-$\overline{\text{RAS}}$ REFRESH CYCLE



- **DRAM Variations**

Page Mode DRAM:

read/write bit within last accessed row without RAS cycle

RAS, CAS, CAS, . . ., CAS, RAS, CAS, ...

New column address for each CAS cycle

Static Column DRAM:

like page mode, except address bit changes signal new cycles rather than CAS cycling

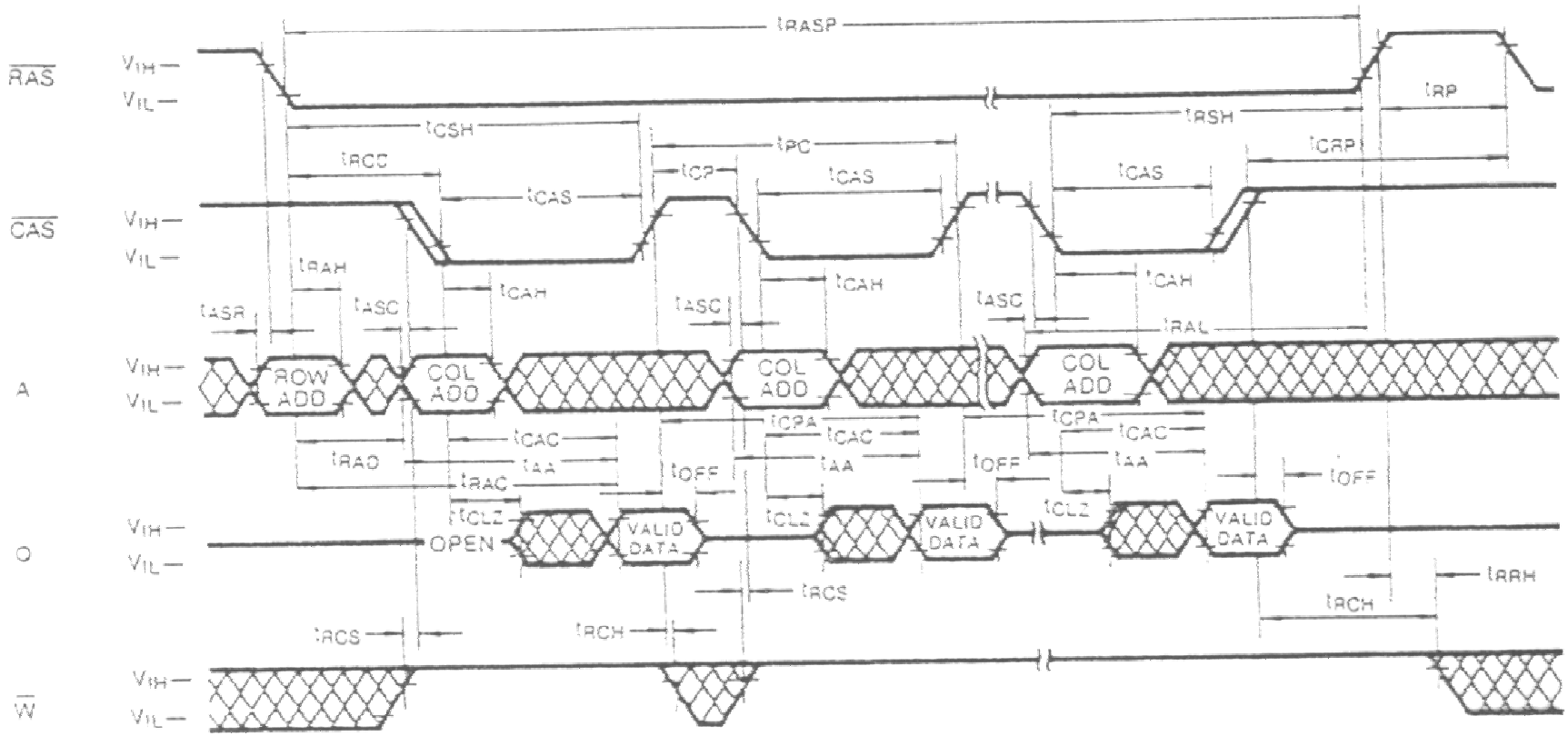
on writes, deselect chip or CAS while address lines are changing

Nibble Mode DRAM:

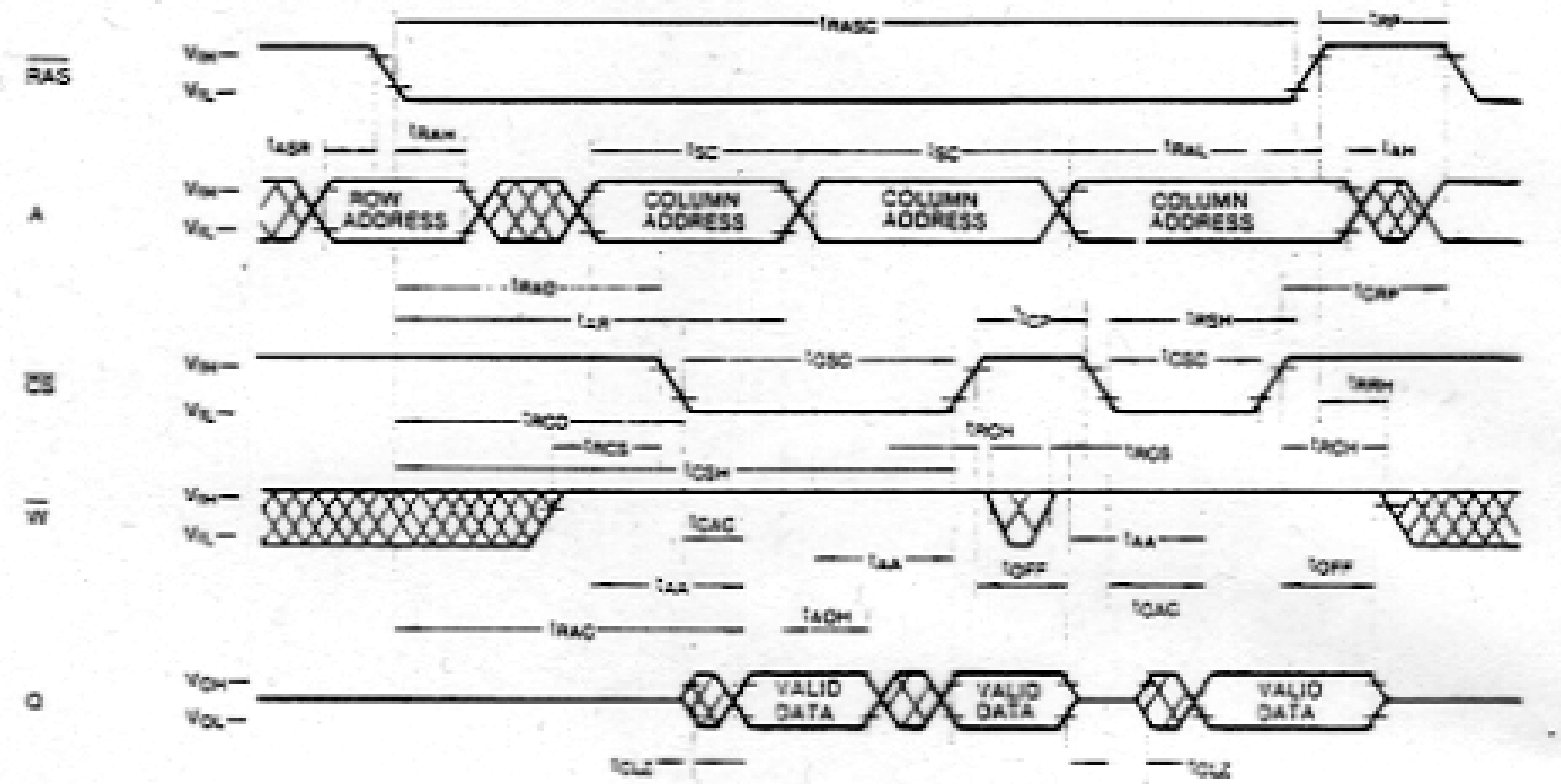
like page mode, except that CAS cycling implies next column address in sequence -- no need to specify column address after first CAS

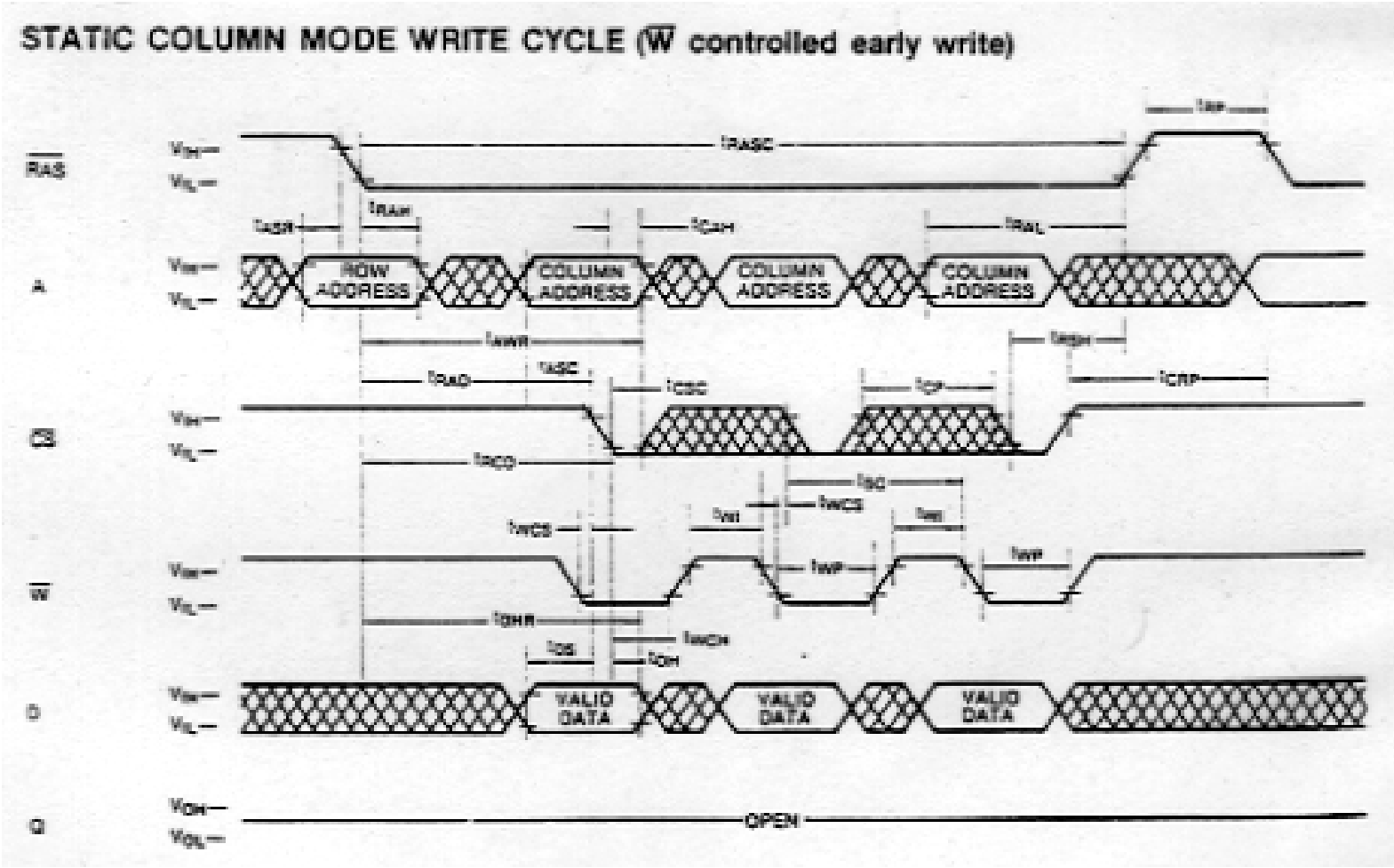
Works for 4 bits at a time (hence "nibble")
RAS, CAS, CAS, CAS, CAS, RAS, CAS, CAS, CAS, CAS, . . .

FAST PAGE MODE READ CYCLE

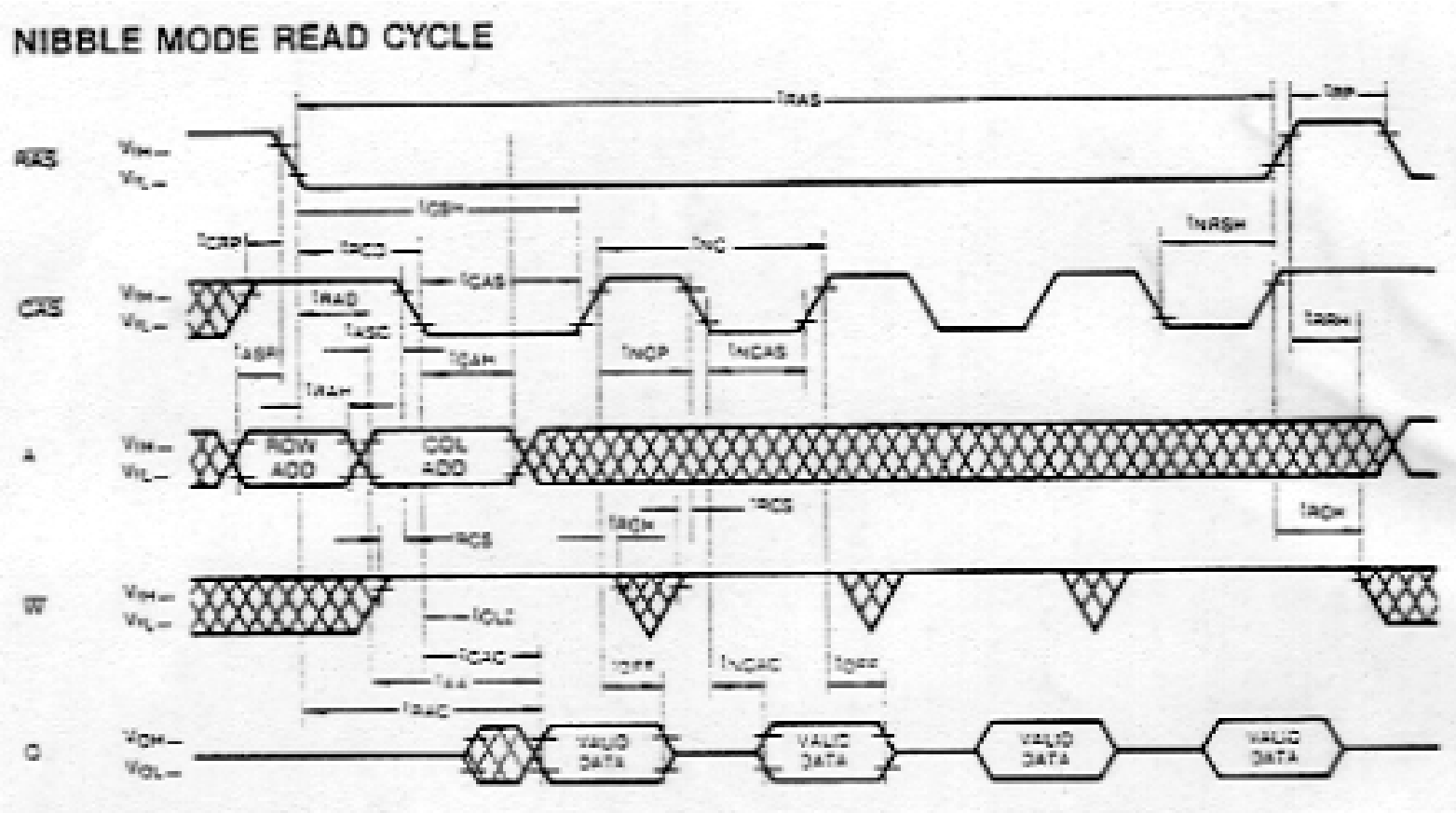


STATIC COLUMN MODE READ CYCLE




STATIC COLUMN MODE WRITE CYCLE (W controlled early write)
RAS
A
CS
W
D
Q
ROW ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
COLUMN ADDRESS
VALID DATA
VALID DATA
VALID DATA
OPEN

NIBBLE MODE READ CYCLE



- **More advanced DRAM Technologies**
  - **EDO DRAM (Extended Data Out DRAM)**
    - **One access to the memory can begin before the last one has finished**
  - **SDRAM (Synchronous DRAM)**
    - **Tied to the system clock and is designed to be able to read or write memory in burst mode (after the initial read or write latency) at 1 clock cycle per access (zero wait states)**
  - **DDR SDRAM (Double Data Rate SDRAM)**
    - **Doubles the bandwidth of the memory by transferring data twice per cycle on both the rising and falling edges of the clock signal**
  - **DRDRAM (Direct Rambus DRAM)**
  - **SLDRAM (Synchronous-Link DRAM)**