Lecture 11:

Si/Poly-Si etch - Reactive Ion Etching -

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RIE Principles (1)

- Reactive Ion Etching ٠
- Process in which chemical etching is accompanied by ionic bombardment
- Combination of physical and chemical etching
- Anisotropic etching



Typical parallel-plate reactive ion etching system



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RIE Principles (2)

\sim	Plasma Etching		Reactive Etching		Physical Etching	
	Barrel Reactor	Planar Reactor	Ion	Ion Beam	Sputtering	Ion Beam Milling
Substrate Location	Surrounded by plasma	On grounded electrode in Plasma	On powered electrode in plasma	In beam, remote from plasma	On powered electrode in plasma	In beam, remote from plasma
Pressure (torr)	10 ⁻¹ ~ 1	10 ⁻¹ ~ 1	10 ⁻² ~ 10 ⁻¹	10 ⁻⁴ ~ 10 ⁻³	10 ⁻⁵ ~ 10 ⁻³	10-4
Ion energy(eV)	Ο	1 ~ 100	100 ~ 1000	100 ~ 1000	100 ~ 1000	100 ~ 1000
Active Species	Atoms. Radicals	Atoms, radicals, reactive ions	Radicals, reactive ions	Reactive ions	Ar+ ions	Ar+ ions
Products	Volatile	Volatile	Volatile	Volatile	Nonvolatile	Nonvolatile
Mechanism	Chemical	Chemical/ Chemical-Physical	Chemical/ Physical	Chemical/ Physical	Physical	Physical
Etch Profile	Isotropic	Isotropic/ Anisotropic	Isotropic/ Anisotropic	Anisotropic	Anisotropic	Anisotropic
Selectivity	30 : 1 - 10 : 1	10 : 1 – 5 : 1	30 : 1 – 5 : 1	10 : 1 – 3 : 1	1:1	1:1
Resist Compatibility	Excellent	Excellent	Good	Good	Poor	Poor
Device Damage	Little	Little	Some possible	Some possible	Very possible	Very possible
Etch Rate (um/min)	0.1 ~ 0.5	0.1 ~ 0.5	0.05 ~ 0.1	0.05 ~ 0.1	0.02 ~ 0.05	0.02 ~ 0.05
Resolution (um/min)	3	2	1 ~ 2	1 ~ 2	0.5 ~ 1	0.5 ~ 1

Ref: J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition



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RIE Principles (3)

• Mechanism of RIE (Reactive Ion Etching)



• Gas type, Chamber pressure, Ion generation influences



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RIE Principles (4)

- Etch performance valuation •
 - Etch rate
 - Anisotropy (define as 1-A/H)
 - Selectivity to mask material
 - Micro-loading effect (RIE lag)
 - Macro-loading effect (dark field or bright field)
 - Etch uniformity
 - Surface quality



5



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RIE Principles (5)

Several RIE system •



CCP: capacitively coupled plasma



ICP: inductively coupled plasma



MERIE: magnetically enhanced RIE



µERIE: microwave electron cyclotron resonance



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Mask Materials for RIE

- Etch mask
 - PR (Photo Resist), Hard mask (SiO₂, Al) is used
 - Selectivity
 - = etch rate of etching material / etch rate of mask
 - Usually, standard PR (for CMOS) is not adequate for O₂ plasma etch → hard mask required
 - Selectivity of silicon: AZ1512
 - Cl based etch (physical etch): <2
 - F based etch (chemical etch): < 10

(if O_2 gas is inserted the chamber the selectivity would be lower than 10)



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7

Reaction in RIE Process (1)

- Reactants
 - Cl-based
 - Sputtering or ion-enhanced etch mechanism
 - High anisotropy
 - Low selectivity
 - Cl₂, BCl₃
 - F-based
 - Chemical etch mechanism
 - High selectivity
 - High etch rate
 - Isotropic etching
 - SF₆



Reaction in RIE Process (2)

• An example of RIE mechanisms (CI based)

Ion and electron formation $e+CI/CI_2 \rightarrow CI^+/CI_2^++2e$ Etchant formation $e+Cl_2 \rightarrow 2Cl+e$

Adsorption of etchant on the substrate $CI/CI_2 \rightarrow Si_{surf}-nCI$ Reaction on surface Si_{surf} -nCl \rightarrow SiCl_{x(ads)}

9

Product desorption SiCl_{x(ads)} $\xrightarrow{(ions)}$ SiCl_{x(gas)}



Reaction in RIE Process (3)

• An example of RIE mechanisms (F based Si etch)





CCP: BCl₃ Recipe and Example (1)

- System: Drytek DRIE-284
- Process parameter ٠

	Step 1		Step 2	Step 3	
Power		200 W	300 W	475 W	
Pressure		20 mTorr	20 mTorr	40 mTorr	
Time		1 min	1 min	10 min	
Cl ₂		0 sccm	2 sccm	50 sccm	
Gas	BCI ₃	14 sccm	14 sccm	5 sccm	
	N ₂	7 sccm	7 sccm	0 sccm	

- Etch rate: 850 nm/min •
- Selectivity: 8.5:1 for oxide hard mask •



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CCP: BCI₃ Recipe and Example (2)

• Fabrication example (proportional amplifier)





CCP: SF₆ Recipe and Example (1)

- System: Drytek DRIE-284
- Process parameter

Power	150 W		
Pressure	150 mTorr		
SF ₆	30 sccm		
O ₂	10 sccm		

- Etch rate: 4.2 um/min
- Selectivity: 14.2:1 for oxide hard mask



CCP: SF₆ Recipe and Example (2)

• Fabrication example (vortex amplifier)





CCP: Poly-Si Etch Test (1)

- System: Drytek DRIE-284
- Process parameter

Power	300 W		
Pressure	75~250 mTorr		
CI ₂	58 sccm		
He ₂	100 sccm		



CCP: Poly-Si Etch Test (2)

• Test results





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ICP Etch System

- Inductive Coupled Plasma etch
- Low pressure: less than 30 mTorr
 → improving ion directionality
- High ion density: more than 10¹¹ cm⁻³





ICP: Poly-Si Etch Recipe of ISRC (1)

- System: STS ICP poly Etcher
- Process parameter

		Step 1	Step 2	
		(native oxide etch)	(poly-Si etch)	
Dowor	Coil	600 W	900 W	
POWer	Platen	100 W	50 W	
Pressure		2 mTorr	2 mTorr	
Time		15 sec	60 sec	
Temperature		20 ^o C	20 °C	
	Cl ₂	20 sccm	0 sccm	
Gas	HBr	0 sccm	20 sccm	
	02	0 sccm	1 sccm	



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ICP: Poly-Si Etch Recipe of ISRC (2)



Line width: 2 um

Line width: 1.5 um

Line width: 0.55 um

- Etch rate of poly-Si: 0.3 um/min
- Selectivity to PR: 3:1
- Selectivity to oxide: 100:1
- Etch profile: 88 ° to 90 °



ICP RIE System in ISRC (1)

- STS ICP poly Etcher (in CMOS area)
- Plasma source type: ICP (inductively coupled plasma)
- Main feed gas : HBr, Cl₂, Ar, SF₆, O₂, He₄
- Main power: 13.56 MHz 1000 W
- Bias power: 13.56 MHz 30/300 W





ICP RIE System in ISRC (2)

- TCP-9600 (in CMOS area)
- LAM Research, USA
- Features
 - Plasma source type: TCP (transformer coupled plasma)
 - Main feed gas: Cl₂, O2, SF₆, He
 - Main power: 13.56 MHz
 - Bias power: 13.56 MHz
- Stand Process Parameter
 - Main feed gas: Cl₂ (100 sccm), O₂ (10 sccm)
 - Main power: 13.56 MHz, 300 W
 - Bias power: 13.56 MHz, 40 W
 - Operating pressure: 5 mTorr



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Various Gas for Poly-Si Etching

Gas	Reactor	Pressure (torr)	Etch Rate	Etch Selectiv	/ity	Comments
CCl₄/Argon	Planar	.4	.02(Undoped)	Poly Si : SiO ₂	15:1	_
SiF₄(50%)/ Argon(50%)	Planar	.2	.4(Undoped)	Poly Si : SiO ₂	25:1	-
CF ₄ /O ₂	Barrel	.2	.05 ~ .1(Undoped)	Poly Si : Si ₃ N ₄ : 25 : 2.5: 1	SiO ₂	-
CF ₄ /O ₂ (4%)	Planar	.4	.057(Phos doped)	Poly Si : SiO ₂	10:1	-
C ₂ CIF ₃	Planar	.225	.05(Phos doped)	Poly Si : SiO ₂	3.5 :1	-
CF ₄ (92%)/O ₂ (8	Dlapar	25	.115(Phos doped)	Poly Si : SiO ₂	10:1	Isotronic
%) Planar	.30	.105(Phos doped)	Poly Si : SiO ₂	9:1		
C ₂ F ₄ (50%)/	Dlanar	Δ	.159(Phos doped)	Poly Si : SiO ₂	8:1	Isotronic
CF ₃ CI(50%)	Plallal	.4	.098(Undoped)	Poly Si : SiO ₂	5:1	rsotropic
C ₂ F ₄ (81%)/	Dlapar	Λ	.082(Phos doped)	Poly Si : SiO ₂	5:1	Anisotropic
CF ₃ CI(19%)	Fialiai	.4	.070(Undoped)	Poly Si : SiO ₂	4:1	Anisotropic
C ₂ F ₄ (92%)/	Dlapar	25	.057(Phos doped)	Poly Si : SiO ₂	6:1	Anisotropia
Cl ₂ (8%)	Pidildi	.30	.050(Undoped)	Poly Si : SiO ₂	5:1	Anisotropic
CF ₃ CI	Planar	.35	.08(Phos doped)	Poly Si : SiO ₂	13:1	Intermediate between
5			.03(Undoped)	Poly SI : SIO_2	6:1	Isotropic and Anisotropic

Ref: J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition



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Deep Reactive Ion Etching (1)

- Uses high density plasma to alternatively etch silicon and deposit etch resistant polymer on sidewall
 - Unconstrained geometry 90° side walls
 - High aspect ratio 1:30
 - Easily masked (PR, SiO₂)
- Bosch process: sidewall passivation → etch → sidewall passivation → etch ...





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Deep Reactive Ion Etching (2)

- Characteristics of the Deep RIE process
 - SF₆ flow: 30 \sim 150 sccm
 - $C_4 F_8$ flow: 20 ~ 100 sccm
 - Etch cycle: $5 \sim 15$ sec
 - Deposition cycle: $5 \sim 12$ sec
 - Pressure: 0.25 ~ 10 Pa
 - Temperature: 20 ~ 80 °C
 - Etch rate: 1.5 ~ 4 um/min
 - Selectivity to resist mask: more than 75:1
 - Selectivity to oxide mask: more than 150:1
 - Sidewall angle: $90^{\circ} \pm 2$
 - Etch depth capability: up to 500 um



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Deep Reactive Ion Etching (3)

• Fence (levee) structure and trench (furrow) structure have different etch side wall profile





Deep Reactive Ion Etching (4)

- Characteristics of Bosch process
 - Scalloping
 - Under cut



Undercut



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Deep RIE Example (1)

Fabrication example (deep trench) ٠



350/m-depth

100µm-depth

80µm-depth, 4.5µm space width, 2µm line width



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Deep RIE Example (2)

Fabrication example (IMU device) •



Gyroscope

Accelerometer (170/Lm-depth)



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RIE Lag in Deep RIE Process

- RIE lag (microloading effect)
 - Etch rate differs from the area of opening



Plasma-Therm, SLR-7701-10R-B data



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Footing in Deep RIE Process (1)

• Footing





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Footing in Deep RIE Process (2)

• Footing formation





Footing in Deep RIE Process (3)

Footing SEM pictures •





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Deep RIE System in ISRC (1)

- ICP deep silicon RIE (in MEMS area)
- Plasma-Therm, SLR-7701-10R-B
- Plasma source type: ICP (inductively coupled plasma)
- High aspect ratio up to 20~30
- Feature
 - 2 kW, ICP source and 500W bias power
 - gas line: C_4F_8 , SF_6 , Ar, O_2 , NF_3 , C_2F_6)

		Deposition	Etch A	Etch B
Time	e (sec)	5	3	5
Gas (sccm)	C_4F_8	70	0.5	0.5
	SF ₆	0.5	50	100
	Ar	30	30	30
Power (W)	RF1 (bias)	1	9	9
	RF2 (source)	825	825	825
Pressur	e (mTorr)	22	23	23





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Deep RIE System in ISRC (2)

- Etch rate: 2.35 um/min
- Under cut at the top of 4 um line & space: 0.41 um
- RIE lag (2 um/4 um): 24 % etch rate difference
- Selectivity to resist mask: 75:1
- Selectivity to oxide mask: 199:1
- Sidewall profile (levee): 88.5 °
- Sidewall profile (furrow): 90 °
- Etch depth capability: up to 500 um



Reference

- 1. K.A. Shaw, Z.L. Zhang, and N.C. MacDonald, "SCREAM I: a single mask, single-crystal silicon, reactive ion etching process for microelectromechanical systems," *Sensors and Actuators A*, vol. 40, pp. 63-70, 1994
- 2. T. Kim, C. Cho, and D. Cho, "A Three-dimensionally siliconmicromachined fluidic device," *IOP J. of Micromechanics and Microengineering*, vol. 8, no. 1, pp. 7-16, March 1998.
- 3. C. Cho, J. Kim, and D. Cho, "A Large-force fluidic device micromachined in silicon," *IOP J. of Micromechanics and Microengineering*, vol. 8, no. 3, pp.195-199, Sept. 1998.
- J.K. Bhadwaj and H. Ashraf, "Advanced silicon etching using high density plasmas," *Proc. SPIE Micromachining and Microfabrication Process Technology*, Oct. 1995, Austin, Texas, vol. 2639, pp. 224-229.
- 5. Matt Wasilik, "Low Frequency Deep Reactive Ion Etching For SOI Processing," Berkeley Sensor & Acutator Center
- Lee, S., Cho, C., Kim, J., Park, S., Yi, S., Kim, J., and Cho, D., "The Effects of Post-deposition Processes on Polysilicon Young's Modulus", *IOP Journal of Micromechanics and Microengineering*, vol. 8, no. 4, pp. 330-337, Dec. 1998



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Reference

- 7. S. Park, "Plasma-Therm Deep Silicon Etcher 공정개발 결 과," Nov. 1999
- 8. Marc J. Madou, "Fundamentals of MICROFABICATION," 2nd edition
- 9. J. D. Lee, "Silicon Integrated Circuit microfabrication technology," 2nd edition

