2.3. CV Characteristics of MOS Devices

Goal;

To understand the capacitance characteristics of MOSFET under the Quasistatic Approximation.

Ref. D.Ward and Dutton

1. "A Charge-Oriented Model for MOS Transistor Capacitances," Journal Solid St. Circuits, vol. SC-13, no.5, pp. - 707, 1978
2. H.Park, et. al, "A Charge-Conserving Non-Quasi static MOSFET model for SPICE transient analysis," IEDM, 1988

A. Intrinsic Capacitance and Extrinsic Capacitance

- MOSFET device is a multiterminal device, and there are charges are present in the device. If charges are stored in the device and the quantities of the charges are changed as the terminal voltages are changed, so the capacitance of the terminal C_{ij} is defined as, $C_{ij} = dQ_i/dV_j$ with other terminal voltage is fixed.

- Fig. 1 shows a schematic picture of the charge distribution in the device. Charges in the dotted area are related with the MOS operation whereas charges outside of the dotted area are unnecessary charges. Capacitances associated with the charges inside the dotted area are called "the intrinsic capacitance" whereas those associated with the parasitic charges are called "the extrinsic capacitances"(or sometimes called "parasitic capacitances").

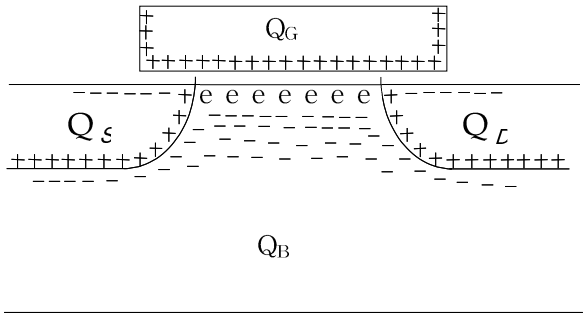

Fig. 1. Intrinsic and Extrinsic charges in NMOSFET when VGS>VT, VG>VD.

– Q_G, Q_S, Q_D and Q_B.

For the modeling purpose, it is convenient to divide the charges in the device and relate the charges with the connected "terminal" as,

Q_G : charges present in the overlap region + intrinsic Q_G,
Q_S : the depletion charge + a part of Q_n,
Q_D : the depletion charge + a part of Q_n,
Q_B : PN junction the depletion charge + Q_d,

and $Q_G + Q_S + Q_D + Q_B = 0$.

B. Bias dependence of capacitance

With Q_i defined, it is rather straightforward to obtain C_{ij}. C_{ij} is dependent on the bias conditions. Only thing which is not clear is Q_n. How do we know, in priori, how much is from "Source" and how much is from "Drain"? Usually, 50:50(or 60:40) is assumed even though more accurate ratio can be found from a device simulation and it depend on the bias condition.

- Gate-Bulk capacitance
- Gate-Drain capacitance
- Drain-Gate, and Source-Gate capacitance

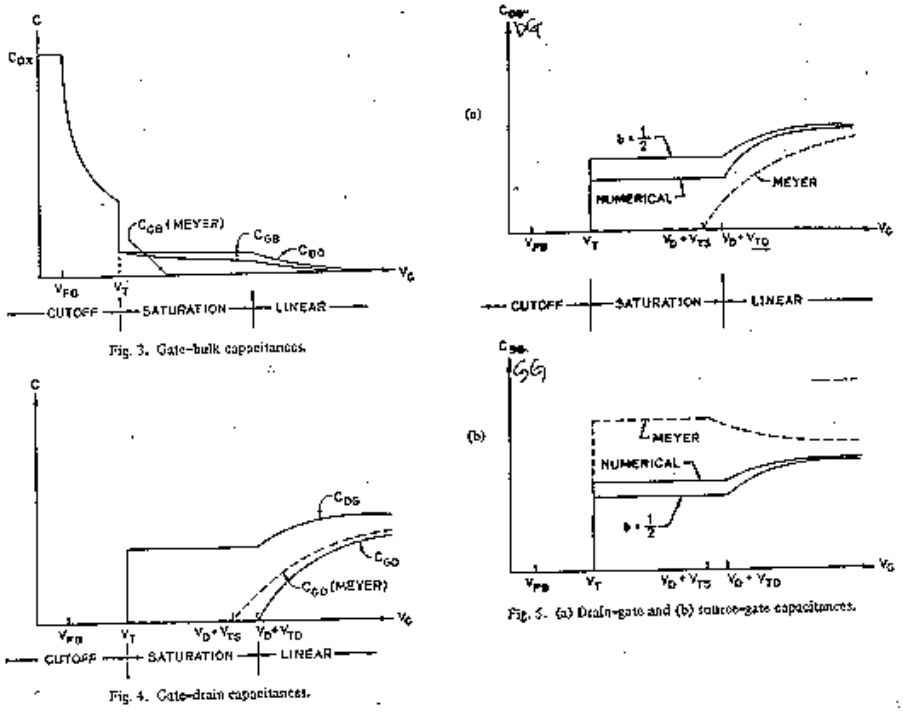

Fig. 3. Gate-bulk capacitances.

Fig. 4. Gate-drain capacitances.

Fig. 5. (a) Drain-gate and (b) source-gate capacitances.

Fig. 2 Figures from the reference 1.

B. Non Quasi static model(NQS):

Quasi static model;

$Q(t_1)$'s are readily known if V(t1)'s are given. That assumes that Q's are only a function of terminal voltages. The model is valid only when charges in the device are "instantaneously" distributed according to the "terminal voltage changes".

However, in the high speed/high resolution MOS A/D converters and low distortion switched capacitor filter (not mention the high speed digital circuits), the "NQS(Non Quasi Static" behavior of the capacitor becomes important. For proper modeling of the NQS effect, the time dependent continuity equations for electrons and holes should be solved to find Q in the device. The one dimensional solution of Q_n in NMOSFET has been proposed in ref. 2. As can be seen from fig.5, the channel charge injection effects are not properly dealt by the QS model.

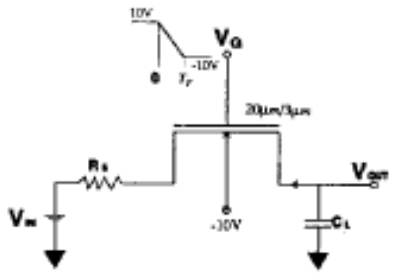

Fig.4. A NMOS switch circuit to investigate the charge injection problem(for Fig.5) Neither overlap capacitance nor junction capacitance is included in the simulation

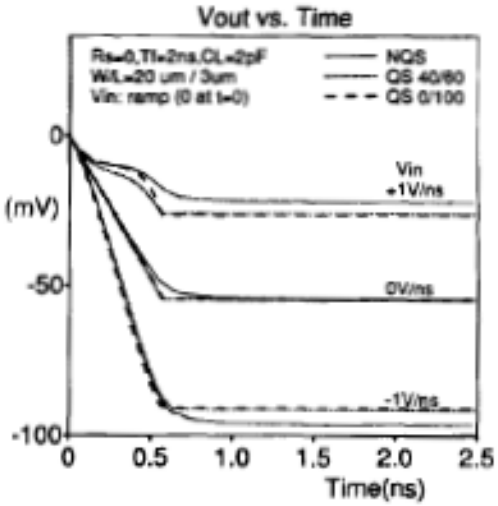

Fig.5. The output voltage waveform of the NMOS switch in Fig.4 with Vin=0 initially and then ramps with rate of +1V/ns, -1V/ns and 0V/ns(DC).

Fig. 4. Fig. 4 and 5 of Ref.2. The drain current does not follow the change in VGS as the function of time.