5.4 MOSFET Mobility(long channel)

Goal;

1)To understand the surface mobility

Ref :

[1] S. Takagi, M. Iwase, and A. Toriumi, "On the universality of inversionlayer mobility in n- and p-channel MOSFETs," in IEDM Tech. Dig., 1988, pp. 398-401.
[2] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A physicallybased mobility model for numerical simulation of nonplanar devices," IEEE Trans. Computer-Aided Design, vol. 7, pp. 1164-1171, 1988.
[3] J. T. Watt and J. D. Plummer, "Universal mobility-field curves for electrons and holes in MOS inversion layers," in VLSI Technol. Tech. Dig., 1987, pp. 81-82.
[4] M. Takayanagi-Takagi and Y. Toyoshima, "Importance of Si-N atomic configuration at the Si/Oxynitride interfaces on the performance of scaled MOSFETs," in IEDM Tech. Dig., 1998, pp. 20.6.1-20.6.4.

1. Universal Relations

– As the vertical field increases as the T_{ox} scales while V_{DD} is not scaled the vertical field increases. The following equations are the Electric field in each section of the device based on the 'classical approximations in the MOS equation'.

$$E_s = -\frac{Q_n + Q_d}{\varepsilon_s}$$

$$= C_{ox}\frac{(V_{GS} - V_T) + \gamma\sqrt{2\Phi_f - V_{sub}}}{\varepsilon_s}$$

$$E_{ox} = E_s\left(\frac{\varepsilon_s}{\varepsilon_{ox}}\right) = \frac{(V_{GS} - V_T) + \gamma\sqrt{2\Phi_f - V_{sub}}}{T_{ox}}$$

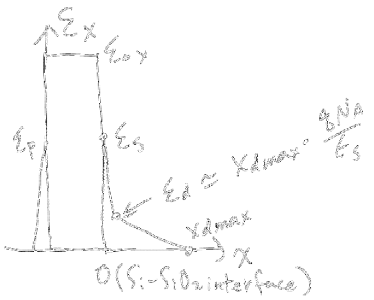


Fig. Sketch of the vertical field in the inversion layer. Eeff,n = (Es + Ed)/2.

It the mobility is plotted vs. the Effective mobility defined as,

$$E_{eff} = \frac{0.5Q_n + Q_d}{\varepsilon_s} \text{ for electrons and}$$

$$E_{eff} = \frac{\frac{1}{3}Q_p + Q_d}{\varepsilon_s} \text{ for holes,}$$

mobilities are on a universal curve. Three definite regions can be noticed in the fig. First region is where the mobility increases with E_{eff}. In the region, the Coulomb scattering with the channel impurity atoms dominates the mobility. As E_{eff} increases, the inversion carriers increase and screen the impurities and reduce the scattering rates. In the 2nd region, the mobility reduces with $E_{eff}^{-1/3}$. Theoretically, the dependence comes from the lattice scattering rates. In the 3rd region, the mobility reduced with E_{eff}^{-2}, which is known due to the surface roughness scattering. As the E_{eff} increases as L is scaled to 0.1㎛ range, the device operates in the "surface roughness" dominant region.

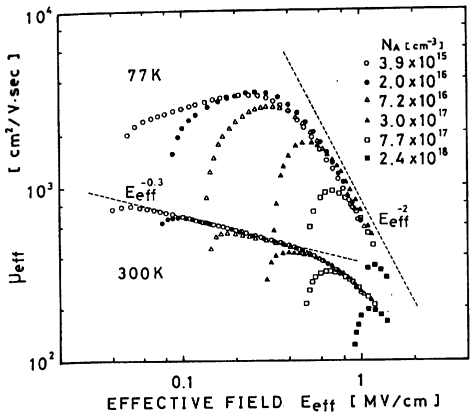


Fig.1 Effective electron mobility μ_{eff} at 300 K and 77 K in n-channel MOSFETs versus effective normal field E_{eff} as a parameter of substrate acceptor concentration. Here, E_{eff} is defined by $E_{eff} = q(Ndpl+Ns/2)/\varepsilon_{Si}$.

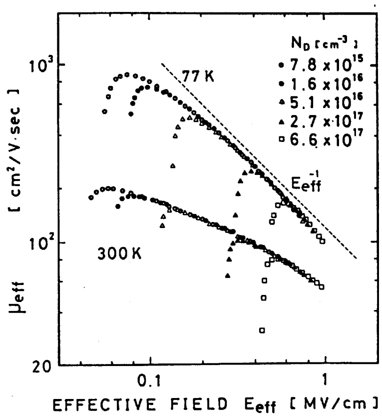


Fig.2 Effective hole mobility μ_{eff} at 300 K and 77 K in p-channel MOSFETs versus effective normal field E_{eff} as a parameter of substrate donor concentration. Here, E_{eff} is defined by $E_{eff} = q(Ndpl+Ns/3)/\varepsilon_{Si}$.

- Mattiesen's law

In the case when there are multiple scattering centers, the total mobility can be written as,

$$1/\mu = 1/\mu_1 + 1/\mu_2 + 1/\mu_3 \ ....$$

In the MOSFET case,

μ_1: Coulomb limited mobility

μ_2: Surface photon mobility

μ_3: Surface roughtness mobility

-Each mobility has differenct functional dependences on TL(lattice temperature), Tn(carrier temperature) and Eeff.

2. Enhancement of Mobility

references

[1] S.-E. Thompson *et al., IEEE Trans.Electron Devices* ***51,*** 1790 (2004).

[2] M. Horstmann, A. Wei, and T. Kammler, in Proc. Intl.

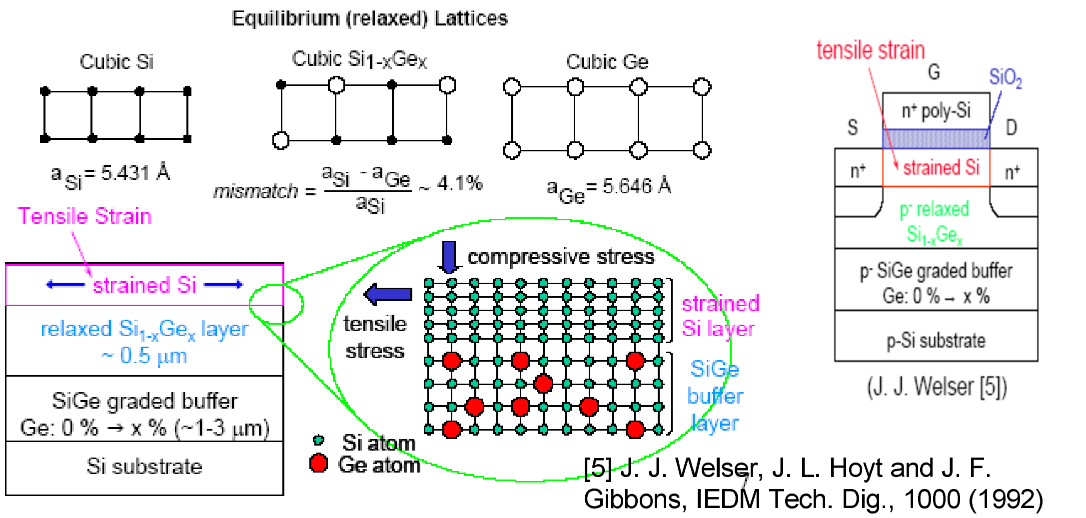
Electron Device Meeting (2005), pp. 233-236.
[3] C.-H. Jan, P. Bai, and J. Choi, in Proc. Intl. Electron Device Meeting (2005), pp. 60-63.
[4] K. Uchida, T. Krishnamohan, K. Saraswat, and Y.Nishis, in Proc. Intl. Electron Device Meeting (2005), pp. 135-138.
[5]For modeling of the mobility enhancement for NMOSFET, for example, E. Ungersboeck,, et.al, Electron Inversion Layer Mobility Enhancement by Uniaxial Stress on (001) and (110) Oriented MOSFETs, SISPAD, 06
from ref. 5 above

B-1. By way of strained layer

Mobility enhancement(from Tagaki, IEDM short lecture , 2003)

- Using the strained layer to decrease the effective mobility

Using the strained layer to change the effective mass.



B-2. By way of stress from the source/drain

E. Energy band due to the strain in the silicon

— Band structure is modified due to the deformation of the regular crystal structure in silicon.

Typical example of the local deformation of the energy band structure caused by the lattice vibrations(optical phonon and acoustic phonon).

ref)

- Efforts to use the strain to modify the energy band shape have been made for a long time to enhance the mobility of carriers.

There have been two approaches: Using the epi layer such as Si1-x Gex as the relaxed layer to give the strained Silicon grown on top of the relaxed layer.

ref.) J. Welser, et. al, IEDM, Tech. Dig. 1000(2002)

- Another efforts is to use the silicon nitride film to give the stress from the side wall for NMOS and Silicon Germanium implantation to the source/drain regions.

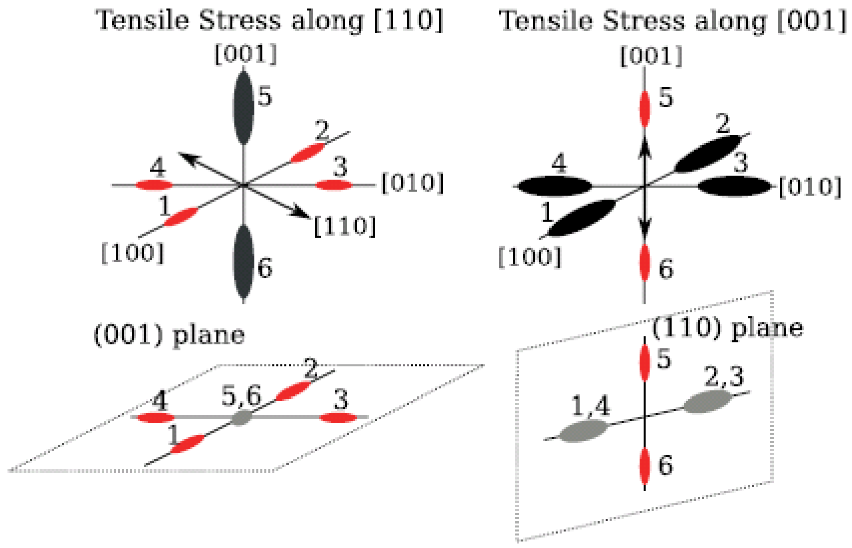


Figure 1: Constant energy surfaces of the Si conduction band under uniaxial tensile stress along [110] / [001] with projection on the (001) / (110) plane.

- effects of strain on the performance of PMOS and NMOSFET
Y. Luo, 'Enhancement of CMOS Performance by Process-Induced Stress'
IEEE, TED, VOL. 18, NO. 1, FEBRUARY 2005 63

- From the figures below, it can be seen that (From Ref. [1] above), the stress is given from the film deposited on the sidewall, or the $Si_{1-x}Ge_x$ film on the source and drain regions to give a stress to the channel.

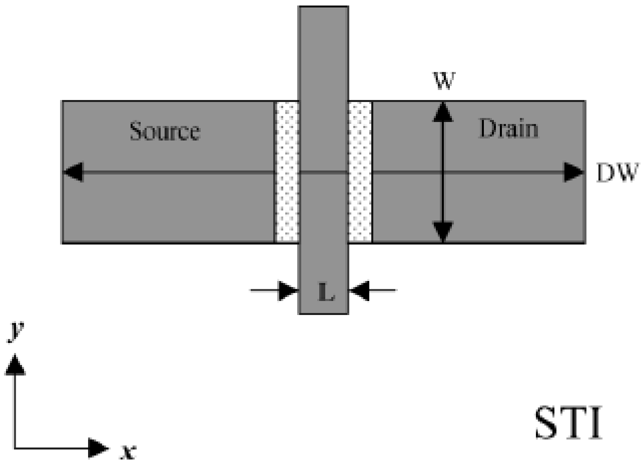


Fig. 1. Schematic of MOSFET for study, showing the three main parameters: channel length L, channel width W, and diffusion width DW. Stress components x, y are along L (DW) and W, respectively.

TABLE I
IMPACT OF STRESS COMPONENTS ON MOSFET PERFORMANCE

	axis	*NMOS*	*PMOS*
Tensile stress	*x*	↑	↓
	y	↑	↑
Compressive stress	*x*	↓	↑
	y	↓	↓

↑ - enhancement; ↓ - degradation