MOSFET, NMOS and CMOS logic
4190.309
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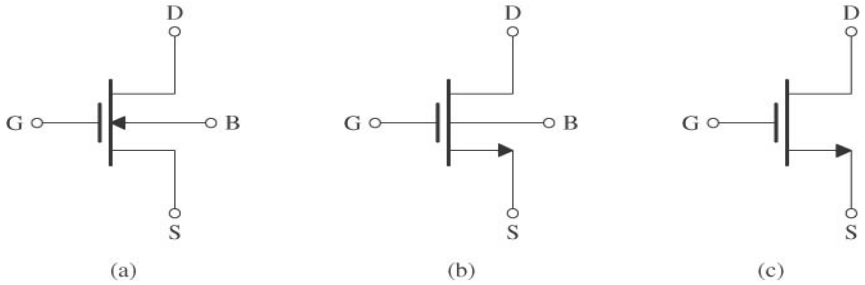
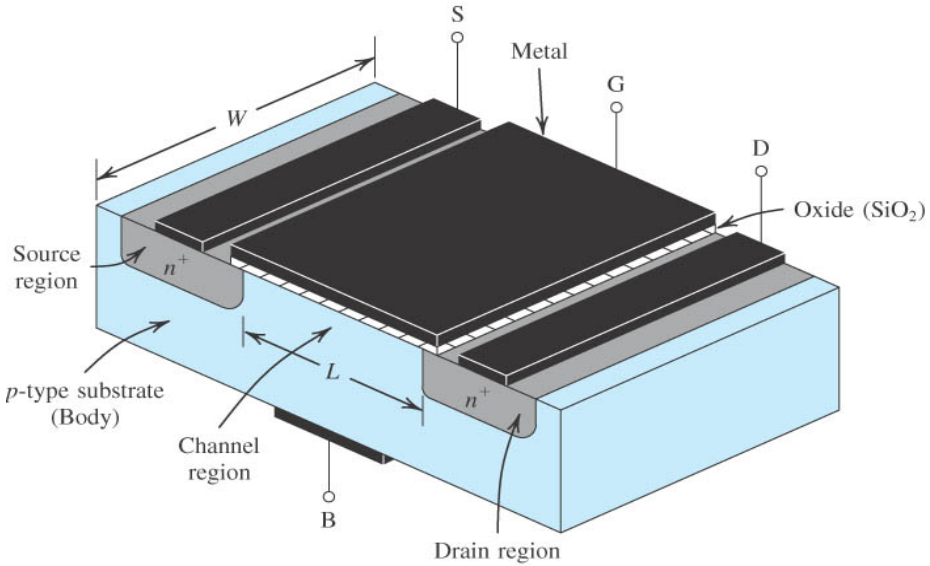
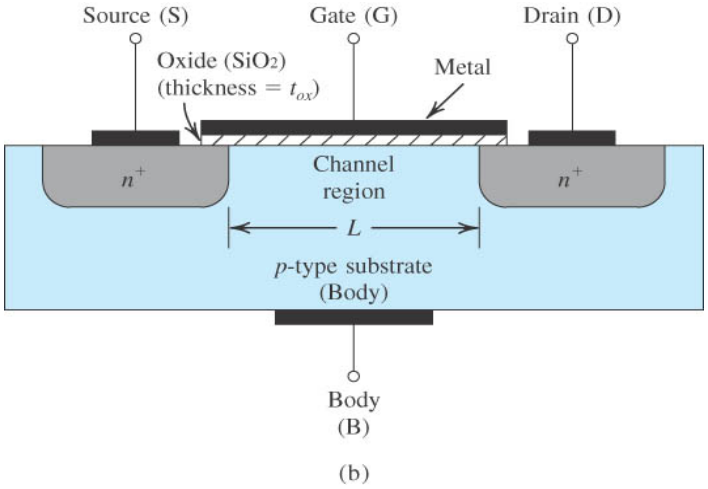
MOSFET structure

- Source, drain and gate
- Channel length and width

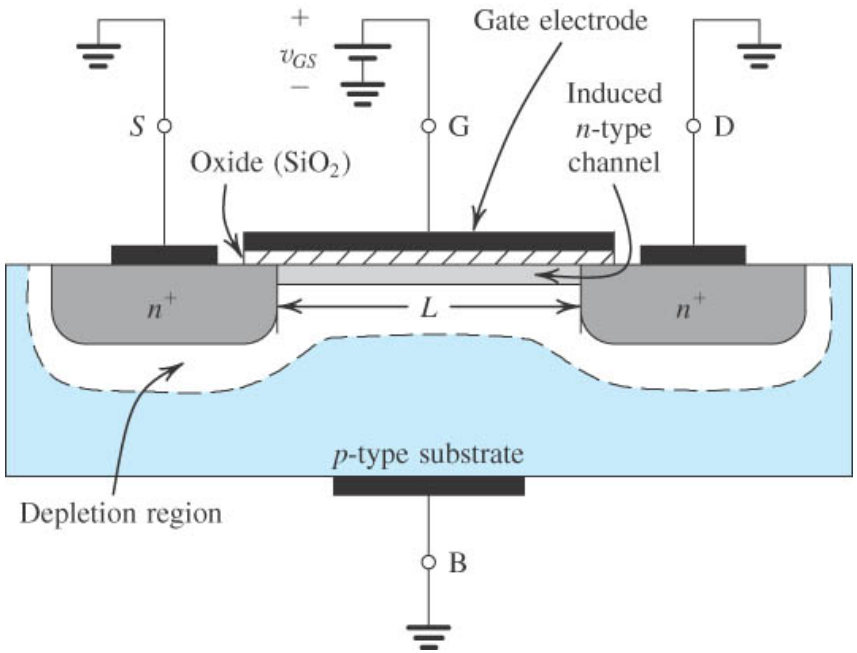






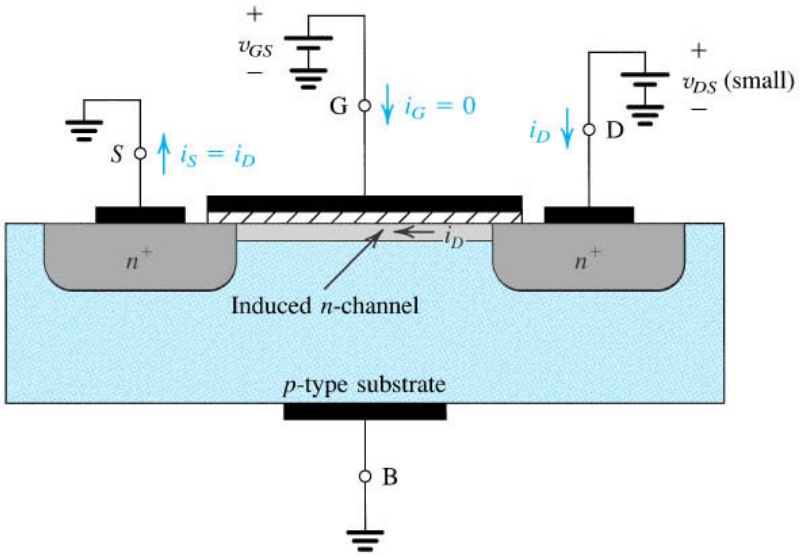
N-channel enhancement MOSFET

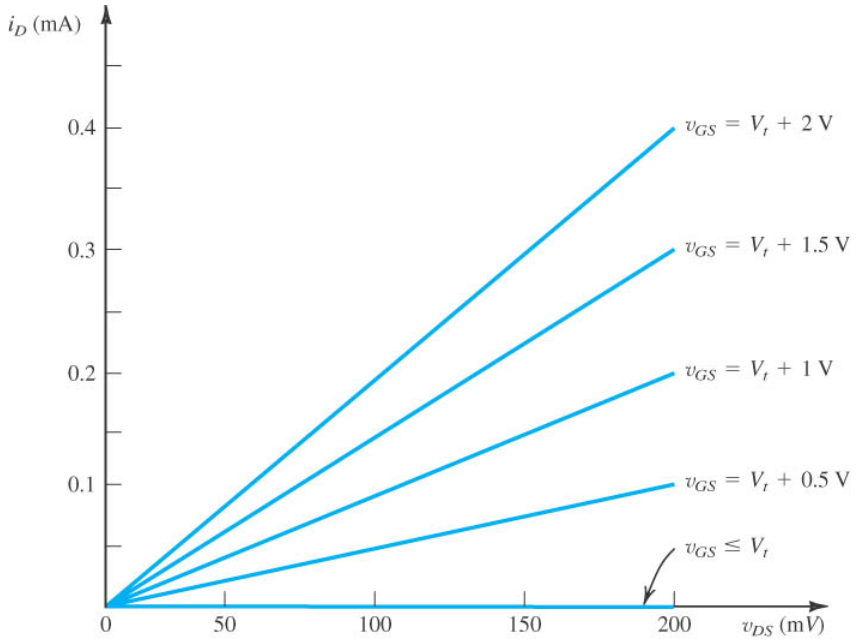
- The enhancement-type NMOS transistor with a positive voltage applied to the gate
- An n channel is induced at the top of the substrate beneath the gate



N-channel enhancement operation

- An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied.
- The device acts as a resistance whose value is determined by v_{GS}
- The channel conductance is proportional to $v_{GS} - V_t'$ and thus iD is proportional to $(v_{GS} - V_t)\, v_{DS}$





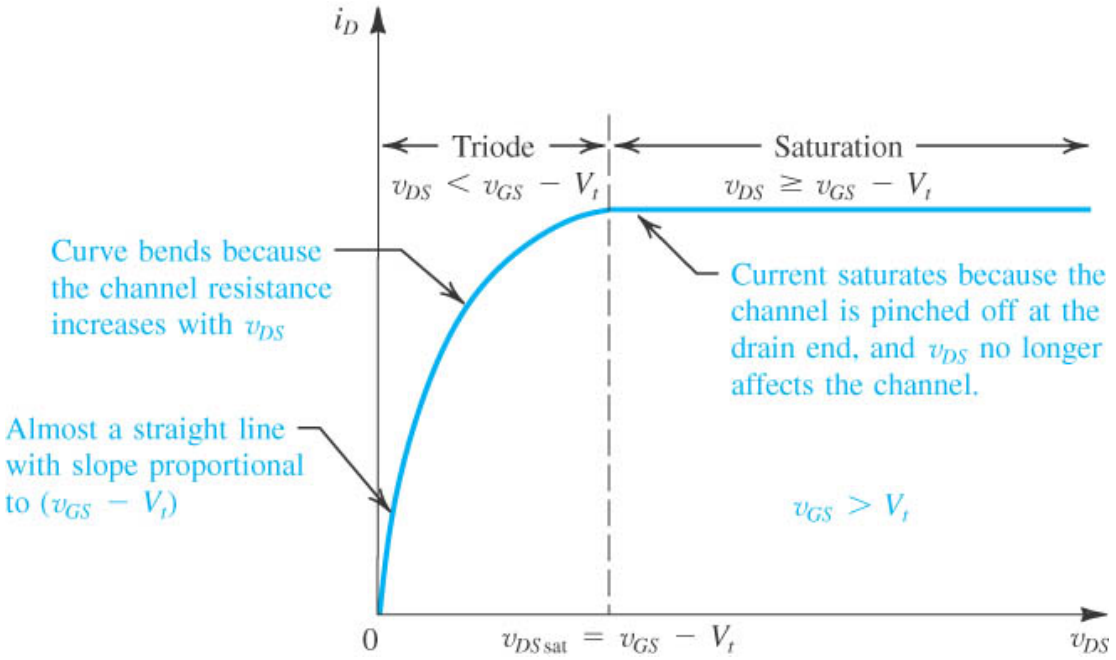
Triode and saturation modes

- Triode region:

$$i_D = k_n \frac{W}{L}\left((v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right)$$

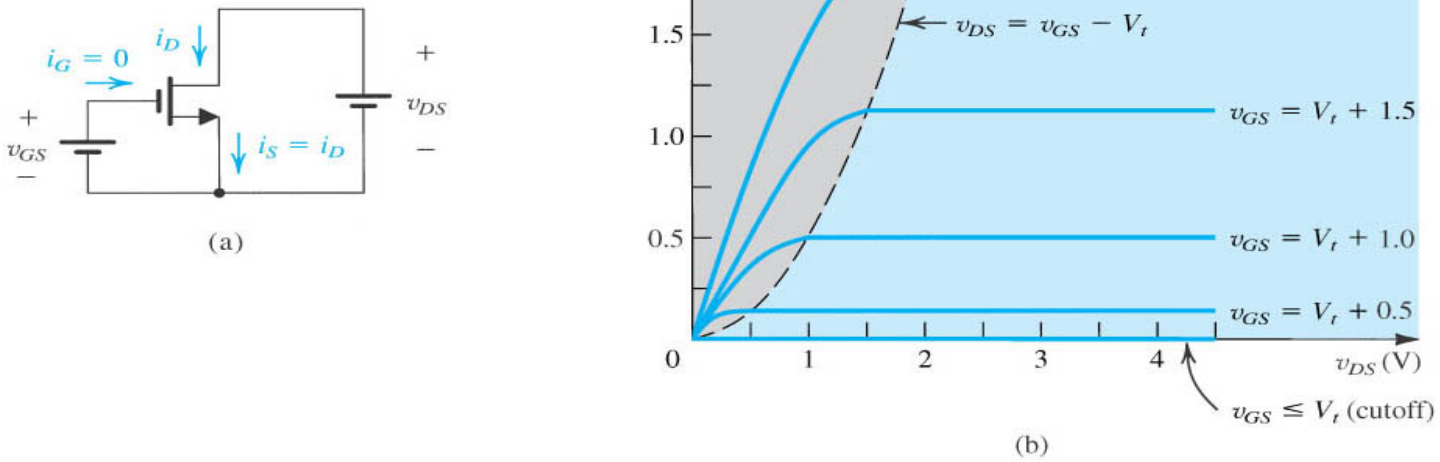
- Saturation region:

$$i_D = k_n \frac{W}{L}(v_{GS} - V_t)^2$$



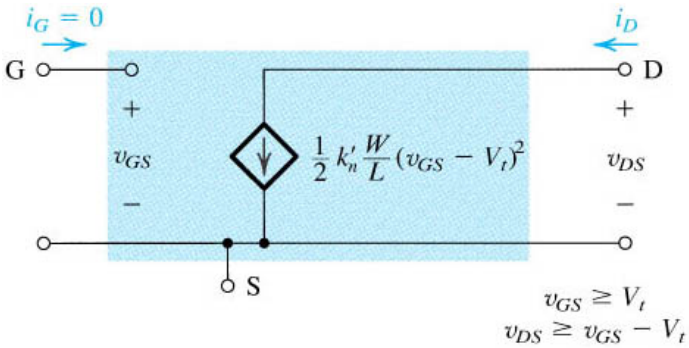
MOSFET characteristics

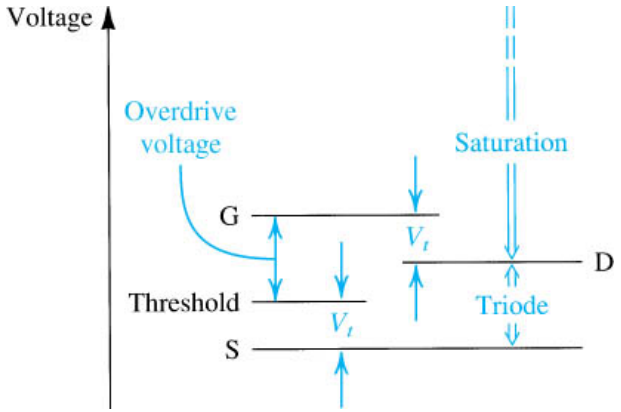
- The i_D–v_{DS} characteristics for a device with k'_n (W/L) = 1.0 mA/V^2

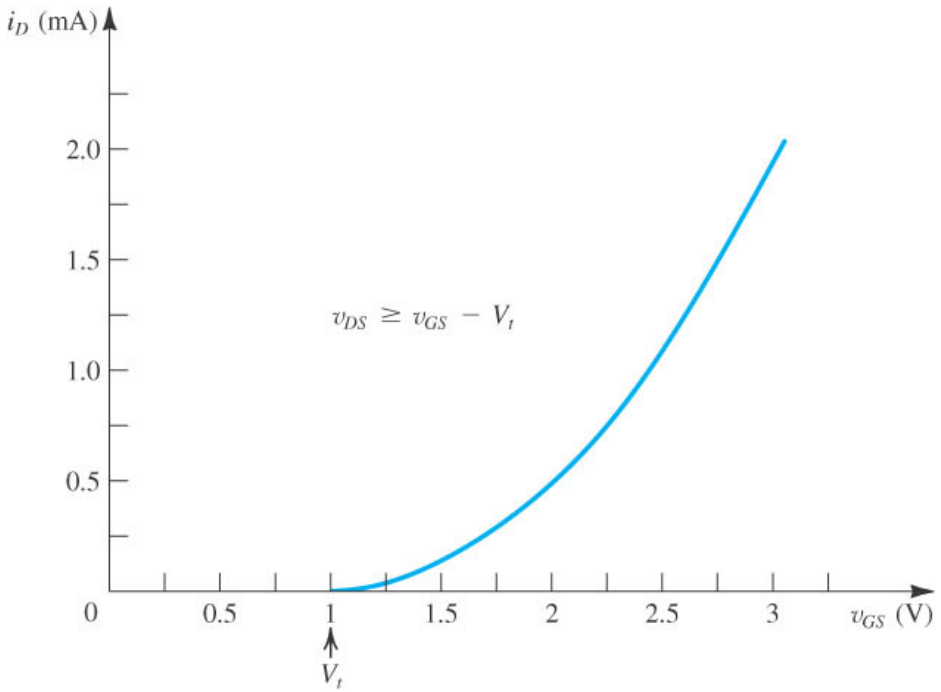


MOSFET characteristics

- Large signal equivalent circuit

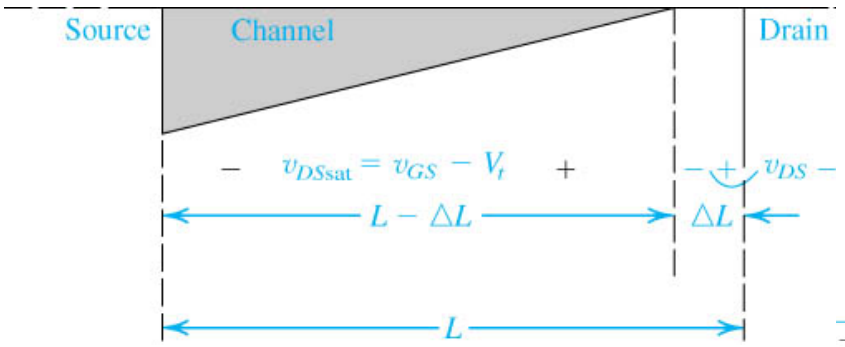


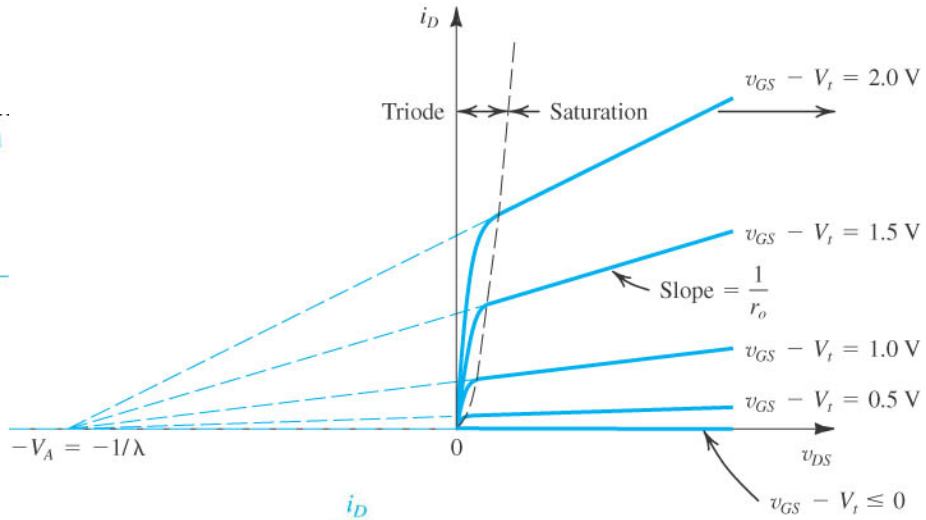


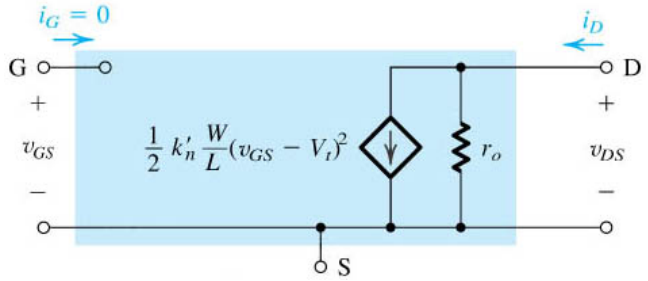


Channel-length modulation

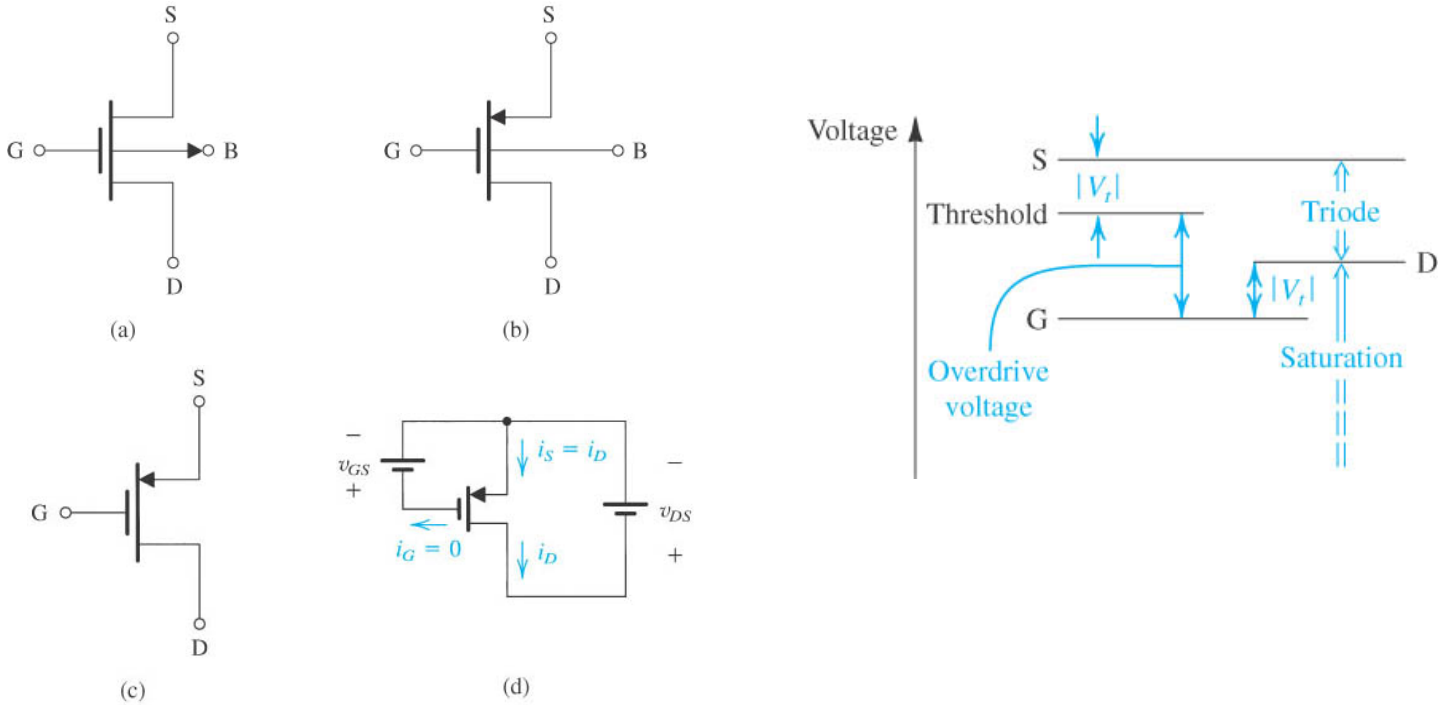
- Finite output resistance in saturation
  - Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by DL).





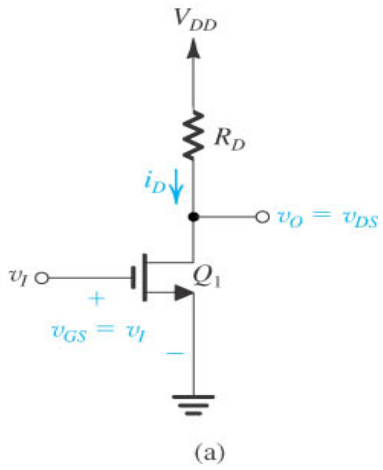


P-channel MOSFET

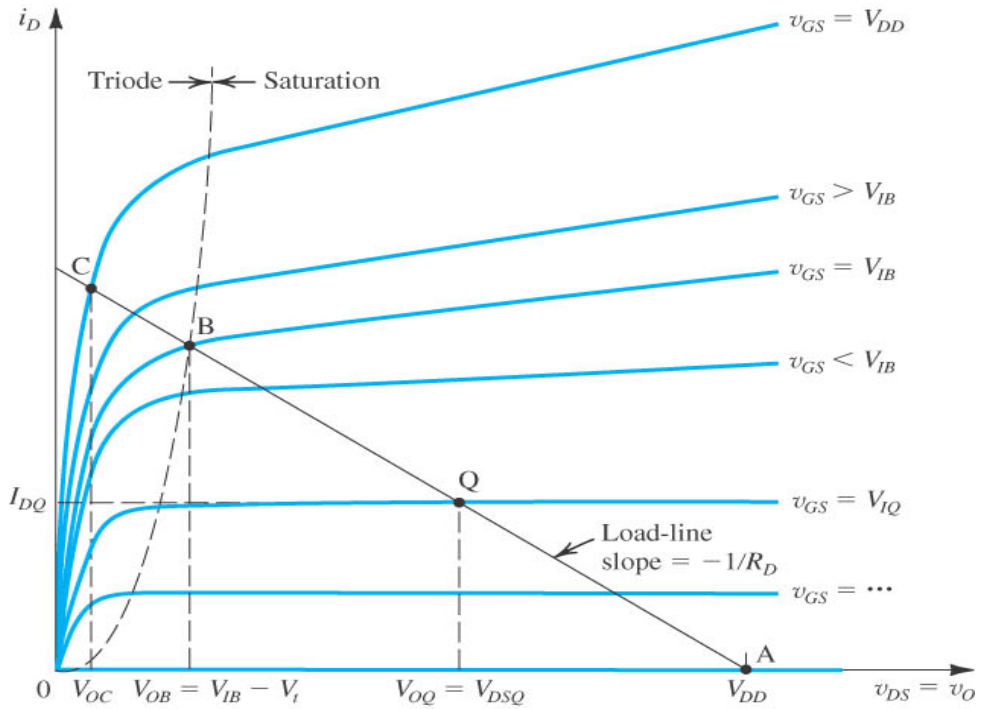


Large-scale operation

- Common-source circuit

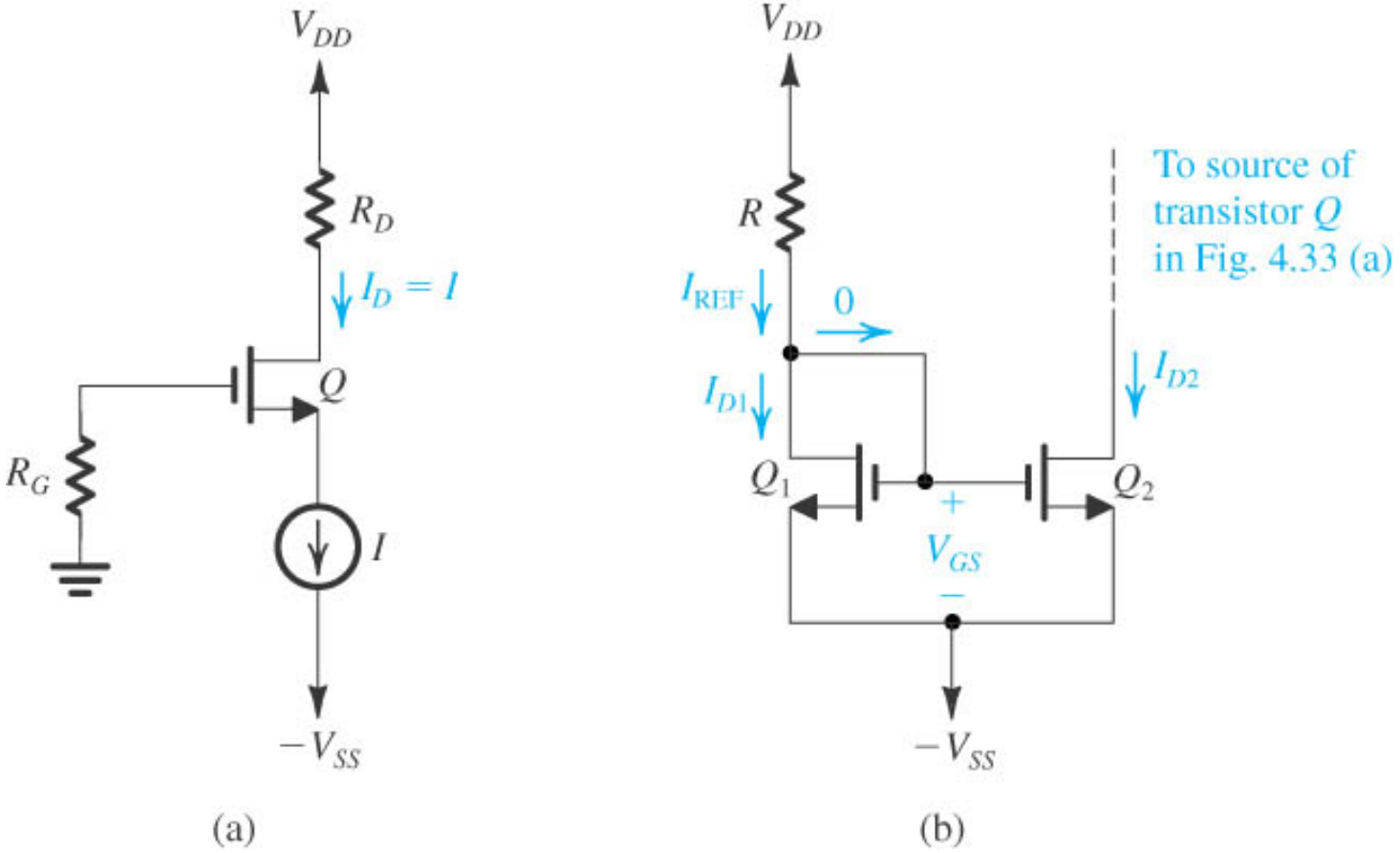


(a)

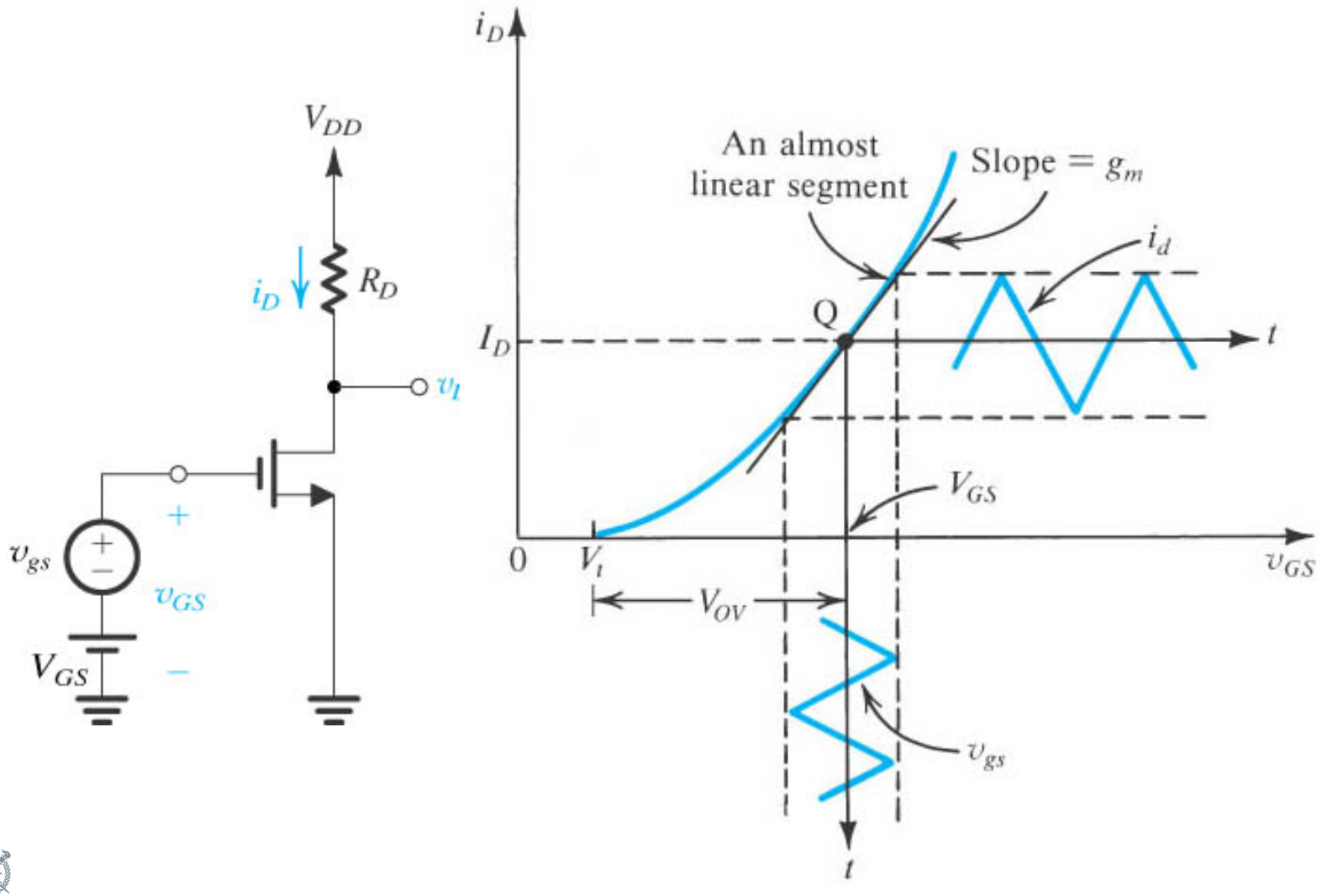


(b)

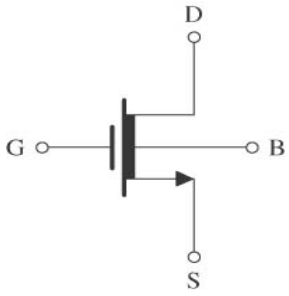
MOS current mirror

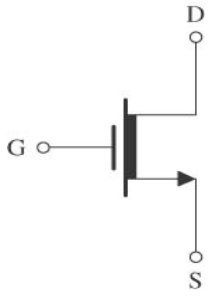


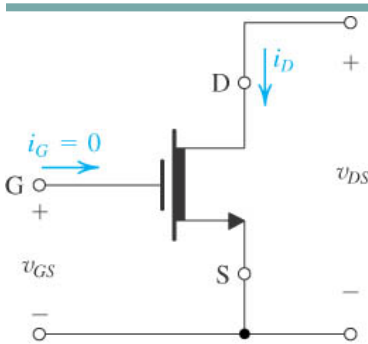
MOSFET amplifier



Depletion MOSFET







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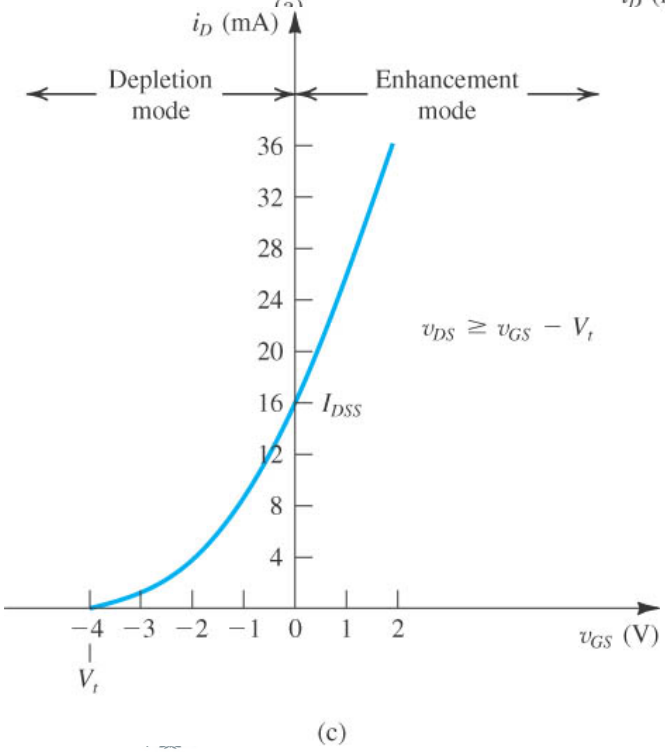

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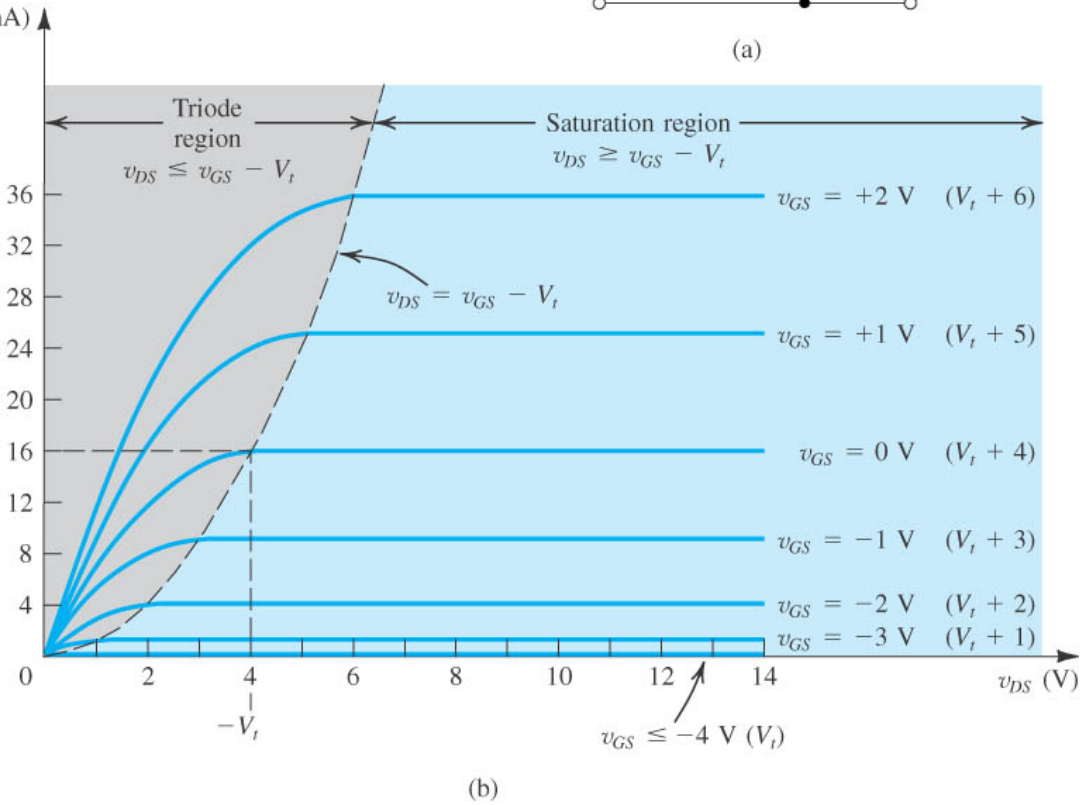

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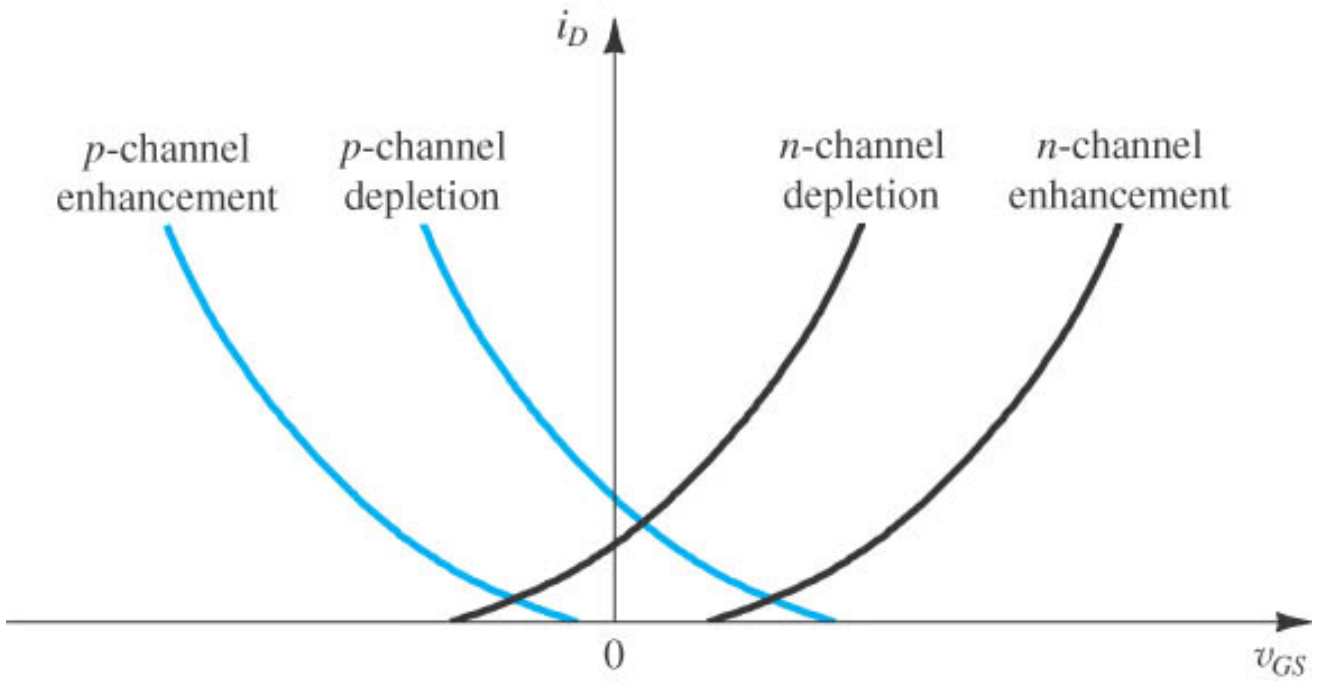
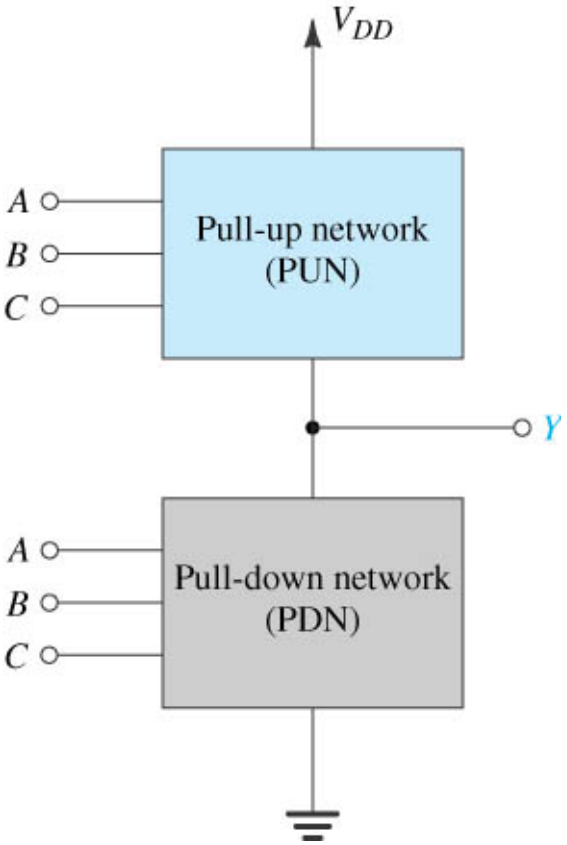
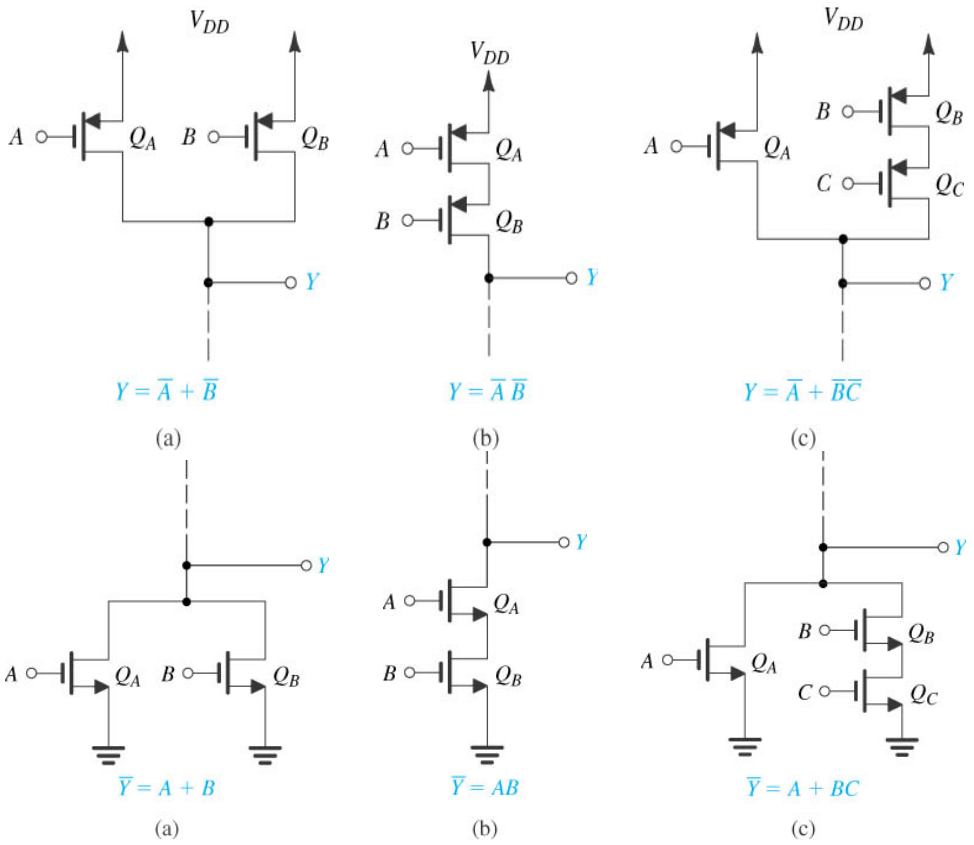
Depletion MOSFET



MOS digital logics

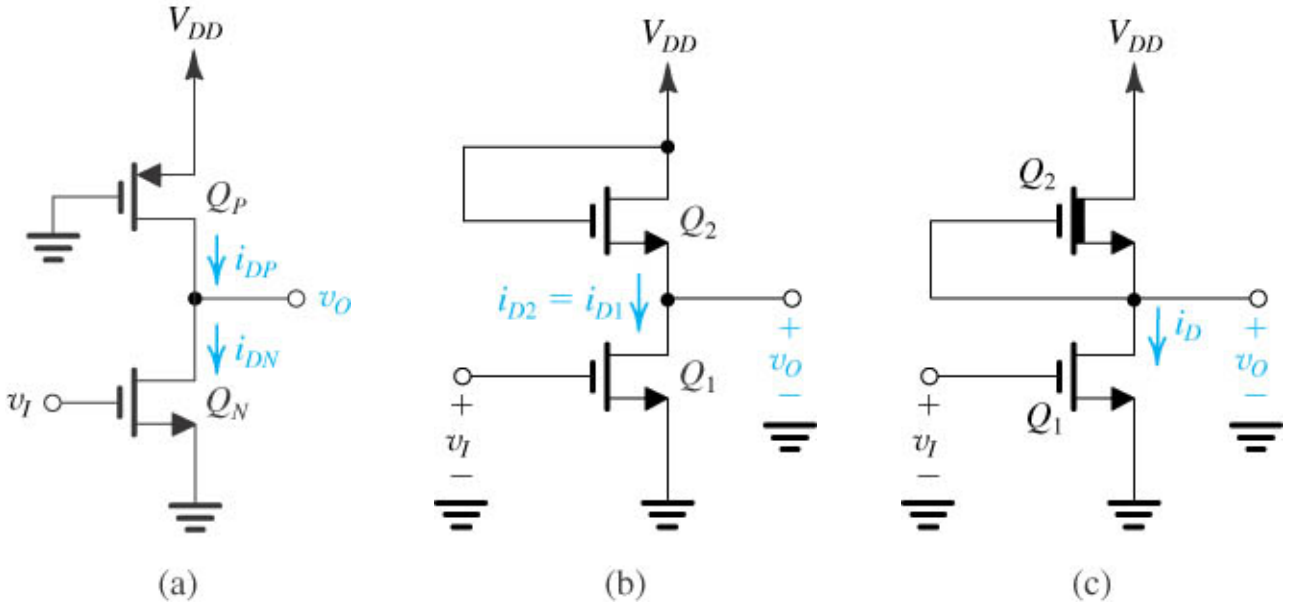
- Pull-up and pull-down networks





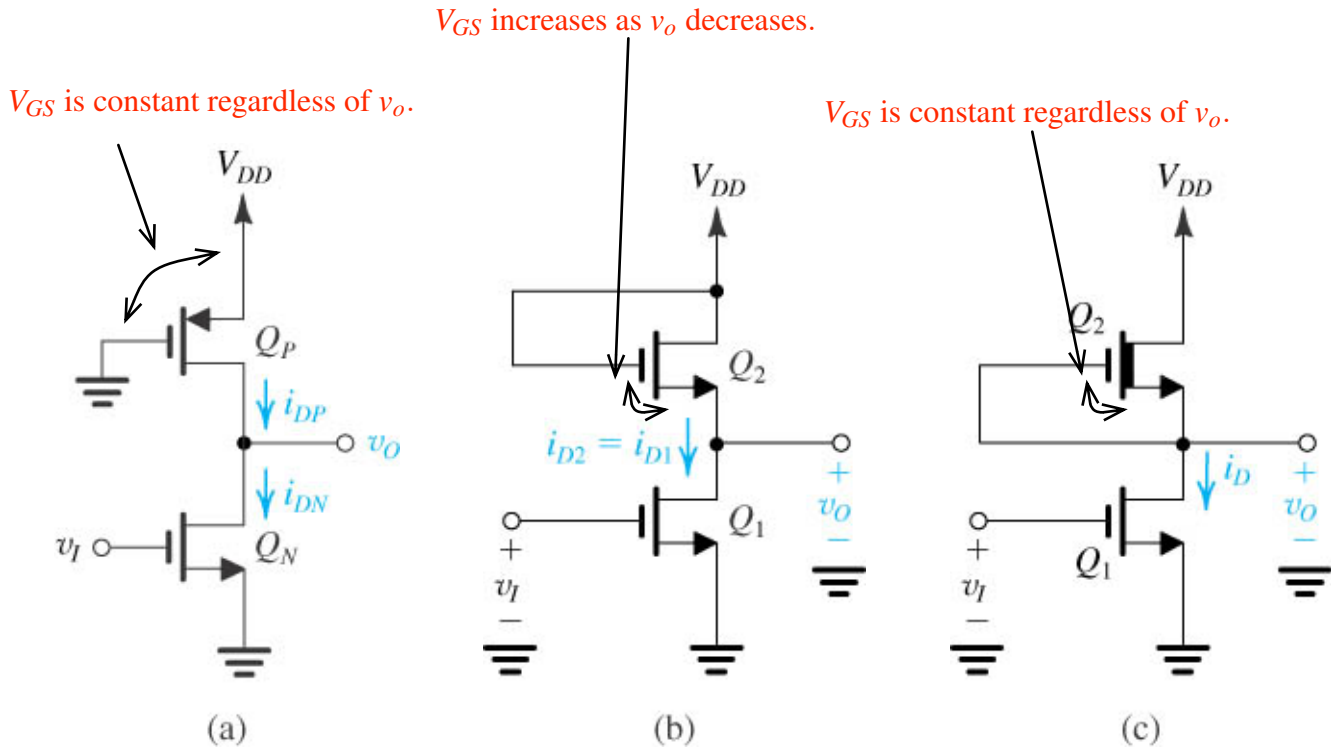
MOS digital logics

- Implementation of pull-up and pull-down networks
  - Pseudo NMOS
  - Enhanced-mode NMOS
  - Depletion-mode NMOS



How the static current varies

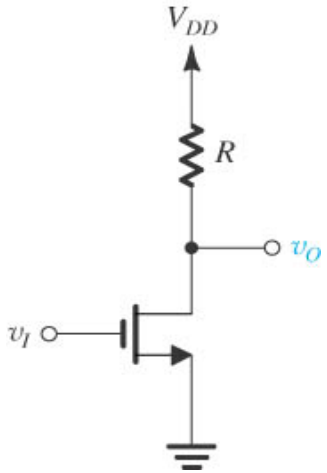
- Static current characteristics

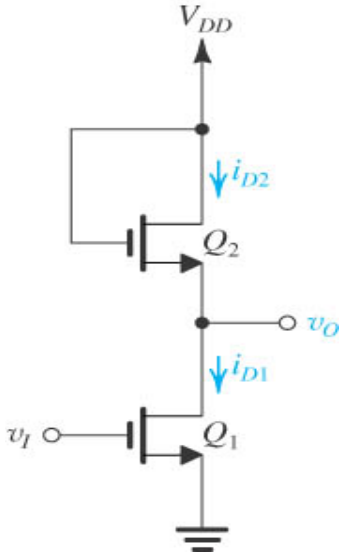


Large static current!

Enhanced-mode NMOS inverter

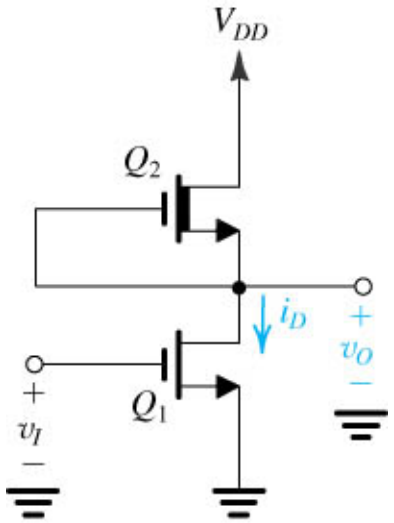
- Simple and old configuration
  - Relatively small logic swing
  - Small noise margin
  - High static power
  - Now virtually obsolete





Depletion-mode NMOS

- Initially operates like a constant-current source
  - Ideal VI characteristics
  - Quickly deviates from the constant-current source but a lot better than the enhanced-mode NMOS
  - Needs extra processing (ion-implanting channel)



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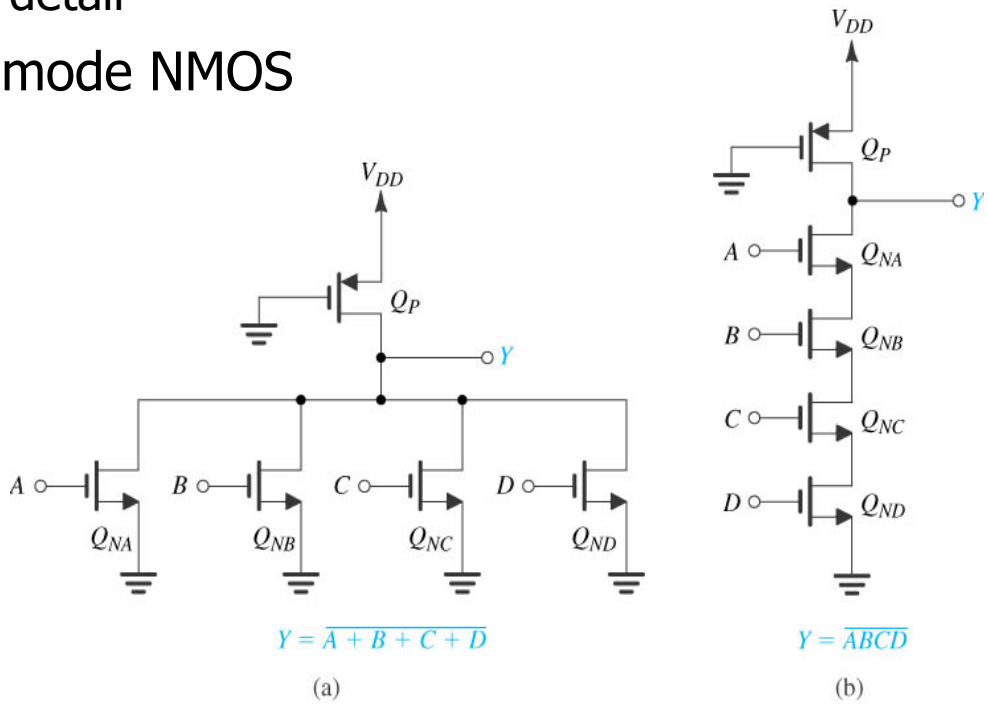
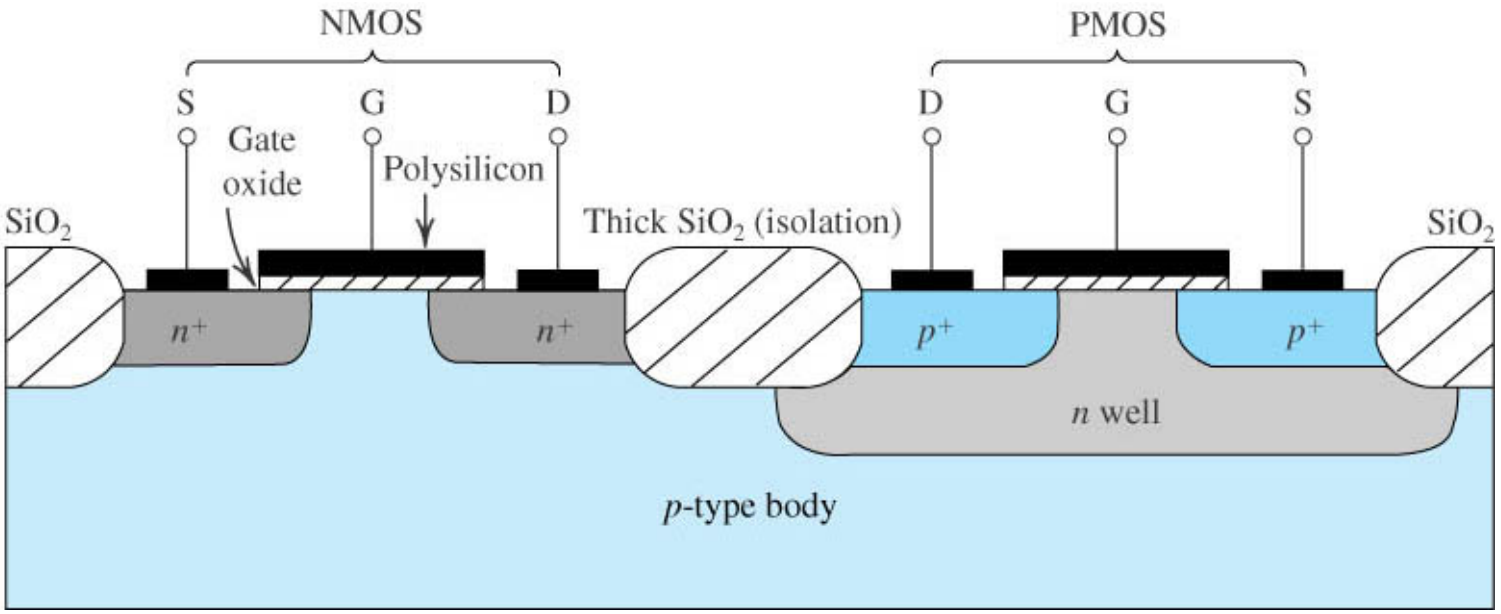
Pseudo NMOS

- CMOS shows excellent characteristics
  - But involves significant area overhead
  - Transistor sizing
  - Talk to you later in detail
- Similar to depletion-mode NMOS
  - But slightly better



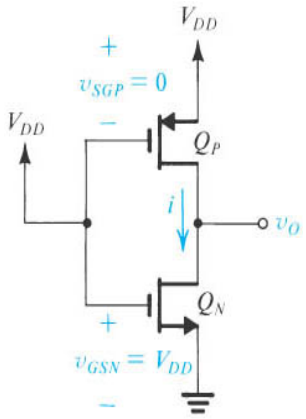
CMOS digital logic

- Structure of a CMOS



CMOS digital logic

- Principle of operation



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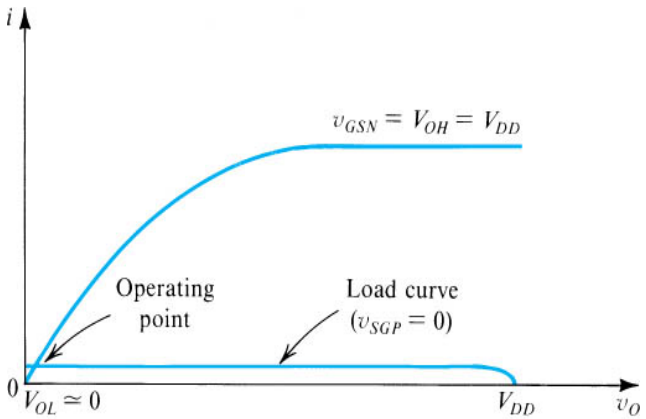

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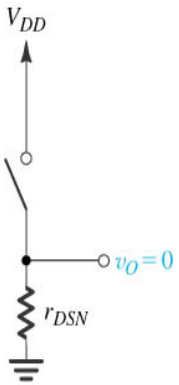

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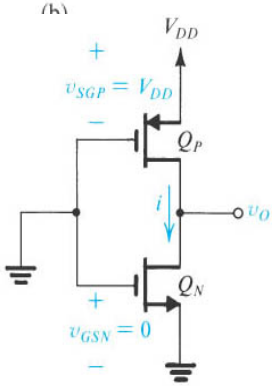

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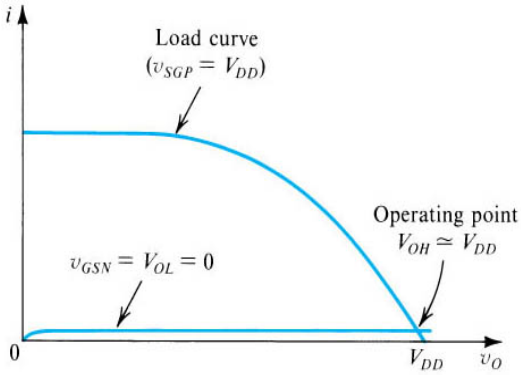

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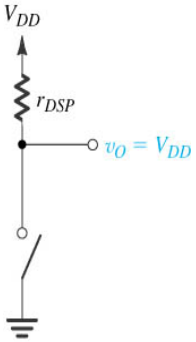

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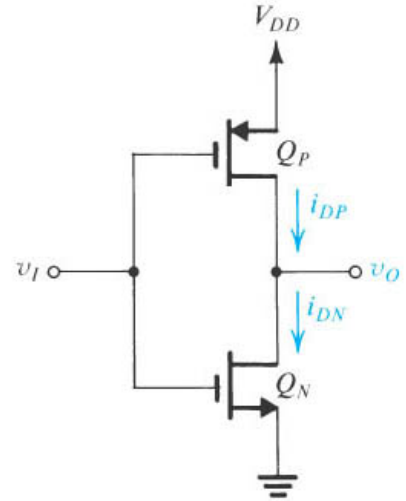
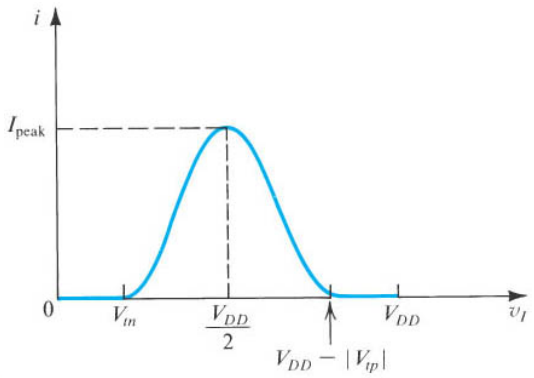
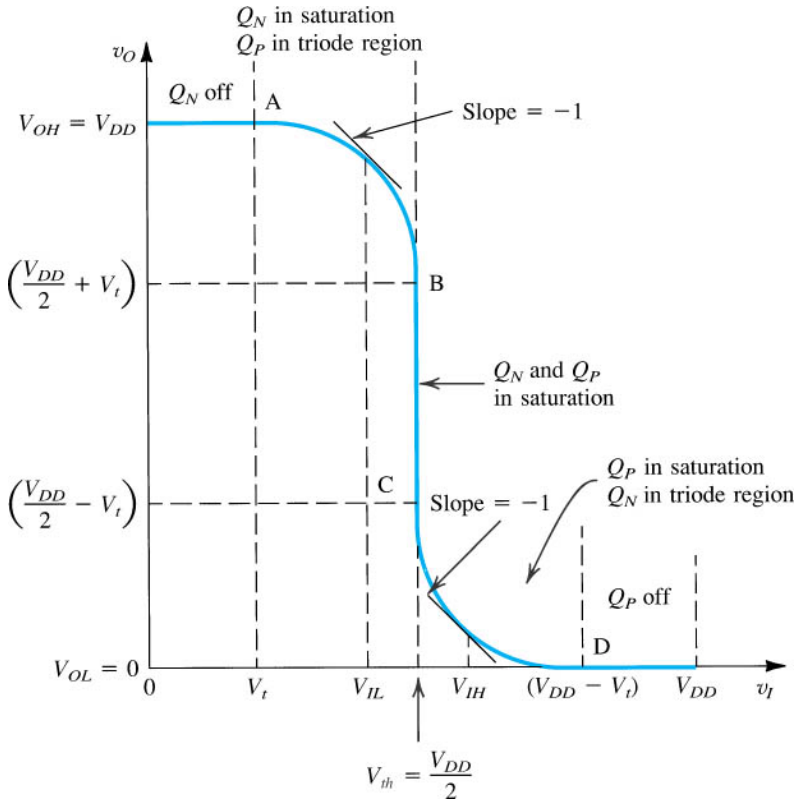
CMOS digital logic

- VI characteristics

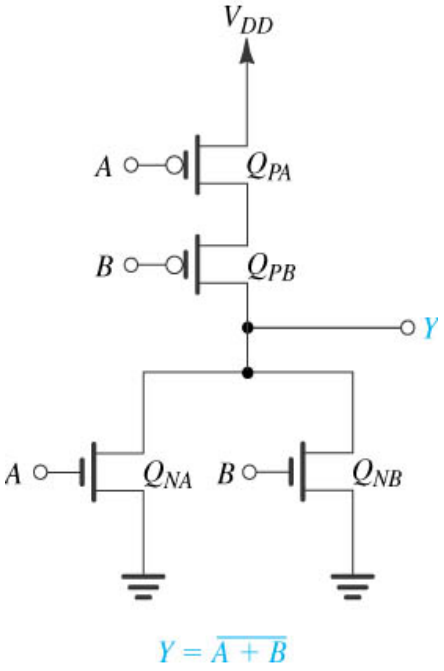


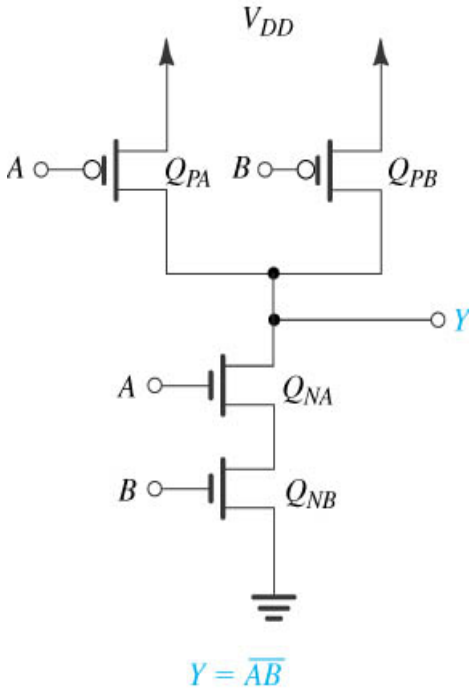


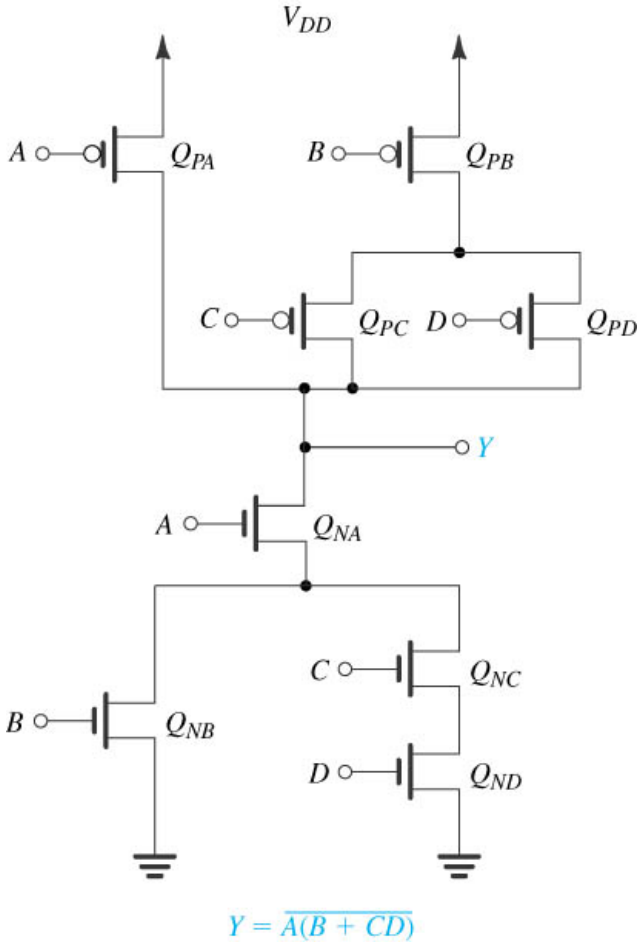


CMOS logic gates

- Pull-down and pull-up networks

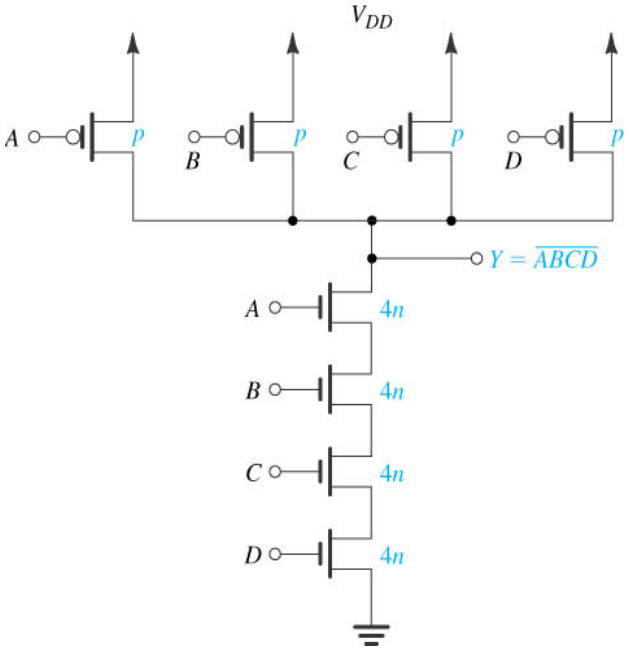


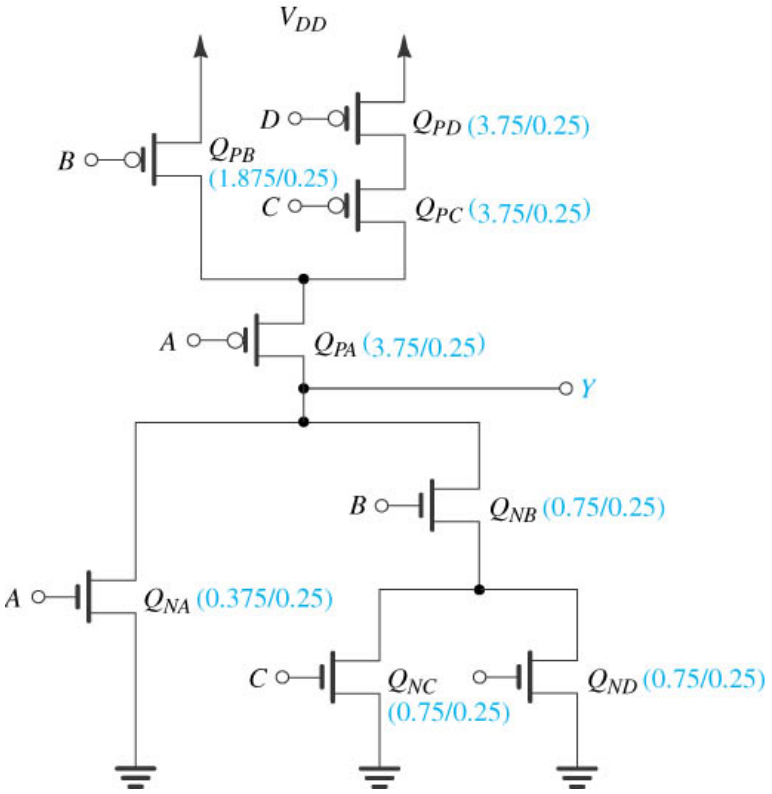




CMOS logic gates

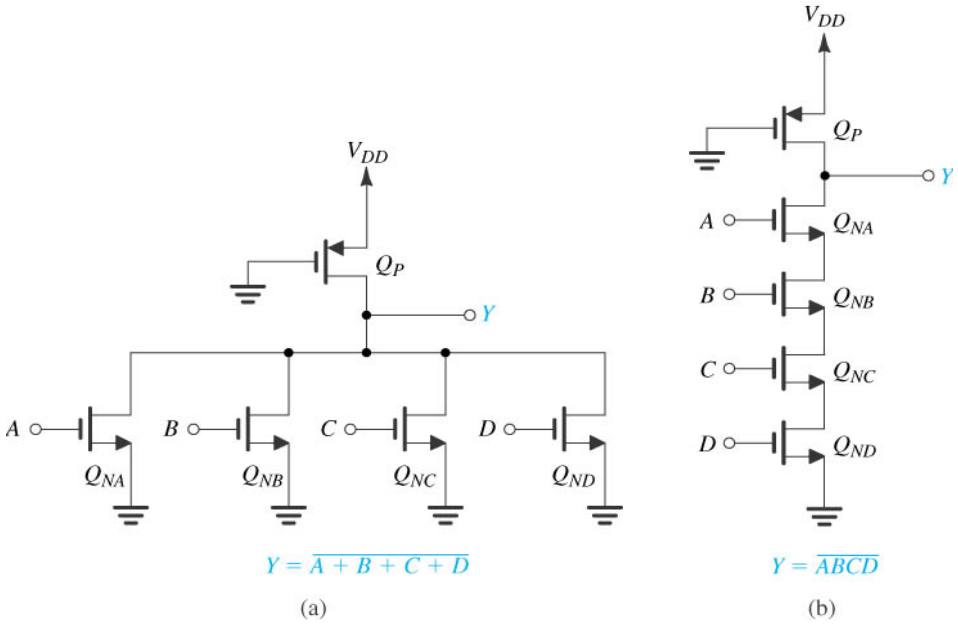
- Transistor sizing
  - To maintain a symmetrical characteristic





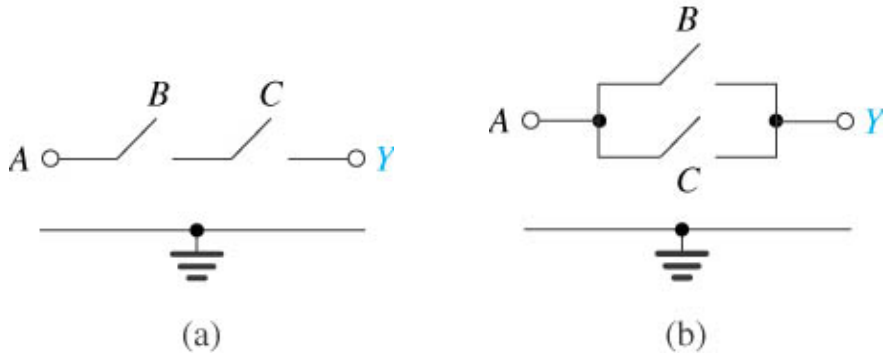
CMOS logic gates

- Pseudo NMOS
  - Think about the area overhead of the pull-up network

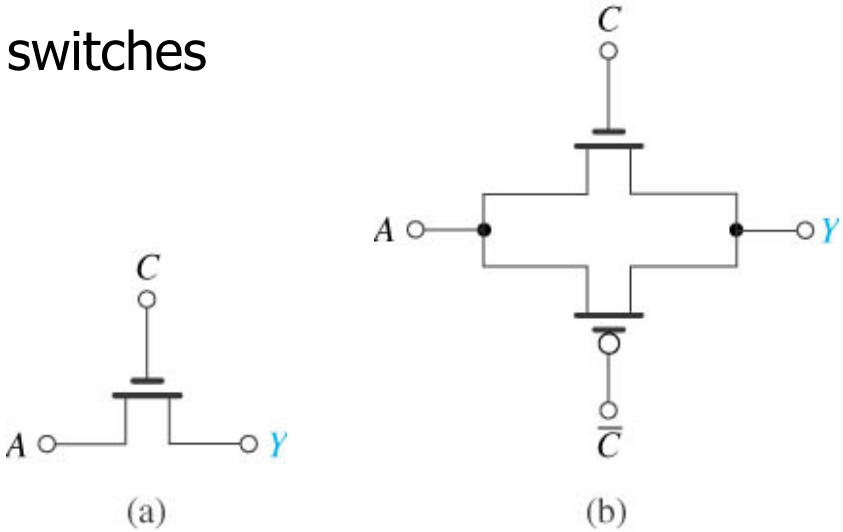


Pass transistor logics

- Pass transistor logics

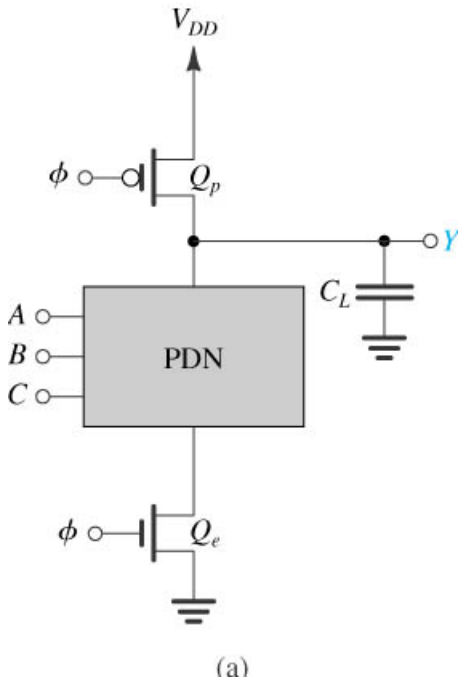


- Pass transistor switches

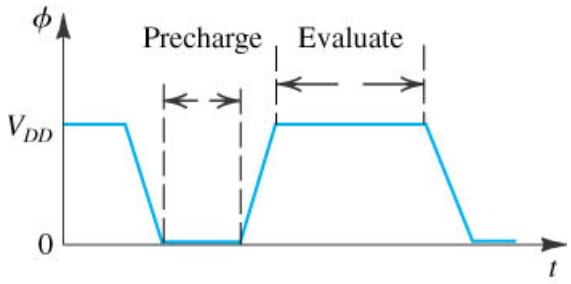


Dynamic logic gates

- Dynamic operation
  - Precharge and evaluation
  - Requires minimum operating speed



(a)



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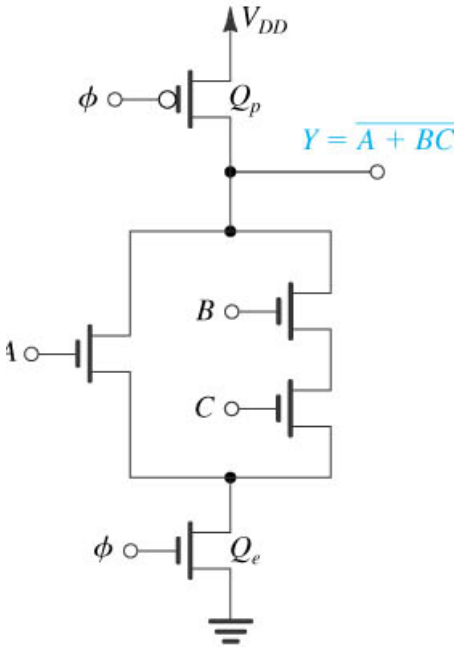

(c)

Note: Some figures are from Microelectronic Circuits fourth edition by Sedra and Smith, Oxford.